

LEAKAGE CURRENT IN SUBMICRON PARTIALLY DEPLETED SOI NMOSFETS OPERATING AT HIGH TEMPERATURES

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ABSTRACT

It is presented numerical bidimensional simulations results concerning to the study of the leakage drain current behavior in submicron partially depleted SOI nMOSFETs operating from room temperature up to 573K. The results show that the leakage current depends strongly on the channel length. Also, it was observed that the leakage current density distribution is non uniform and depends on the channel length and changes as the temperature goes up.

1. INTRODUCTION

Bulk silicon CMOS circuits operation as a function of the temperature is usually limited to approximately 200°C (473 K) due to the leakage current increase [1-4]. Improvements in the modeling and design techniques of integrated circuits operating under severe conditions have prompted renewed-interest on a part of research with respect to applications as well as automobiles, aerospace engines and systems and nuclear power plants [5].

In this paper we present some numerical bidimensional simulations results concerning to SOI nMOSFETs which are fabricated using a submicron CMOS technology, where our goal is to present and discuss the leakage current behavior as a function of the temperature as well its composition as a function of the channel length.

Figure 1 presents the cross section view of the partially depleted SOI nMOSFET analyzed. From that, it is possible to observe some details concerning to the physical dimensions and polarization.

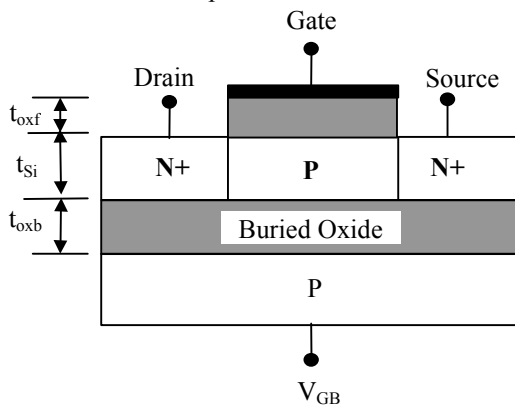


Figure 1 - Cross section view of the submicron partially depleted SOI nMOSFET.

2. DEVICE CHARACTERISTICS

The submicron SOI partially depleted nMOSFETs analyzed has the gate oxide, silicon film and the buried oxide thickness being $t_{oxf} = 2.5\text{nm}$, $t_{Si} = 100\text{nm}$ and $t_{oxb} = 400\text{nm}$, respectively. The doping levels are $N_A = 5.10^{17}\text{cm}^{-3}$ for the channel and $N_D = 1.10^{20}\text{cm}^{-3}$ for the drain and source regions. To develop these studies, it was used devices whose channel length L are between $0.5\mu\text{m}$ and $10\mu\text{m}$.

3. NUMERICAL SIMULATIONS RESULTS

The simulations were performed using the bidimensional numerical simulator ATLAS [6].

To study the drain leakage current I_{Leak} in SOI nMOSFETs operating at high temperatures, it is necessary to extract it from the drain current I_{DS} versus the front gate voltage V_{GF} curves, at the same bias. Then, it was noticed that for $V_{GF} = -1\text{V}$, the current is almost independent of V_{GF} , as it can be seen in figure 2. Similar results were observed for all channel length range studied.

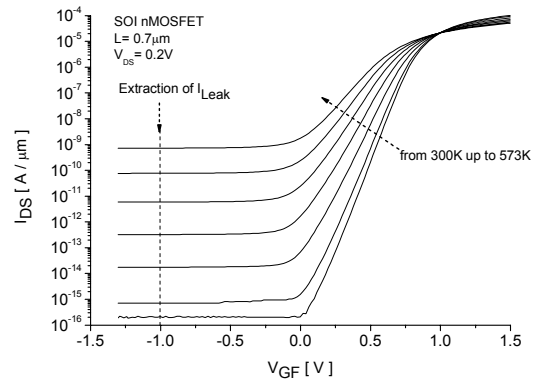


Figure 2 - Extraction of I_{Leak} as a function of the temperature, for the SOI nMOSFET with $L=0.7\mu\text{m}$.

Analyzing the drain leakage current I_{Leak} behavior as a function of the temperature, it can be seen that, for the same device, I_{Leak} increases when the temperature gets high. Otherwise, also, it is possible to observe that as L decreases, I_{Leak} increases when the devices are submitted to the same temperature. These results are shown in figures 3 and 4, for the drain voltage $V_{DS} = 0.2\text{V}$ and the back gate voltage $V_{GB} = 0\text{V}$. Its worthwhile to mention that similar behavior is observed for higher V_{DS} values.

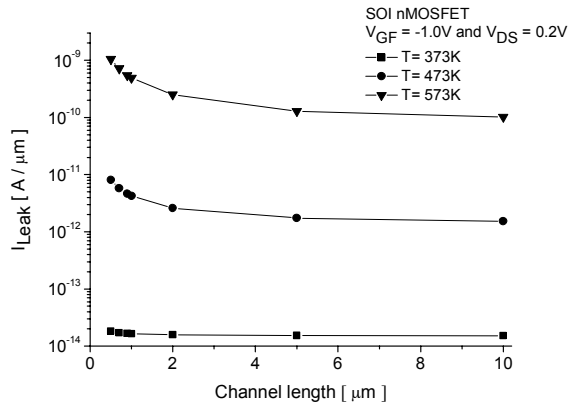


Figure 3 - Drain leakage current behavior in SOI nMOSFETs as a function of the channel length at high temperatures.

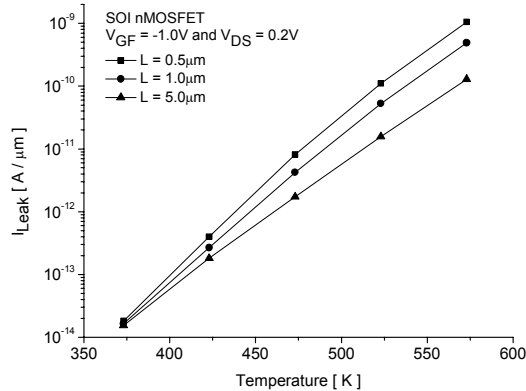


Figure 4 - Drain leakage current evolution in SOI nMOSFETs as a function of the temperature.

In order to understand I_{Leak} evolution as a function of L , the total leakage drain current density J composition was analyzed into the channel along the silicon film depth. Figures 5 and 6 shows these results for L being $0.5\mu m$ and $5.0\mu m$, respectively, at $573K$.

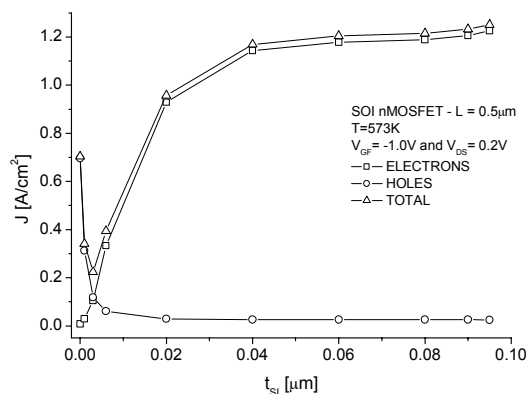


Figure 5 - Leakage current density J composition for the SOI nMOSFET with $L = 0.5\mu m$ at $573K$.

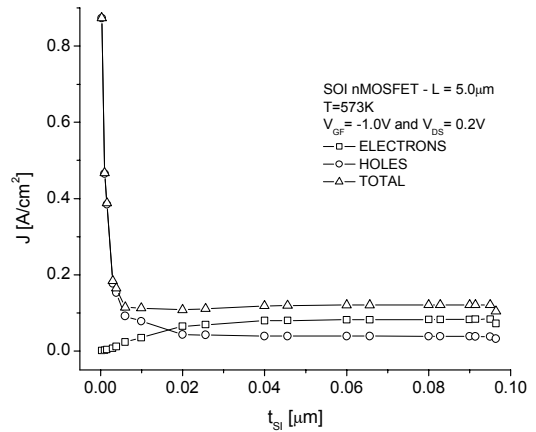


Figure 6 - Leakage current density J composition for the SOI nMOSFET with $L = 5.0\mu m$ at $573K$.

From figure 5, it can see that the total leakage current I_{Leak} is composed mainly by holes in the region near the gate oxide / silicon film interface and by electrons, into the transistor body. Similar behavior is also observed for lower temperatures.

For similar analysis for higher L , as shown in figure 6, it can be seen that the leakage current composition changes just into the body which is composed by the sum of holes and electrons.

From these previous results it is possible to notice that as the channel length reduces, the total I_{Leak} gets higher because the body leakage current increases much more than the gate interface component.

4. CONCLUSIONS

The leakage drain current behavior in submicron partially depleted SOI nMOSFETs is analyzed as a function of the temperature and the channel length changes. It is observed that for $L \gg 1.0\mu m$, I_{Leak} is composed mainly by holes. But as the channel length gets lower, I_{Leak} is higher and it becomes composed mainly by electrons, which explain why the total drain leakage current increases as the channel length reduces. This behavior is observed for all temperature range analyzed in this work.

5. REFERENCES

- [1] J. P. Colinge, Silicon-on-Insulator Technology: Materials to VLSI, 3rd Edition, Kluwer Acad. Pub., Massachussets, 2004
- [2] P. Francis, A. Terao, B. Gentinne, D. Flandre and J. P. Colinge, in IEDM Tech. Dig., p.13.5.1, 1992.
- [3] D. Flandre et al, in IEEE Elec. Dev. Lett., p.14, 1993.
- [4] D.S. Jeon and D.E. Burk, IEEE Trans. On Electron Dev., p.38, 1991.
- [5] A. J. Auberton-Hervé, J. P. Colinge and D.Flandre, in Japanese Solid-State Technology, p.12, December, 1993.
- [6] ATLAS Device Simulation Framework, version 5.10.0.R, Silvaco International, 2005.