DESIGN OF AN ALL-DIGITAL PHASE LOCKED LOOP: ANALYSIS AND CHARACTERIZATION IN FPGAS

Luciano Severino de Paula, Altamiro Amadeu Susin, Sergio Bampi
Universidade Federal do Rio Grande do Sul - UFRGS
Porto Alegre, Rio Grande do Sul, Brazil
{lspaula, bampi}@inf.ufrgs.br, {susin}@eletro.ufrgs.br

ABSTRACT

This paper presents a case study of an ADPLL (All Digital Phase Locked Loop). The designed architecture, based on the Texas 74xx297 integrated circuit, is implemented in a complete VHDL RTL level code and prototyped in a Xilinx Virtex II Pro FPGA board, increasing the level of reusability/portability of the structure. The aim is to obtain some inherent performance parameters of the structure, such as hold range, phase jitter and frequency resolution. First, the design structure is presented followed by some implementation results. A future VLSI integration will make possible to study the influence of the noise generated by the ADPLL structure in the other blocks in a mixed-signal chip.

1. INTRODUCTION

PLL´s in general are used to track and synchronize a particular signal to another. These systems are responsible for synchronizing an output signal, most of the time generated by a local oscillator, with a reference input signal, both in frequency and phase. When the system is in synchronization, often called locked state, we observe a small or even zero phase error between the oscillator output and the reference signal. If some phase error is introduced, a feedback mechanism acts in the DCO in such a way that the error is reduced again to a minimum value. In this condition, the phase of the output signal is actually locked to the phase of the reference signal. There are four types of PLL´s according to [1]: Linear PLL, Classical Digital PLL (DPLL), All-Digital PLL (ADPLL) and Software PLL (SPLL).

In recent technologies the use of PLL's are widely spread from low to high frequencies. The demand on reusability and portability is increasing as the architectures become more flexible [2]. Considering these main aspects, one can use some design methodologies that allows a fully digital implementation. Different from the mixed-signal implementations, the top frequency obtained by the all digital design implementation is connected to the frequency that the FPGA device reaches.

2. ADPLL OVERVIEW

In some cases, the implementation of an exclusively digital PLL is advantageous compared to the mixed signal version. An example of that is when power management is an important issue. With ADPLL is possible to shutdown to zero the dynamic power consumption of the unit [4]. With the use of ADPLL some other relevant aspects can be minimized, such as sensitivity to DC drifts, component saturation, difficulties on implementing superior order loops besides the fact that is not necessary to perform initial calibration and periodical adjustments to the structure. The fact of implementing architecture by only using digital blocks lead us to an increase in the portability/reusability of the architecture.

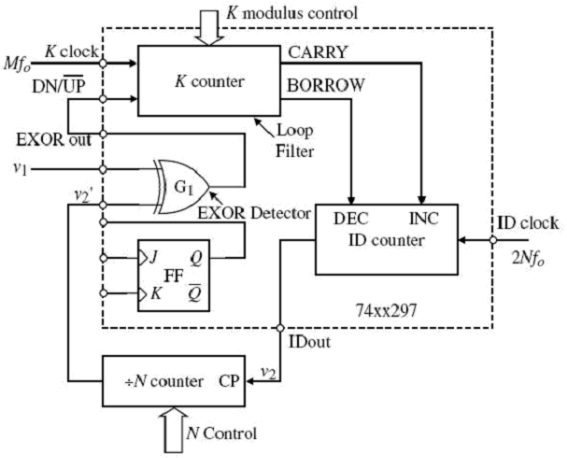

Figure 1. Internal structure of the 74xx297 integrated circuit [5]

The ADPLL works differently from the traditional PLL systems but based upon the same concept, since the involved signals are fully digital [5]. For a digital phase locked loop, the input signal is a bit stream. The bit stream can have a variety of sources including an analog-to-digital (ADC) converter or a regular bit stream with which the receiver must synchronize.

3. ADPLL STRUCTURE

The present design is based in the Texas Instruments 74xx297 [3] integrated circuit which contains all the blocks necessary to perform an ADPLL design as stated in [5]. The complete architecture described on figure 1 was implemented in a VHDL code.

3. CASE OF STUDY

As a case of study we intend to implement an ADPLL in a Xilinx FPGA board. In order to demonstrate and validate the ADPLL structure, a target of 16 frequency channels was set.

3.1. Design Procedure

The design procedure, based on [1] and [6], returned the following results for the calculation of the ADPLL parameters (N=16, K=8, M=2N=32):

- $f_o = 312.5KHz$
- The Lock Range $(f_{in} - f_o)$ is:

$$\Delta f_{MAX} = \frac{f_o \cdot M}{2 \cdot K \cdot N} = 39.0625KHz$$

- The frequency resolution is:

$$\Delta f = \frac{2 \cdot f_o}{K \cdot N} = 4{,}883KHz$$

- So, the output frequencies are in the range of:

$273.438KHz < f_2 < 351.563KHz$

4. SIMULATION RESULTS

All blocks where designed and validated through electrical simulation using the XILINX Modelsim tool. The results of the implementation are shown in fig. 2. In the same figure we can observe the addition/suppression of pulse in the ID out signal which is responsible for the maintenance of the locked state.

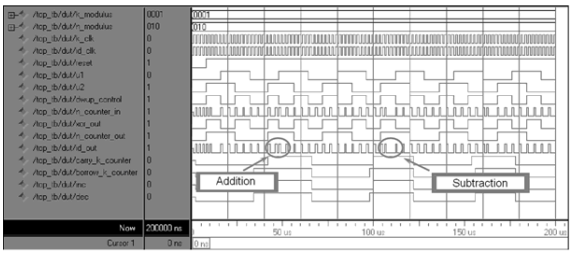

Figure 2. Simulation waveforms

5. EXPERIMENTAL RESULTS

After the simulation, the system was prototyped in a Virtex II Pro (XC2VP30) FPGA board. This prototipation makes possible practical evaluation of the main parameters involved. The FPGA logic utilization is shown in table I. Simulation and practical results are shown in table II, where we can observe good coherence between them.

TABLE I. FPGA RESOURCES USED AFTER THE SYNTHESIS

Logic utilization	Used	Available
Flip Flops	91	27392
LUT´s	147	27392
IOB´s	17	556

TABLE II. SIMULATION AND PRACTICAL RESULTS (M = 2N = 8; FO = 312.5KHz; K CLOCK = I/D CLOCK = 10MHZ)

Parameter	Calculated Results	Simulated Result	Practical Results
Lock Range	39.0625KHz	39.12KHz	39.14KHz
Frequency Resolution	4.883KHz	4.89KHz	4.893KHz
Lock In Period	-	320µs	450µs
Phase Jitter	-	≈ 11°	≈ 14 °

The measurement results obtained through an Agilent Logic Analyzer (16903A) can be viewed on figure 3. In this figure we can observe the addition/suppression of pulse in the ID Out signal and the ripple generated in the internal signals of the K counter (Borrow, Carry and Toggle FF). This ripple takes no influence on the external signals because its period is less than the necessary to switch the ID counter.

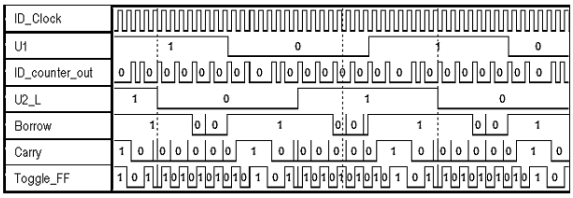

Figure 3. Logic Analyzer Waveform data from FPGA implementation

In order to achieve wide frequency coverage, the implementation was tested in all frequencies up to 100MHz. The measured data is shown in table III.

TABLE III. MAXIMUM FREQUENCY (M = 16; N = 8; K=8)

Mfo=2Nfo		Calculated Results	Practical Results
100MHz	f_O (MHz)	6.250	6.2245
	Δf_{MAX} (KHz)	1562.5	1552.4
	Δf (KHz)	390.625	388.4

6. CONCLUSION

With the measurements we can observe that the results obtained with this structure validate the design methodologies and required specifications.

As future work, we intend to integrate this system in a target CMOS technology. The purpose of this prototipation is to evaluate the influence of the noise generated by the ADPLL structure referred to other blocks in a mixed-signal chip.

7. REFERENCES

[1] R. E. Best, "Phase-Locked Loops," 2nd ed., New York, McGraw-Hill, 1993.

[2] Y. H. Temg, B. Shieh, C. Lee, "An all-digital phase-locked loop (ADPLL)-based clock recovery circuit," *Solid-State Circuits, IEEE Journal of Solid State Circuits*, Volume 34, Issue 8, Aug. 1999, Page(s):1063 – 1073.

[3] Texas Instruments Technical Datasheet, Digital Phase-Locked-Loop Filters. SN54/74LS297, 1981.

[4] J. Dunning, G. Garcia, J. Lundberg, E. Nuckolls, "An all-digital phase-locked loop with 50-cycle lock time suitable for high-performance microprocessors," *Solid-State Circuits, IEEE Journal of Volume 30*, Issue 4, April 1995 Page(s):412 – 422.

[5] D. G. Troha, " Digital Phase-Locked Loop Design Using SN54/74LS297," TI Application Notes, May 1997.

[6] M. S. Mousa, "Design of ADPLL for Good Phase and Frequency Tracking Performance," *Proceedings of 19th National Radio Science Conference*, Alexandria, March 2002.