AUTOMATIC ANALYSIS OF SET PROPAGATION IN CMOS COMBINATIONAL CIRCUITS

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ABSTRACT

State-of-the-art CMOS circuits are sensitive to faults caused by single event transients (SETs). Traditionally, the circuit SET propagation analysis is performed by circuit simulation. Although very accurate, circuit simulation demands long execution times. In this paper, we propose and evaluate an alternative method to analyze SET propagation in CMOS logic circuits. Such method uses a timed-logical computation, avoiding circuit simulation. Preliminary results have shown that the proposed method is very accurate when compared to Hspice simulations.

1. INTRODUCTION

Due to the continuous evolution of the fabrication technology process of semiconductor, which leaded to reduced transistor dimensions and low power supply voltages, integrated circuits fabricated on the very deep sub-micron technology (VDSM) are becoming more sensitive to faults. One example is the soft error, produced by the interaction of charged particles presented in the atmosphere and neutrons presented at ground level with the silicon substrate. This collision generates a local area ionization that can charge or discharge the circuit capacitor nodes provoking upsets with transient effect.

A single particle can hit either the combinational logic or the sequential logic in the silicon. When a particle strikes one of the sensitive nodes of a memory cell, the effect can produce an inversion in the stored value, in other words, a bit flip in the memory cell. This is called Single Event Upset (SEU) [1]. When a particle hits a combinational logic block, it also generates a transient current pulse. This phenomenon is called Single Transient Efffect (SET) [2]. If the induced transient pulse is not logically or electrically masked by the circuit, then the SET will eventually appear at the input of flip-flop, where it may be interpreted as a valid signal.

Evaluating the SEU and SET sensitivity of an integrated circuit in an early phase of the design cycle is mandatory to determine which part of the circuit must be protected against upsets. However, the analysis of a SET can be high time costly due to the propagation analysis, which is usually performed by electrical simulation. In particular, electric-level simulation is the most accurate evaluation technique because it takes into account the detailed electrical behavior of circuits and the shape of the deposited current pulse (SET). However, circuit simulation demands long CPU times which, for complex circuits, can be from hundreds to thousands of hours [2], rendering difficult to meet time-to-market requirements.

In this paper, we present a method to automatically analyse the propagation of SETs in CMOS logic circuits without using electrical circuit simulation. A tool was developed to evaluate the SET propagation by using an analytical model. Results for a case-studied circuit show the accuracy of our method comparing an exhaustively electrical simulation.

2. PROPOUSED METHOD

To develop an alternative method for the SET propagation analysis, we assume that only one particle hits the circuit, causing a SET at only one gate output. We also assume that circuit outputs are stable under a given input vector v_i when the particle hits the target gate. Since it is impossible to predict the instant when a particle hits the circuit, we assume that the generated SET will have enough time to propagate from its origin forward the circuit outputs. To complete our modeling, the analog nature of a SET must be adapted to a discrete pulse, which may be accomplished by assuming its amplitude as being a complete voltage swing from zero to Vdd (or *vice versa*).

In the pre-processing phase, an input vector v_i is propagated from the inputs to the outputs of the circuit, while the resulting logic values are being saved at the circuit gates. The method could be formalized as follows. Let C be a circuit composed of n logical gates. Suppose one wants to evaluate the propagation of a SET with duration d_i occurring at the output of gate g_i (with $0<i<=n$). The SET and its duration are assigned to the output connections of gate g_i and the logic cone starting at g_i is identified. Then, two steps are performed for every input vector v_i: input vector propagation and SET propagation. Let g_i be a gate where the SET occurs and let d_i be the SET duration. Figure 1 shows the pseudo-code for the proposed method.

In the propagate_vector procedure, a given vector v_i is applied to the circuit inputs and its effect is propagated to the outputs using the classical topological sort algorithm [3].

```
find_logical_cone(gi)
for_each v_i
        propagate_vector(v_i)
        propagate_SET(d_i , g_i)
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Fig. 1 - Pseudo-code to evaluate the sensitivity of gate g_i to a SET with duration d_i

During this first propagation step the resulting logic values *lv* are assigned to the circuit lines. In the propagate_SET procedure, all gates with fan-out of g_i are inserted in a processing FIFO. This FIFO assures that gates are processed in a topological manner: a gate is inserted in the processing FIFO only if all of its predecessors have already been processed. The evaluation of the SET for vector v_i ends when the FIFO is empty.

The processing of a gate g_k, within the propagate_SET procedure consists on one or on two steps. The first step evaluates the waveform of the signals at the inputs of g_k to determine whether a SET can propagate through it or not. This step will be referred as an "*equivalent input waverform*". If a SET propagates through g_k, then the SET duration at the g_k's output is computed applying the propagation function of g_k to the "equivalent input waverform" obtained in the previous step. This second step will be referred to as "SET interval computation".

Although it is assumed that only a SET is generated, the input waveform evaluation step must consider that more than a SET may arrive at the inputs of a gate. This occurs because a SET at the output of a gate with fan-out greater than one will generate transients in all of the fan-out lines. Therefore, a gate that has reconvergent lines as fan-in can present transients at more than one input.

In the following explanation we assume that, given a gate g_k, c(g_k) denotes its controlling value and nc(g_k) denotes its no controlling value.

In the analysis of the waveform at the inputs of gate g_k, one of the three possible situations occurs:

i) At least one input of *gk* has c(g_k) and such input does not have transients. In this case, a logical masking occurs and no pulse is propagated to the output of g_k.

ii) There is at least one input of *gk* with c(g_k), but all inputs exhibiting c(g_k) have a transient. In this case, the resulting transient is computed as the intersection between the durations of the transients at the inputs that have c(g_k). Figure 2 illustrates this situation.

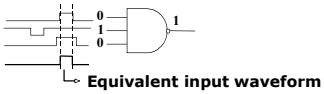

Fig. 2 - Situation ii.

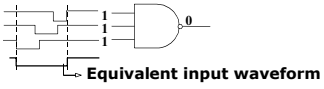

Fig. 3 - Situation iii.

iii) All inputs of gk have nc(g_k). In this case, the resulting transient is computed as the union between the durations of the all transients at the inputs of g_k. Figure 3 shows this situation.

In the SET interval computation step, a "gate propagation function" is used to compute SET duration at the gate's output. For instance, consider that the equivalent waveform in g_k input begins at instant *tb* and ends at instant *te*. Then, the bounds tb_{out} and te_{out} on the pulse at the output of gate g_k may be computed as follows.

For a 0→1 pulse:

$$tb_{out} = tb + tplh \qquad te_{out} = te + tphl \quad (2)$$

And for a 1→0 pulse:

$$tb_{out} = tb + tphl \qquad te_{out} = te + tplh \quad (3)$$

3. PRELIMINAR RESULTS AND CONCLUSIONS

To evaluate the considered method, a prototype of a tool was developed. A 90nm one-bit full adder circuit was used to compare the results obtained from the proposed tool to ones obtained by Hspice electrical simulation. Tests were realized with SET occurrences in all gates of the circuit and analyzing the propagation for input vectors.

The results obtained show that a tool can correctly identify all cases of propagation until primary outputs. Comparing the duration of the pulse showed in primary outputs (considering all cases of propagation), the maximum error between the Hspice results and the prototype results is 13%.

The obtained results have revealed the possibility to use the proposed method to the SET propagation analysis. Some modifications can be introduced in this method, such as having a more efficient equivalent wave form or a gate propagation function considering electrical masks [4], which would increase its precision. The execution time of the prototype is about 1000 times faster than the Hspice simulations, what *per se* justifies the utility of the proposed method.

4. REFERENCES

[1] R. C. BAUMANN, "Soft Errors in Advanced Semiconductor Devices - Part I: The Three Radiation Sources", *IEEE Transactions on Device and Materials Reliability*, Vol. 1, No. 1, March 2001.

[2] D. ALEXANDRESCU, L. ANGUEL, M. NICOLAIDIS, "New Methods for Evaluating the Impact of Single Event Transients in VDSM ICs" *17th IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems*, 2002.

[3] T. H. CORMEN, C. E. LEISERSON, R. L. RIVEST, R. L., "Introduction to Algorithms", Cambrige: MIT, 1990.

[4] G. WIRTH, M. VIEIRA, E. HENES NETO, F. KASTENSMIDT, "Single Event Transients in Combinatorial Circuits", In: *16th International Symposium on Integrated Circuits and Systms Design"*, 2005, Florianópolis. Proceedings. New York (USA): ACM: Association for Computing Machinery, 2005. p. 121-126.