THRESHOLD VOLTAGE OF DOUBLE AND TRIPLE GATE SOI FINFET

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ABSTRACT

The FinFETs are devices of vertical channels with gates allocated in different planes that result in a three-dimensional structure. They are one of the most promising technological solutions to create high-performance ultra-scaled SOI CMOS. In this work the behavior of the threshold voltage in double-gate and triple-gate SOI FinFETs transistors with different channel doping concentrations is studied through three-dimensional simulation. The results indicate that in double-gate a single threshold voltage is observed due to the inversion in both gates sides independent of the channel doping concentration. However in triple-gate it is possible to observe up to three threshold voltages due to the corner effect and the different concentration between the up and down sides of the Fin.

1. INTRODUCTION

In the last few years, the CMOS industry has witnessed a striking progress in downsizing the planar devices. However, scaling planar CMOS to 10 nm and bellow would be exceptionally difficult, due to electrostatics, excessive leakages currents, mobility degradation and short channel effect [1].

Non-planar devices provide potential advantages in packing density, carrier transport and device scalability for postponed the limits above [1].

Nowadays, focus of the industry has been pointing to FinFET, that is a transistor with double-gate or triple-gate, quasi-planar structure and relatively simple fabrication [2]. The FinFETs present higher mobility, higher drive current density (per transistor area), near ideal subthreshold slope and improved short channel effect [3, 4, 5].

In spite of their exceptional electrostatic control, these architectures FinFETs exhibit corner effects. This effect degrades the properties of FinFETs and can affect the threshold voltage. The corner effects are higher when the doping concentration is high and the corners radii of the curvature are small [6, 7].

Figure 1 shows the double-gate and triple-gate SOI FinFETs transistors structures and figure 2 shows the cross sections channel regions Fins of the double-gate and triple-gate.

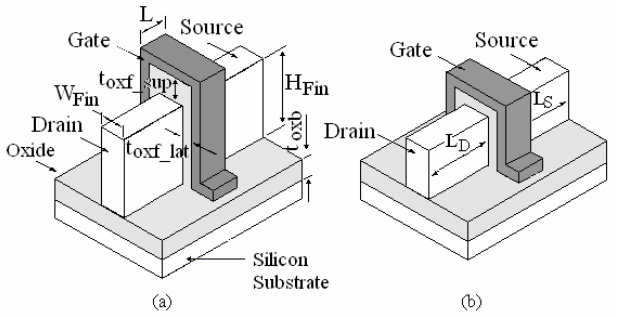

Figure 1 – SOI FinFETs transistors: Double-gate (a); Triple-gate (b).

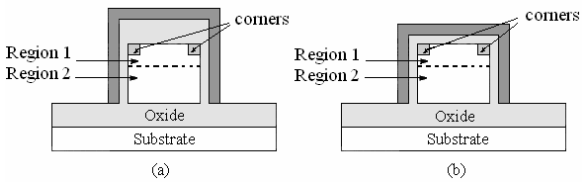

Figure 2 – Cross section view of the FinFETs showing the channel regions and corners: Double-gate (a); Triple-gate (b).

Other important factor that also degrades the properties of FinFETs and can affect the threshold voltage is the different channel doping concentrations [8].

2. DEVICE CHARACTERISTICS

The simulated structures with double-gate and triple-gate SOI FinFETs present the following characteristics: buried oxide thickness t_{oxb} = 145 nm, equivalent gate oxide thickness t_{oxf_lat} = 2 nm; t_{oxf_sup} = 100 nm for double-gate and t_{oxf_sup} = 2 nm for triple-gate, drain and source length $L_D = L_S$ = 100 nm. The channel width is equal to 120 nm; the height of Fin H_{Fin} is 60 nm and the channel length L = 1 μm. The channel of the device was divided in two regions, as shown in Figure 2. Region 1 has channel width W_{Fin} = 120 nm and height H_{Fin} = 5 nm. Region 2 has channel width W_{Fin} is 120 and height H_{Fin} is 55 nm.

The silicon doping concentrations for the drain and source are $N_D = 1 \times 10^{20}$ cm^{-3}. Region 1 of the channel has $N_A = 8 \times 10^{18}$ cm^{-3} and $N_A = 1 \times 10^{19}$ cm^{-3}. Region 2 of the channel silicon doping concentration ranging from $N_A = 3 \times 10^{18}$ cm^{-3} to $N_A = 5 \times 10^{18}$ cm^{-3}. The interface charge densities of 3×10^{10} cm^{-2} and the applied voltage to the drain was of $V_D = 100$ mV. The simulator used was the Atlas of Silvaco [9].

In this work the threshold voltage is extracted by the transcondutance charge method (MTC). According to this method, the threshold voltage can be defined as the gate voltage where the derivative of the transcondutance (d^2I_D/dV_G^2), reaches a maximum value, or, mathematical terms, when $d^3I_D/dV_G^3 = 0$ [10, 11].

3. FINFET THRESHOLD VOLTAGE

Figure 3 presents the curve of the second derivative of the drain current versus gate voltages characteristics for double-gate FinFETs with different doping concentrations in both channel regions. In all cases a single threshold voltage (just a single peak for each curve) is observed. This threshold voltage is due of lateral conductions in Fin (channel).

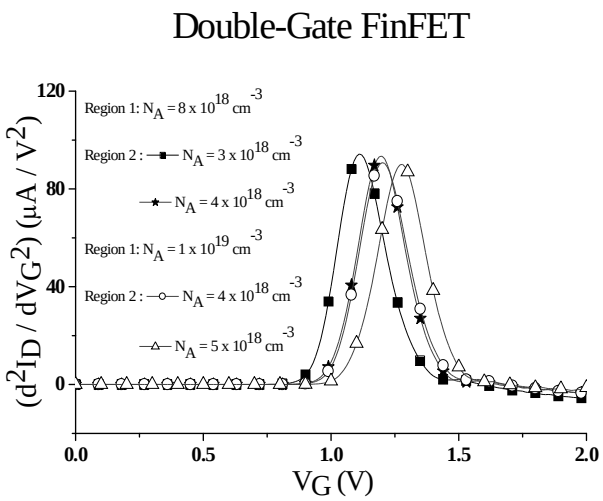

Figure 3 – $d^2 I_D/dV_G^2$ versus V_G for double-gate FinFETs with different doping concentrations.

Figures 4 and 5 show the same curves for triple-gate FinFETs. In this case the presence of three threshold voltages is observed for each curve (3 peaks) called V_{T1}, V_{T2} and V_{T3}.

V_{T1} correspond to the voltage threshold of the top corners, once these are submitted to the vectors of electric field generated by the lateral and top gates simultaneously.

V_{T2} is due to the inversion of the lateral surfaces (controlled by the lateral gates) as in double-gate FinFETs.

V_{T3} is related to the top gate inversion (region 1) where the top doping concentration is higher than in the remaining of the channel (region 2).

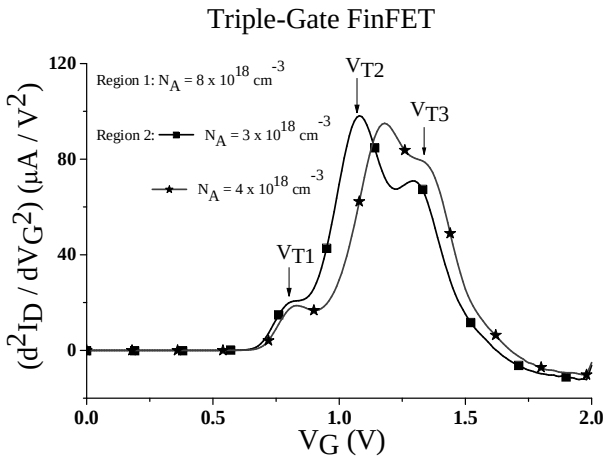

Figure 4 – $d^2 I_D/dV_G^2$ versus V_G for triple-gate FinFETs with different doping concentrations.

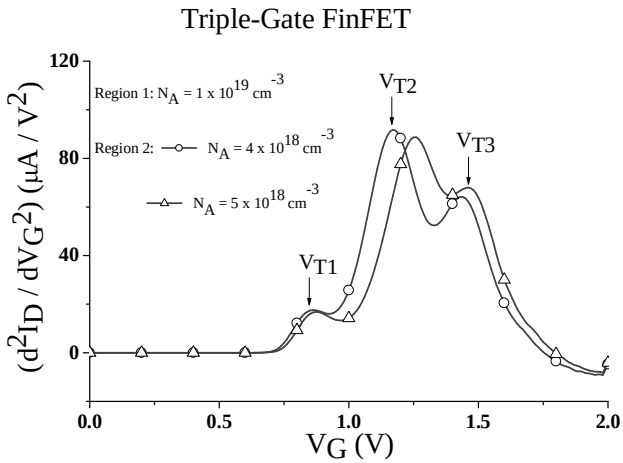

Figure 5 – $d^2 I_D/dV_G^2$ versus V_G for triple-gate FinFETs with different doping concentrations.

Table 1 shows the results of the threshold voltage obtained in the Figures 4 and 5.

Table 1 – Threshold voltage of triple-gate FinFETs with different doping concentrations.

Doping Concentrations Channel Regions (cm^{-3})		Threshold Voltage (V)		
Region 1	Region 2	V_{T1}	V_{T2}	V_{T3}
8×10^{18}	3×10^{18}	0.82	1.08	1.29
8×10^{18}	4×10^{18}	0.83	1.18	1.34
1×10^{19}	4×10^{18}	0.86	1.17	1.43
1×10^{19}	5×10^{18}	0.87	1.26	1.46

Figure 6 presents the curve of the second derivative of the drain current versus gate voltage characteristics for double-gate and triple-gate FinFETs with channel doping concentration of $N_A = 1 \times 10^{15}$ cm^{-3}.

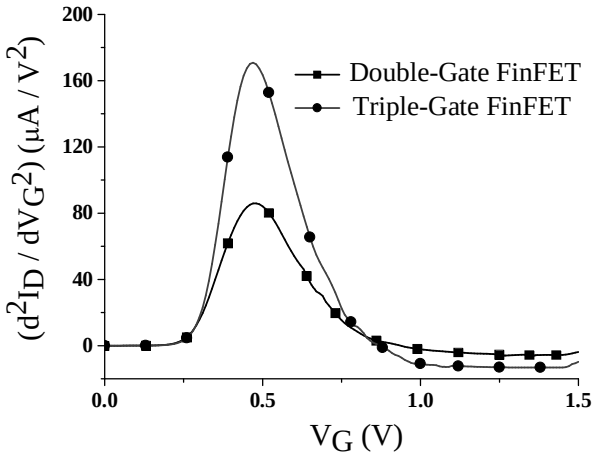

Figure 6 – $d^2 I_D/dV_G^2$ versus V_G for double-gate and triple-gate FinFETs with channel doping concentration of $N_A = 1 \times 10^{15}$ cm^{-3} and $W_{Fin} = 120$ nm; $H_{Fin} = 60$ nm; $L = 1$ μm.

It is observed that devices with the lowest doping concentration exhibit a single peak, just one threshold voltage. This threshold voltage is due to corners and edges inversion (up and side wall) at the same time.

4. CONCLUSION

Double-gate FinFETs present a single peak in the second derivative of the drain current versus gate voltage curve, which means a single threshold voltage, independent of the doping concentration in channel regions. A double-gate has not electrostatic potential influence of the top gate.

However, the triple-gate FinFETs can present up to three threshold voltages which depend on the corners, up and lateral side condition of the Fins.

The devices with the highest and different doping concentrations in the regions present three threshold voltages being these V_{T1}, V_{T2} and V_{T3} that are due to the threshold voltage of the top corners, once these are submitted to the vectors of electric field generated by the lateral gates and top gate; the inversion of the lateral surfaces (controlled by the lateral gates) and the inversion caused by the top gate respectively.

The triple-gate devices with low doping concentration exhibit a single hump indicating only one threshold voltage, because the inversion of the lateral and top surfaces (controlled by the lateral and top gates) happens at the same time of the corners. A low channel doping reduces the electrostatic potential influence of the top gate and corners.

5. REFERENCES

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