CHARGE PUMP CURRENT LIMITATION AND DRIVER

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ABSTRACT

This paper presents a new Charge Pump current limiter scheme. The current limitation system and the Driver equations will be presented and described. Simulations have been done for a typical case, as well as taking temperature and process variation into account. ELDO simulator has been used with AMS 0.35um H35 fabrication process models. The Driver circuit layout has been done and will also be presented on this paper.

1. INTRODUCTION

One important function on integrated systems for Power Management applications is the Power Stage current limitation. This current limitation protects the system from current transient, and protects the output system from a short to ground. Also, it limits the maximum system power dissipation, avoiding system damage. A new current limitation system has been designed to limit the output current of a Bridge Voltage Duplicator Charge Pump [1]. This limitation concerns the output voltage level of the Charge Pump system and it protects the system until the output capacitor reaches a known voltage level, roughly 2.6V. Thereby, the current limitation avoids capacitor current peak, protecting power switches from damages. The limitation system core is a Driver, which limits the output current, and a voltage Comparator. Both have been realized on CMOS technology. The Driver circuit demands a reference current on the order of μA to limit currents around mA flowing through the power switches.

2. THE CURRENT LIMITATION SYSTEM

The main idea of the current limitation circuit is to saturate the power transistors and make them work as current sources. Therefore, the current driven through the transistors tends to be invariable and it is possible to limit the current at a desired level.

Figure 1 shows the block diagram of the Current Limitation System. The circuit compares a fraction of the Charge Pump output voltage to a voltage reference. The output voltage depends on the load current and the switches resistance, so that if the load current rises, the output voltage drops. Then, the Comparator generates a flag to the Driver whenever the Charge Pump output voltage becomes smaller than the reference voltage.

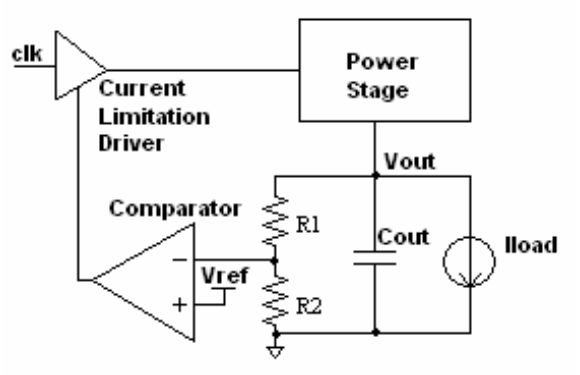

Figure 1 Block Diagram of the Current Limitation System.

This current limitation avoids then damage due to transient current peaks at the Charge Pump start-up. In fact, avoiding current peaks as the circuit starts up is one of the most important features of a Charge Pump due to the fact that it does not have inductors to help on limiting in-rush currents.

The advantage of sensing the Charge Pump output voltage is to avoid power switches current peak after the output capacitor has suffered an intense discharge (like a shortcut to ground). Another advantage is to prevent from oscillations due to short period current peaks (much shorter than clock period). The disadvantage is however the capacitor charge time. The capacitor takes relatively a long time to reach the desired voltage level because of its limited charge current.

3. CURRENT LIMITATION DRIVER CIRCUIT

Figure 2 illustrates the circuit schematic of the Current Limitation Driver. A couple of switches (m_9 and m_6) form an inverter. The transistor M3 is a switch that enables the Driver function if the “ctrl” net is low. Otherwise, it performs as a current limiter. Working as a current limiter, transistors m_5 and m_3 operate on the triode region. The transistor m_5 allows that

m_14 gate voltage goes to the "output" net. The transistor m_3 allows a reference current through transistor m_1, which generates the reference currents to M6, m_14 and M9. The part of the circuit comprised by M9, M6, m_4 e M1 supplies the power transistor when the Driver operates as a current limiter. The transistors M2 and m_14 provide the source to gate voltage (Vgs) to the output power transistor. Therefore, this part of the circuit is responsible for keeping the power transistor operation in the saturation region. Then, it works as a current source and the power switch current limit can be approximated by

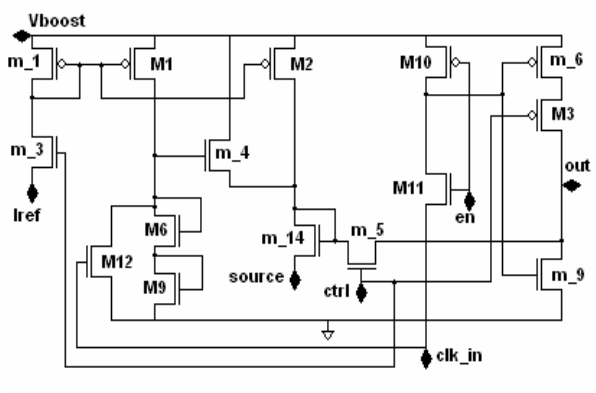

Figure 2 Circuit Schematic of the Current Limitation Driver.

$$I_{Limit} = \frac{\beta_{ch}}{2} * \left(Vt_{m\_14} + \sqrt{\frac{2 * Iref}{\beta_{m\_14}}} - Vt_{ch} \right)^2 \quad (1)$$

where,

β_{ch} : k_n'* Cox * $(W/L)_{ch}$ (power transistor) .

Vt_{ch} : threshold voltage of power switch.

Iref : reference current of the current limiter circuit.

The limit current depends then on the switch transistor and m_14 threshold voltages. Furthermore, it is known that a MOS threshold voltage depends on the bulk to source voltage

$$Vt_N = Vt_{N0} + \gamma * \left(\sqrt{V_{SB} + |2 * \phi_F|} - \sqrt{|2 * \phi_F|} \right) \quad (2)$$

Since $V_S \neq V_B$ on most devices, and V_S depends on Vgs_{m_14}, the threshold voltages relies on Vgs_{m_14}. Another important consideration is the fact that the Driver must supply current to the power transistor gate capacitance as soon as it starts working as a current limiter. The supplying current is provided by transistor m_4, whose magnitude is given by

$$Idrive = \frac{\beta_{m\_4}}{2} * \left(Vgs_{M6} + Vgs_{M9} - Vgs_{m\_14} - Vt_{m\_4} \right)^2 \quad (3)$$

where Idrive is the Driver output supplying current.

As it can be noted, Idrive depends on Vgs_{m_14}, which affects the threshold voltage of the power transistor and consequently, the power transistor limited current. Then, β_{m_4}, Iref, β_{m_14} and β_{ch} must be adjusted to provide the right current limitation, so that Idrive supplies properly the gate capacitance.

4. CURRENT LIMITER CIRCUIT SIMULATION

Figure 3 shows the Current Limiter Simulation bench, whereas Figure 4 depicts the Current Limiter simulation at a typical (27°C and typical process) case.

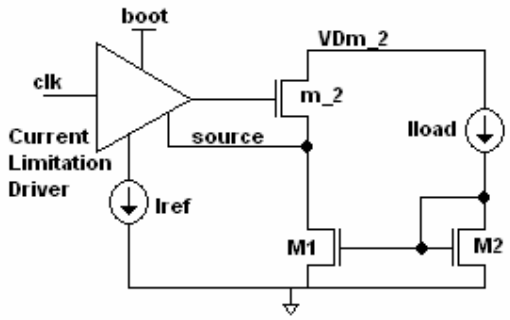

Figure 3 Current Limiter Simulation Bench.

For boot = 5.5V, VD_{m_2} = 1.5V, Iref = 2uA, $(W/L)_{M6}$= $(W/L)_{M9}$= 1u/5u , $(W/L)_{m\_4}$ = 10u/2u , $(W/L)_{m\_14}$= 10u/0.5u and $(W/L)m\_2_{(ch)}$= 8000u/0.5u, $Iload_{máx}$ = 120mA, the power transistor limited current is 30mA. It is possible to observe in Figure 4 that before reaching 1ms of simulated time, the Driver works as a Current Limiter. Afterward, it functions normally as a Driver, when power transistor conducts the maximum load current.

Figure 5 shows the simulation waveforms, taking temperature and process variation into account. For all cases, AMS 0.35um H35 fabrication process parameters and models were used.

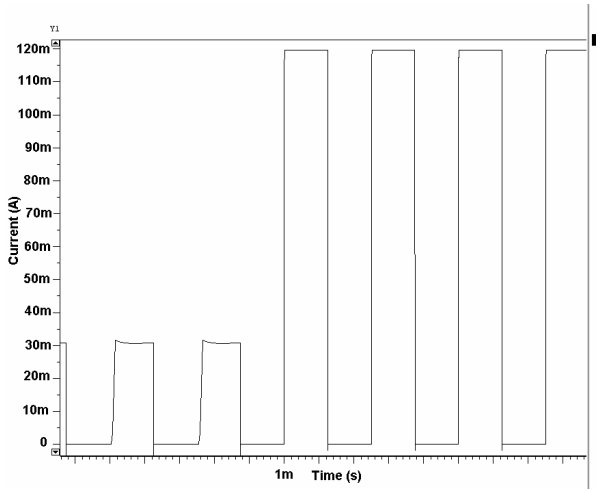

Figure 4 Current Limiter typical waveforms.

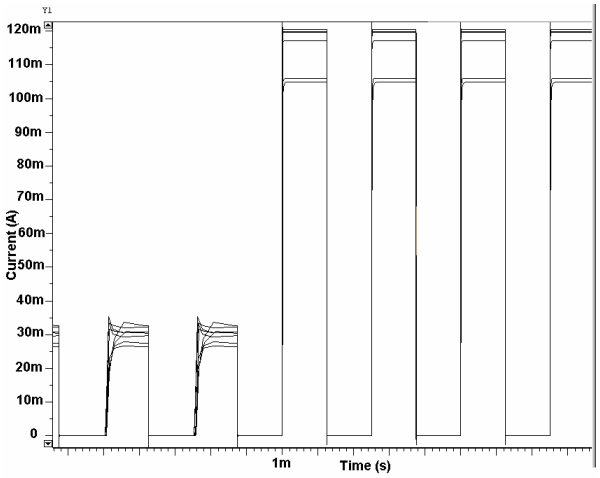

Figure 5 Current Limiter waveforms against temperature and process variations.

For temperatures from -40°C to 125°C the limited current variation is +/-5%, process variations cause a +/-7% simulation results revealed the Current Limiter features +/-11.3% of variation on the limited current, taking all variations into account. In addition, it is worthy noticing that the presented waveforms are close to square waves, with fast transients, which is important to reduce charge losses [2].

5. LAYOUT

Figure 6 shows the Layout of the Current Limiter Driver. Layout size is 53.9um x 43.5um in AMS 0.35um H35 fabrication process. The Driver circuit is a full-MOS structure, so that a BiCMOS process is not required for its design.

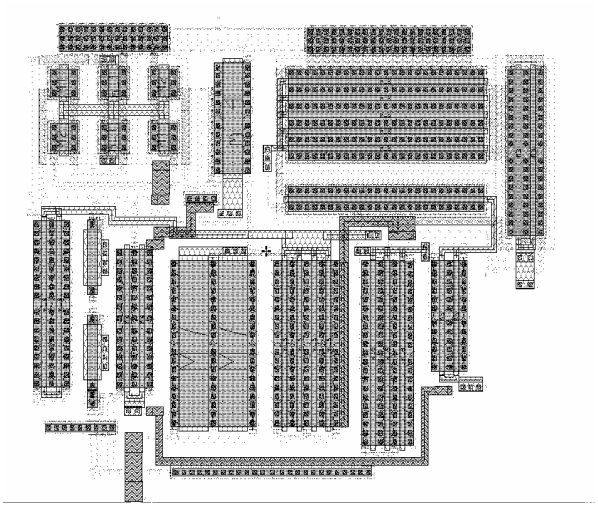

Figure 6 Layout of the Current Limiter Driver.

6. CONCLUSION

A circuit that performs a current limitation on Charge Pumps, whose current limit is controlled by the Charge Pump output voltage, has been presented. The proposed circuit is based on a Voltage Comparator and a Current Limiter Driver.

The equations presented on this paper show that the current limitation depends on the transistors parameters, as well as on the approach of output current Driver. Also, threshold variation is taken into account on the calculation of the current limit value. Moreover, the current waveforms are square-wave shaped, which is essential to minimize charge losses.

The Layout combines both digital and analog cells on the same bulk and its total size is 53.9um x 43.5um. For a 5.5V supply and 2uA reference current, it has been possible to limit a power transistor current on 30mA within +/-11.3% deviation, taking temperature and process variations into account.

7. ACKNOWLEDGEMENT

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8. REFERENCES

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