TRANSCONDUCTANCE AND TRANSCONDUCTANCE OVER DRAIN CURRENT RATIO BEHAVIORS IN CIRCULAR GATE SOI nMOSFET BY USING 0.13 μm PARTIALLY-DEPLETED SOI CMOS TECHNOLOGY.

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ABSTRACT

This paper studies the transconductance and the transconductance over drain current ratio behaviors in circular gate by using 0.13 μm partially-depleted SOI CMOS technology, based on experimental results, at room temperature. The drain/source asymmetric effects are considered in terms of drain current as a function of the gate and drain voltages. Circular gate transconductance and transconductance over drain current ratio comparisons with conventional SOI nMOSFET are performed, regarding the same effective channel length (L) and width (W). It can use circular gate transistors instead conventional SOI nMOSFET in order to improve the voltage gain of analog integrated circuits.

1. INTRODUCTION

The random errors of the fabrication process [1] and the devices geometrical forms [2] heavily affect the performance of analog integrated circuits. In order to verify the influence of other geometrical form than conventional in analog integrated circuits, this work is focusing in the circular gate transistor (CGT) (figure 1), where the internal contact can operate either as a drain or as a source. Besides, this structure is asymmetric because it presents different drain and source dimensions and the drain current is in the radius direction (all directions), in contrast of the conventional counterpart.

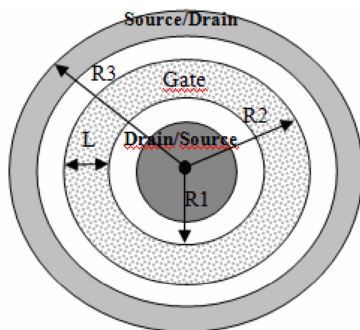

Figure 1 – Circular gate SOI nMOSFET structure, where the internal contact can be operating either as a drain.

In the figure 1, R1 is the internal radius that defines the channel beginnings, R2 is the external radius that defines the channel external edge, L is the channel length (=R2-R1) and R3 is the radius that defines the device external edge.

The geometrical factor (f_r) of GCT and conventional SOI nMOSFET is determined by equation (1) [3].

$$f_r = \left(\frac{W}{L}\right)_{Conventional} = \left[\frac{2\pi}{\ln\left(R2/R1\right)}\right]_{Circular} \quad (1)$$

In the equation (1), W is the channel width.

The references [4, 5] show that larger transconductance (g_m), transconductance over drain current ratio (g_m/I_{DS}) and Early voltage (V_{EA}) reach larger operational transconductance amplifiers (OTAs) open-loop voltage gain (A_{V0}) and unit voltage gain frequency (f_T). It is showed in the reference [6] that the CGT Early voltage with external drain configuration is larger than it is operating with internal drain and than conventional SOI nMOSFET. So, the focus of this work is to investigate the transconductance (g_m) and transconductance over drain current (g_m/I_{DS}) behavior in circular gate SOI nMOSFETs taking in account the drain/source asymmetric effects regarding experimental results. Comparisons between rectangular and circular gates SOI nMOSFETs are also performed, considering the same effective channel length and width.

2. EXPERIMENTAL RESULTS

The transistors used to perform the experimental measures were fabricated at IMEC, Belgium, and using 0.13 μm Partially-Depleted SOI CMOS technology. The technologic parameters of the SOI nMOSFETs are: t_{oxf}=2.5 nm (gate oxide thickness), t_{oxb}=400 nm (burred oxide thickness), t_{si}=100 nm (silicon thickness), N_A=5.5x10^{17} cm^{-3} (channel concentration), $N_{Drain/Source}$= 1x10^{20} cm^{-3} (Drain/Source concentration), L = 1 μm (channel length) and W = 100 μm (average channel

width). The calculated values for R1 and R2 are 15.5 µm and 16.5, respectively, in order to obtain W/L=100 [expression (4)]. The conventional transistor dimensions are L = 1 µm and W = 10 µm, resulting W/L=10.

In the figure 2 are presented the I_{DS}/W x V_{GT} experimental curves of CGT with both drain configurations (operating with internal and external drain) and conventional SOI nMOSFETs, where V_{GT} is equal to V_{GS}-V_{TH}, V_{GS} is the gate to source voltage and V_{TH} is the threshold voltage. The normalized drain current in relation of channel width and V_{GT} are used to implement this graphic in order to eliminate the channel widths and threshold voltages differences between CGT and conventional, respectively.

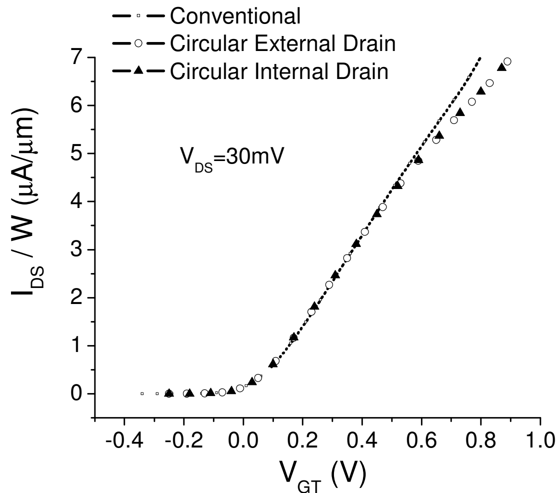

Figure 2 – Experimental results of circular gate devices and conventional SOI nMOSFET.

Observing the figure 2, it can see that the normalized drain current (I_{DS}/W) of CGT with internal drain configuration is higher than with external drain configuration and than conventional one. Besides, CGT I_{DS}/W with external drain configuration has practically the same than rectangular gate transistor.

Figure 3 presents the experimental transconductance curves as a function of V_{GT} for the CGT with both drain configurations and conventional SOI nMOSFETs.

Regarding the figure 3, it can verify that the transconductances of CGT with both drain configurations and conventional SOI nMOSFETs present practically the same behaviors for V_{GT} values bellow of the maximum transconductance ($V_{GT}\leq 0.25$ V) and they also have practically the same maximum transconductance (g_{mmax}). Besides, for V_{GT} values above of g_{mmax}, the CGT with both drain configurations presents smaller transconductance than conventional SOI nMOSFET. As the carriers mobility depend on the material crystallographic orientation, one hypothesis to understand this phenomenon (carriers mobility degradation in the CGT) is due to CGT carriers move in the radius directions (all directions) in channel, while they move in one unique direction in the conventional transistor. Three dimensional simulations have been performed with these transistors in order to confirm this affirmation.

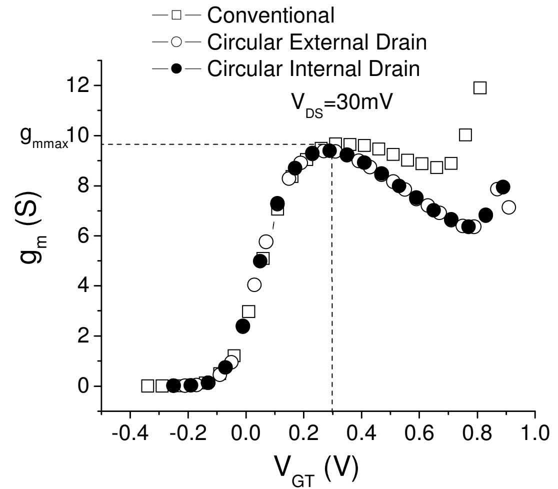

Figure 3 – Experimental transconductance curves of CGT for both configurations and conventional SOI nMOSFET.

In the figure 4 are showed $g_m/I_{DS}xV_{GT}$ experimental curves of CGT and conventional SOI nMOSFET.

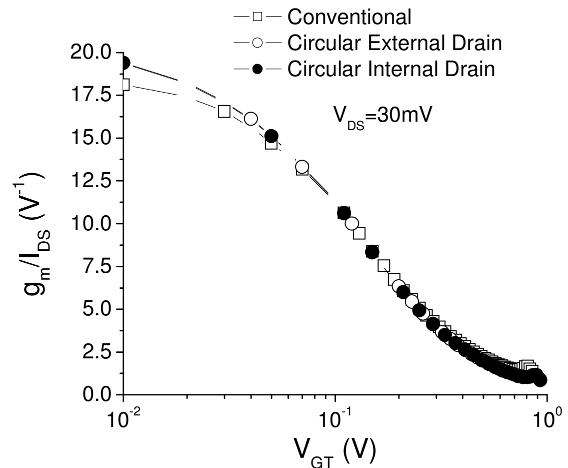

Figure 4 – Experimental $g_m/I_{DS}xV_{GT}$ curves for the circular gate transistor and conventional SOI nMOSFET.

Observing figure 4, it can note that CGT with both configurations and conventional g_m/I_{DS} are practically the same for V_{GT} higher than 0.1 V (moderate and strong inversion regions). And, regarding V_{GT} less than 0.1 V (weak inversion region), the CGT with internal drain configuration presents higher g_m/I_{DS} than conventional SOI nMOSFET due to it has higher transconductance in this region.

In the figure 5 are presented the transconductance over drain current ratio over DC drain current normalized as a function of channel width over length ratio curves [$g_m/I_{DS}xI_{DS}/(W/L)$] of the CGT with both drain configurations and conventional SOI nMOSFET. This graphic is an important merit figure in order to design

analog integrated circuits and presents an universal characteristic of all the transistors belonging to the same fabrication process [4, 5].

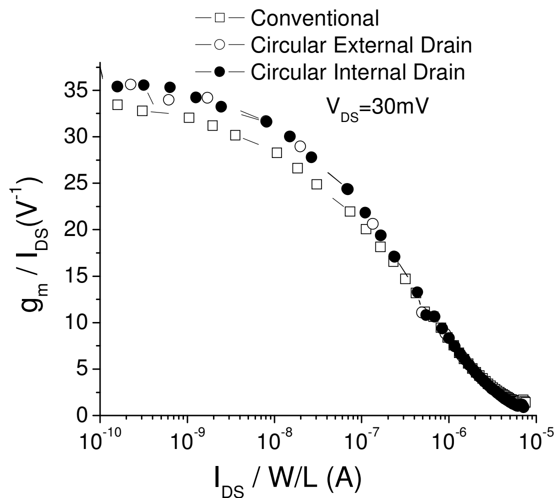

Figure 5 – CGT and conventional SOI nMOSFET $g_m/I_{DS}xI_{DS}/(W/L)$ experimental curves.

Note that in the figure 5, the g_m/I_{DS} of CGT with both drain configurations is higher than conventional SOI nMOSFET for $I_{DS}/(W/L)$ less than 0.3 A [weak inversion (18% maximum) and inferior half of moderate inversion regions] and it is practically the same in the strong inversion region.

3. CONCLUSIONS

This paper performs the behavior study of transconductance and transconductance over drain current ratio in circular gate SOI nMOSFET. For $V_{GT}\leq0.25$ V, the transconductances behaviors of CGT with both drain configurations and conventional SOI nMOSFETs is practically the same. Besides, they present practically the same g_{mmax} and the CGT transconductance has larger degradation than conventional transistor for $V_{GT}>0.25$, due to carriers mobility depend of the material crystallographic orientation and in the CGT the carriers move in the radius direction (all directions) in channel.

The g_m/I_{DS} of CGT with both drain configurations is higher (18% maximum) than conventional SOI nMOSFET in the weak inversion region and up to inferior half of moderate inversion regions, for $I_{DS}/(W/L)$ less than 0.3 A. Besides, it is practically the same in the strong inversion region. So, in order to improve the voltage gain (18%) of analog integrated circuits, operational transconductance amplifiers (OTAs) for example, where usually the differential pair is biased in weak or moderate inversion regions, it can use the CGT instead conventional SOI nMOSFET.

4. ACKNOWLEDGMENTS

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5. REFERENCES

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