COMPARISON OF THE DRAIN LEAKAGE CURRENT BETWEEN A CONVENTIONAL AND A DOUBLE GATE SOI nMOSFETs AT HIGH TEMPERATURES

Alfonso Braz Gutierrez and Marcello Bellodi

Centro Universitário da FEI
av. Humberto de Alencar Castelo Branco, 3972 - SBC - SP - Brazil - Zip Code 09850-901
alfonsobraz@yahoo.com.br

ABSTRACT

In this paper we present a comparison between the conventional and the Double Gate SOI nMOSFETs operating from room temperature up to 623K, where the drain leakage current behavior is analyzed and compared. In order to realize this work, two-dimensional numeric simulations were performed. It is observed that the leakage current composition changes as the channel length reduces and its intensity depends on the kind of device under evaluation.

1. INTRODUCTION

Since conventional CMOS structures are applied in integrated circuits, there is limitation of its uses in environments where temperatures are higher than 473K [1]. Pushed by the need of new challenges in more severe environments, it was created a new technology, the SOI MOSFET [2]. This technology presents some advantages when compared to the conventional CMOS [3,4].

Figure 1 shows the cross section view of both structures under evaluation in this work: the single gate and double gate SOI nMOSFETs.

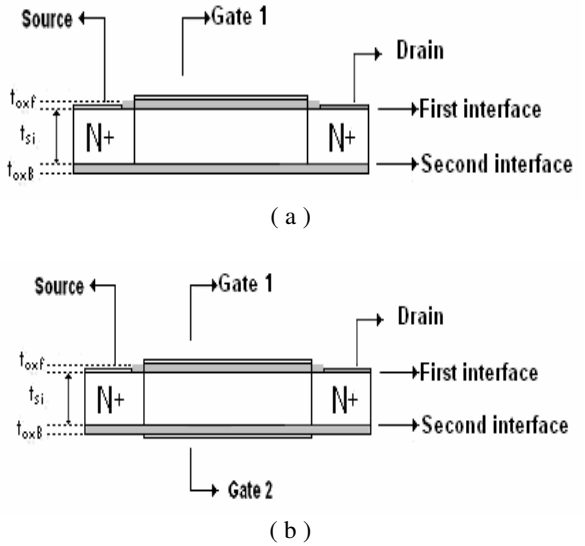

Figure-1: Cross section view of the (a) Single gate SOI nMOSFET (b) Double gate SOI nMOSFET.

2. DEVICE CHARACTERISTICS

The characteristics of the SOI nMOSFET transistors used were the gate oxide, buried oxide and silicon film thickness being t_{oxf} = 2.5nm, t_{oxB} = 2.5nm and t_{si} = 0,1µm, respectively. The channel length L used is from 0,5µm up to 10µm. The silicon doping used in all simulations were $N_a = 5.10^{17}cm^{-3}$ and $N_d = 1.20^{20}$ cm^{-3} for the *p* and *n* regions, respectively.

3. SIMULATIONS RESULTS

The numerical simulations were performed using the numerical simulator ATLAS [5] in order to evaluate the drain leakage behavior and its components in the conventional and the double gate SOI nMOSFETs operating since room temperatures up to 623K, where it was analyzed the leakage composition behavior (holes and electrons) as a function of the channel length for both structures operating at the same bias conditions.

Figure 2 shows a typical drain current I_{DS} versus the gate voltage V_{GS} curves for the conventional and double gate SOI nMOSFETs, operating at high temperatures.

From these results it is possible to notice that as the temperature increases, the drain current changes according to the temperature changes. Moreover, it was also observed that I_{DS} intensity, operating at same conditions, depends on the transistor layout.

To evaluate the drain leakage current as a function of the temperature it is necessary to obtain it from the I_{DS} versus V_{GS} curves, for both transistors operating at same bias conditions. Then, after doing an evaluation of these curves, it was concluded that the best bias condition to define the drain leakage current I_{Leak} is for V_{GS} = -1.0V, where the current is almost constant.

Figure 3 reports some results concerning I_{DLeak} as a function of temperature for the conventional and double gate SOI nMOSFETs operating at linear region i.e, for the drain voltage V_{DS} = 200mV. These results showed in this figure are for the channel length being L = 0,5µm and 10µm, respectively.

It is important to mention that when the drain voltage bias increases, I_{Leak} also increases, meaning that its intensity depends on the drain bias, for the devices operating at same temperature.

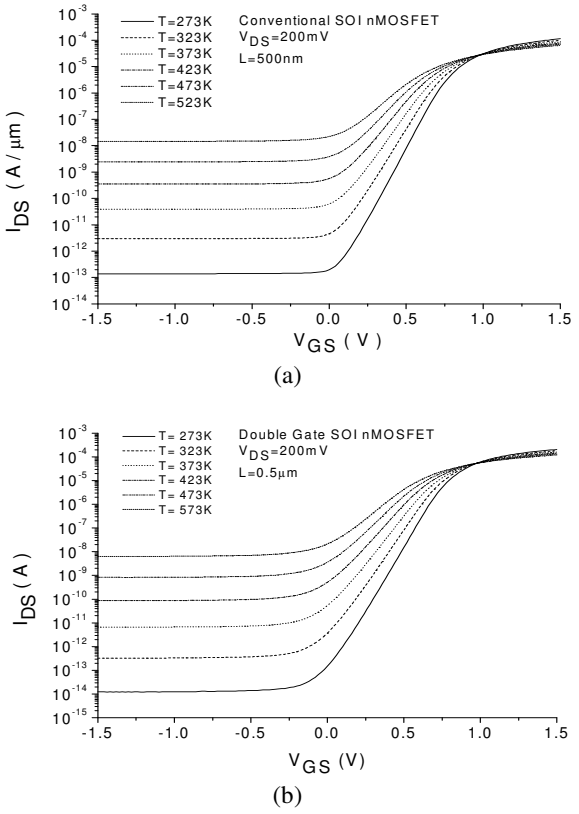

Figure 2: Typical drain current versus the gate voltage curves for the (a) conventional and (b) double gate SOI nMOSFETs, at high temperatures.

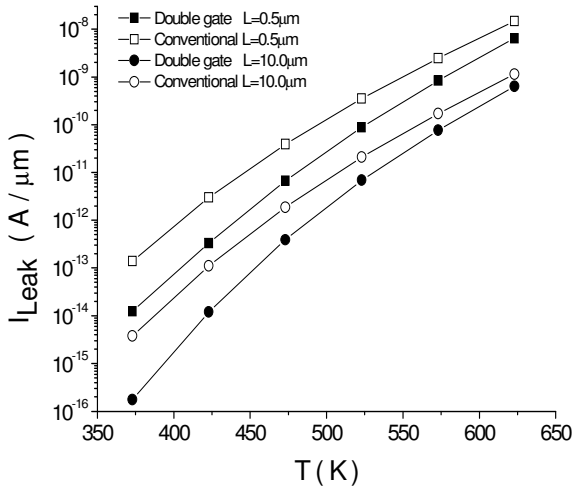

Figure 3: Drain leakage current behavior as a function of the temperature for L = 0,5µm and L = 10µm, for both SOI nMOSFETs structures.

From the results presented in figure 3, it is possible to notice that for the same device, I_{Leak} increases as the temperature rises. On the other hand, it can be seen that for the same temperature, I_{Leak} changes according to the device under analysis. This behavior is clearly observed in figure 4, where I_{Leak} is plotted as a function of the channel length L for both transistors operating at high temperatures.

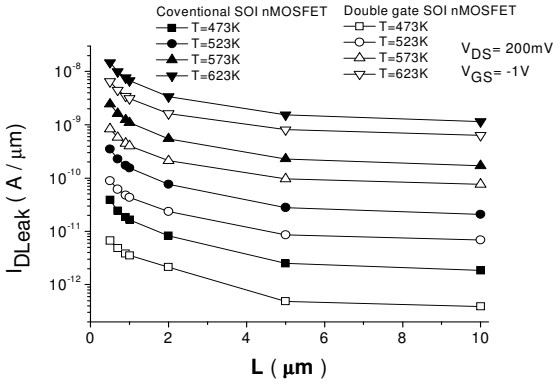

Figure 4: Comparison of I_{Leak} behavior as a function of the channel length L for both transistors operating at high temperatures.

From these results, it is possible to notice that as the channel length reduces, I_{Leak} increases for the same device operating at same conditions (temperature and bias). Besides, it is possible to observe that I_{Leak} in double gate SOI nMOSFET is lower when compared to the conventional device, independently of the temperature.

In order to understand this behavior, the total drain leakage current density J_{Leak} and its components (holes and electrons) were analyzed into the silicon film in both structures, as a function of the temperature and the channel length. This evaluation were done in the middle of the channel length as a function of the silicon film depth, when the devices are operating at the leakage region (V_{GS} = -1.0V).

Figure 5 (a) shows the schematics used to obtain the total drain leakage current density J_{Leak}, by using ATLAS, and its components as described in figure 5 (b).

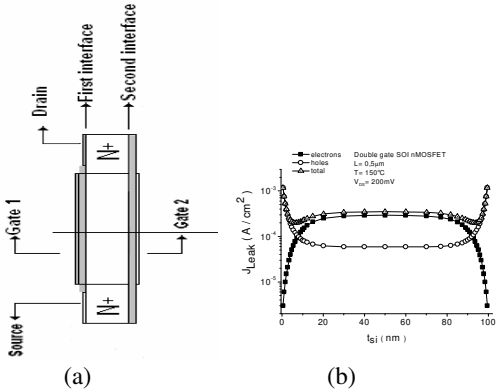

Figure 5: (a) Schematics to extract J_{Leak} and its components (b) Typical J_{Leak} composition as a function of the silicon film depth (t_{Si}).

Once defined the channel length where J_{Leak} is analyzed (L/2), bidimensional simulations were performed in order to extract the total drain leakage

current and its components (holes and electrons) in both transistors operating at same bias and temperatures.

Figures 6 and 7 shows some results of J_{Leak} behavior and its composition for conventional and double gate SOI nMOSFETs.

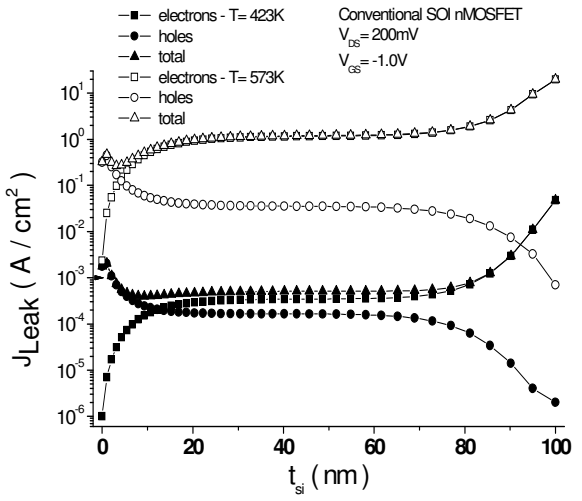

Figure 6: Results concerning to the total drain leakage current density behavior and its components (holes and electrons) for the conventional SOI nMOSFET at high temperatures.

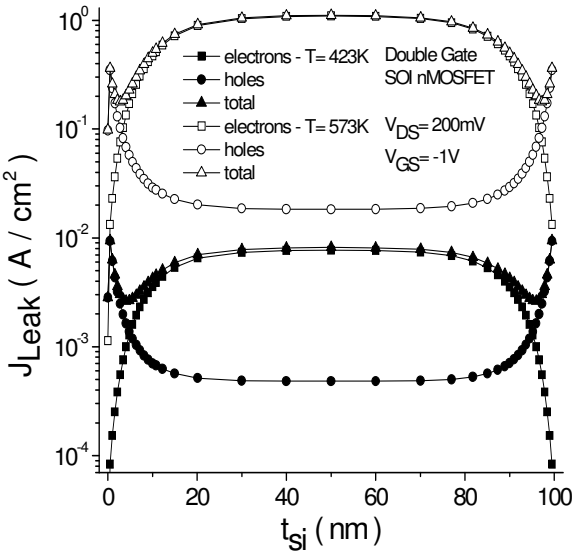

Figure 7: Some results for the double gate SOI nMOSFET related to J_{Leak} behavior and its components (holes and electrons) at high temperatures.

As shown in figures 6 and 7, it is possible to notice that J_{Leak} is composed by holes and electrons. But analyzing J_{Leak} in the conventional SOI nMOSFET it can be seen that the leakage current that flows around the gate oxide / silicon film interface (1st interface) is composed mainly by holes and the one that flows into the silicon film body is mainly given by electrons. Otherwise, in double gate devices (figure 7) similar behavior is also observed but since it has a second gate, J_{Leak} that flows around the silicon film / gate oxide interface (2nd interface) is majority composed by holes (similar to the one observed in the 1st interface).

It is worthwhile to mention that similar results are observed, in both SOI devices, as temperatures change. It can be seen with more details in figures 8 and 9, where some results are reported as a function of the temperature for conventional and double gate SOI nMOSFETs, respectively.

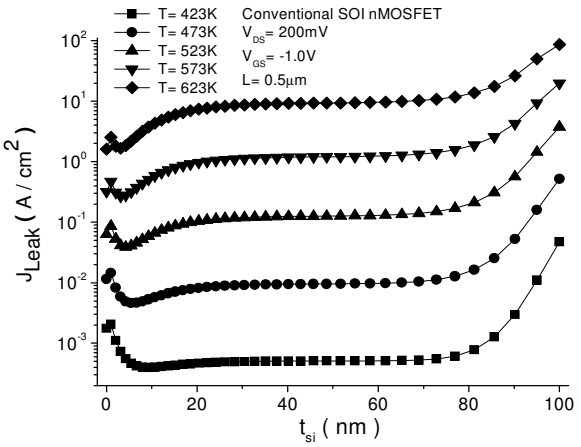

Figure 8: Total drain leakage current density for the conventional SOI nMOSFETs at high temperatures.

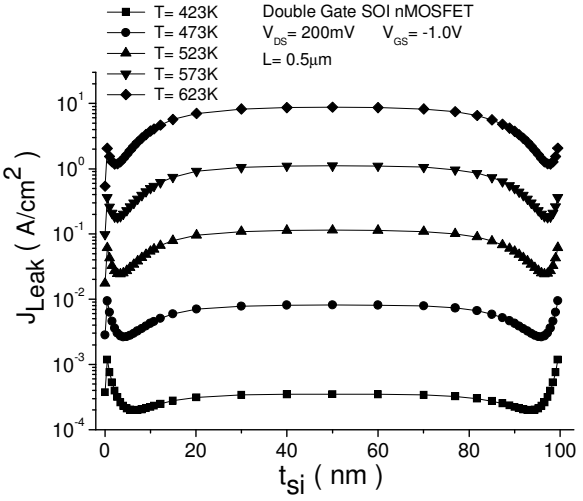

Figure 9: **T**otal drain leakage current density behavior for the double gate SOI nMOSFET operating at high temperatures.

Doing similar analysis for the double gate SOI nMOSFETs, as the temperature changes, the drain leakage current composition in 1st and 2nd interfaces and into the transistors body does not change but its intensity gets higher as the temperatures increases.

4. CONCLUSIONS

In this paper it is described the drain leakage current behavior in conventional and double gate SOI nMOSFETs operating since room temperature up to high temperatures, as a function of channel length changes. Results show that the drain leakage current increases as L reduces and it is composed mainly by electrons, which flows through the silicon film body. The minority component flows near the 1st and 2nd interfaces being composed mainly by holes. For conventional SOI nMOSFETs it flows around in the first interface; for double gate devices it flows in both interfaces.

Also it was noticed that I_{Dleak} is larger in conventional SOI nMOSFETs since the most part of I_{Dleak} flows through the silicon. In double gate devices, on the otherhand, I_{Leak} is divided between the interfaces and the silicon film body.

5. REFERENCES

[1] M. Youssef Hammad and Dieter K. Schroder, Analytical Modeling of the Partially-Depleted SOI MOSFET Life Fellow, IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 48, NO. 2, FEBRUARY 2001

[2] J. P. Colinge, Silicon-on-Insulator Technology: Materials to VLSI, 3rd Edition, Kluwer Acad. Pub., Massachussetts, 2004

[3] J.P. Colinge, Recent advances in SOI technology, In: Technical Digest of IEDM, pp. 817–820, 1994.

[3] Wei Ma and Savas Kaya, Impact of device physics on DG and SOI MOSFET linearity, Ohio University, Athens, OH 45701, USA, 15 March 2004

[4] ATLAS Device Simulation Framework, version 5.10.0.R, Silvaco International, 2005.

[5] Sorin Cristoloveanu, New physics mechanisms enabled by advanced SOI CMOS engineering. Electromagnetism and Photonics (UMR 5531), Institute of Microelectronics, 14 September 2004.