PLANK TRANSISTOR: A NEW GATE STRUCTURE TO REDUCE DIE AREA

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ABSTRACT

This paper performs a comparative study between the Multifingers, Waffle and the new gate structure called Plank transistor, considering die area and electric performance. The Microwind and L-Edit softwares used to implement the layouts and to generate the characteristics curves of these devices. It can use Plank transistor in the place of Multifingers and Waffle structures, in order to reduce die area, without degrading electric characteristics performance.

1. INTRODUCTION

The integrated circuits industry is always under strong pressure to follow the Moore's Law [1], where the number of transistors in the integrate circuit double each two years. This industry growth is directly proportional its capacity to reduce the transistor dimensions and to perform integration of a higher transistor number in an unique integrated circuit. Nowadays, MOSFET (Metal-Oxide-Semiconductor Field Effect Transistor) dimensions have been reduced and reaching nanometric scales, where it presents undesired parasitic effects, called short channel effects [drain induced barrier lowing (DIBL), substrate punchthrought, etc]. These effects have been identified as the main problem to follow Moore's Law. And another manner to increase transistors integration in an unique die is to implement new geometric forms or new transistors layouts, with smaller area than currents multifinger (figure 1) and waffle (figure 2) [2-9] structures. These structures share the drain and source contacts with more than one transistors. The multifinger and waffle layouts share the drain and source contacts with two gates and up to four transistors, respectively, to increase the circuit integration.

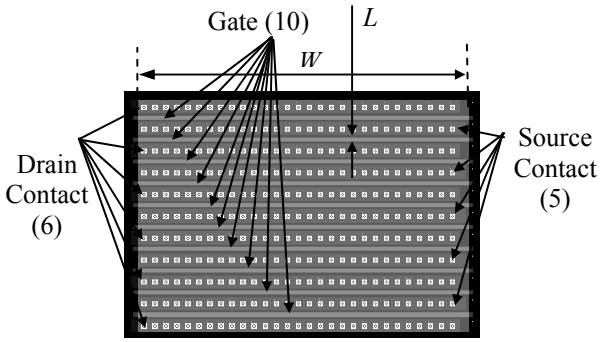

Figure 1 – Multifinger structure with ten (10) transistors in parallel with shared drain and source contacts.

Analysing figure 1, the multifinger transistor presents ten (10) transistors connected in parallel. Each transistor has a geometrical factor given by W/L, where W and L are channel width and length, respectively. The multifinger total geometrical factor is equal to $f_{rT} = [n*(W/L)]$, where n (= 10) is the number of transistors.

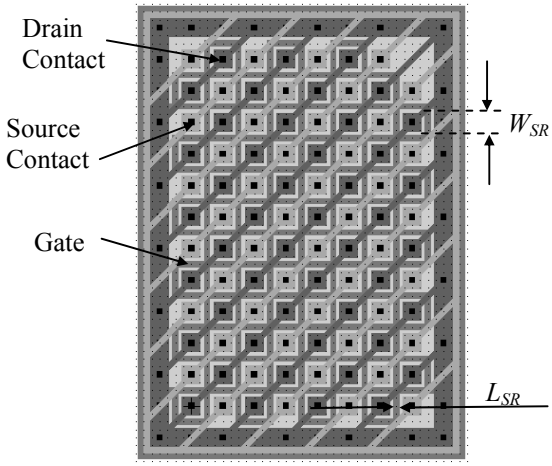

Figure 2 – Waffle transistor implemented with 47 transistors connected in parallel.

Observing figure 2, the Waffle transistor has forty seven (47) transistors connected in parallel. Each transistor (square ring) has a geometrical factor given by W_{TSR}/L_{SR}, where W_{TSR} (= $4.W_{SR}$) is the channel width and L_{SR} is the channel length and is equal to L_{min}. The Waffle total geometrical factor is equal to $f_{rTW} = [n*(W_{TSR}/L_{SR})]$, where n (= 47) is the number of transistors.

Before to present the Planck transistor, it will be presented the circular gate transistor structure (CGT) [4] (figure 3).

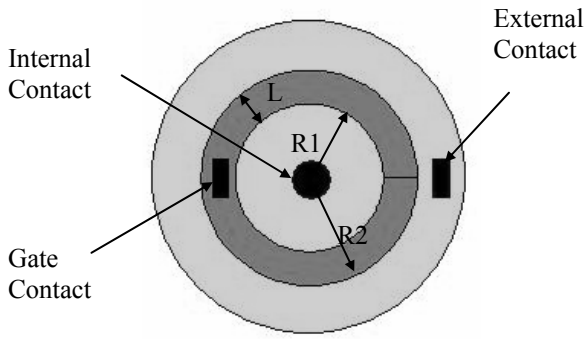

Figure 3 – Circular gate transistor (CGT).

In figure 3, R_1 and R_2 (= $R_1 + L$) are the internal and external radius, respectively and L is the channel length.

The conventional and CGT geometrical factor (f_r) for the same channel length [10], is given by equation (1):

$$f_r = \left(\frac{W}{L}\right)_{Conventional} = \left[\frac{2\pi}{\ln\left(\frac{R_2}{R_1}\right)}\right]_{CGT} \quad (1)$$

The Plank transistor (figure 4) is a combination or a mixed of multifinger and CGT, to increase the geometrical factor (f_r) and reduce die area of multifinger and Waffle structures, by adding a half of circular gate in each extremity of multifinger transistor. Note that this new transistor presents asymmetric drain and source characteristics, because the drain and source dimensions are different, as the CGT.

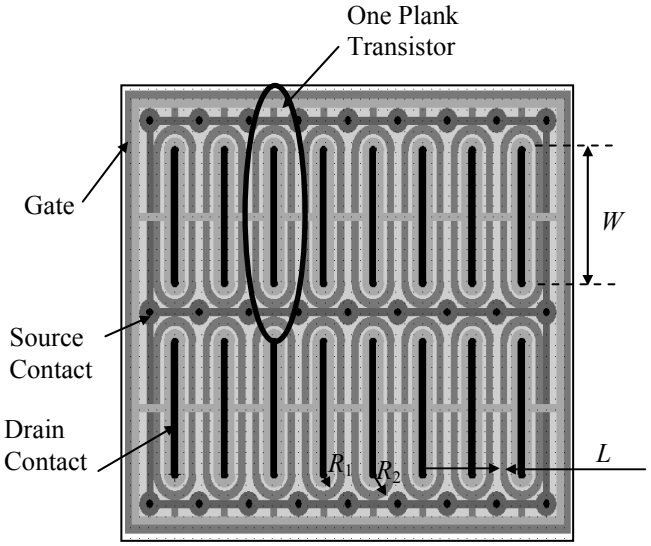

Figure 4 – Transistor implemented with sixteen (16) Plank transistors.

The Plank transistor geometrical factor (f_r), considering the same channel length (L), is given by equation (2):

$$f_r = \left(\frac{W}{L}\right)_{Mult.} + \left[\frac{2\pi}{\ln\left(\frac{R_2}{R_1}\right)}\right]_{CGT} \quad (2)$$

Note that Plank geometrical factor is composed of two components. The first one represents multifinger geometrical factor and the second one represents CGT geometrical factor.

2. AREA COMPARISON

To perform the area study comparison, it is implemented three (3) transistors with three (3) different layouts (Multifinger, Waffle and Plank structures). They are implemented by using Microwind software [11] and design rules used are given by the archive cmos0.8.rul (L_{min} = 0.8 μm). The total geometrical factor (f_{rT}) of each different structure is defined to be equal to 750, considering L_{min} of this technology. In case of multifinger transistor, it is implemented with ten (10) transistors in parallel with W = 60 μm and L = 0.8 μm, resulting an individual (W/L) = 75, for the Waffle structure, there are forty seven (47) square ring structures in parallel, with W_{TSQ} = 4*W_{SR} = 4*3.2 μm = 12.8 μm and L = 0.8 μm, resulting an individual (W/L) = 16 and for the Plank structures are necessary sixteen (16) structures in parallel, with W = 12.3 μm, L = 0.8 μm, R_1 = 0.8 μm and R_2 = 1.6 μm, resulting an individual (W/L) = 46.2. Table 1 summarizes the total W/L ratio, L, individual W/L and quantities of structures are necessary to implement a transistor with same W/L and L.

Table 1: Structure names, W/L, L and number of structures in order to implement transistors with total W/L equal to 750.

Structure Name	Total W/L	L	Individual W/L	Number of Individual Structure
Multifinger	750	0.8	75	10
Waffle	750	0.8	16	47
Plank	750	0.8	46 ☑	16

Table 2 presents the individual geometrical, total die area and the geometrical factor over total area ratio of each structure.

Table 2: Geometrical factor, total die area and the geometrical factor over total area ratio of each structure.

Transistor	$\frac{W}{L}$	$\frac{\frac{W}{L}}{Total\_Area}$	Total Area (μm^2)
Multifingers	75	0.20	2544
Waffle	16	0.15	2396
Plank	46	0.28 ☑	2086 ☑

Observing Table 2, Plank structure presents smaller total die area than Multifinger and Waffle transistors, around 18% and 13%, respectively, due to its higher geometrical factor over total area ratio.

3. SPICE SIMULATIONS

Spice simulations [11] were performed for different layouts and Multifinger, Waffle and Plank transistors electrical characteristics (I_{DS}xV_{GS} and I_{DS}xV_{DS}) are practically the same (5% maximum errors).

4. CONCLUSIONS

This paper performs a die area comparative study and an electrical performance analysis between Multifinger, Waffle and Plank transistors. For the same geometrical factor ($f_r = W/L$) and channel length (L), it is verified that Plank transistor presents smaller die area than Multifinger and Waffle structures, around 18% and 13%, respectively, due to its higher geometrical factor over total area ratio, without degrading electrical performance.

Because the die area is reduced, it turns out to be advantageous to replace multifinger and waffle transistors by the Plank transistor, mainly for analog integrated circuits and power transistors.

5. REFERENCES

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