MOS DEVICES TECHNOLOGY: FABRICATION AND CHARACTERIZATION

Jeferson André da Silva e Victor Sonnenberg

Faculdade de Tecnologia de São Paulo

ABSTRACT

In this paper we show the MOS devices fabrication on LSI Laboratory at USP in two wafers with the same process, except for the diffusion time that were 30 minutes (wafer 1) and 40 minutes (wafer 2).

MOS transistors, diodes and Van der Pauw (VDP) structures were electrically characterized. Drain-to-source current versus gate-to-source voltage ($I_{DS}xV_{GS}$) and drain-to-source current versus drain-to-source voltage ($I_{DS}xV_{DS}$) curves from the MOS transistor, diode current versus direct diode voltage (I_DxV_D) curves from diodes and sheet resistance versus current (Rsh x I) from VDP structures were extracted.

Comparing the results, wafer 1 showed better result, with 97% of these transistors and 90% of these diodes were considered good, while for the wafer 2 only 17% of these transistors and 30% of these diodes were considered good.

1. INTRODUCTION

MOS transistor technology is predominant in microprocessor fabrication due to its lower power, higher integration, simpler fabrication process (source and drain are equal) and lower cost when compared to bipolar transistor technology.

There are two ways of CMOS (complementy MOS) technology power consumption: static and dynamic power. Dynamic power occurs when both transistors (NMOS and PMOS) are conducting current due to the clock and the static power is due to the drain-to-source leakage current, normally by PN junction.

With the downscaling of dimensions, it is necessary to reduce the power voltage (V_{DD}) too. In this case the subthreshold slope and drain-to-source leakage current are very important to achieve low static power.

MOS transistor, diodes and VDP structure were fabricated with different diffusion process and their extracted electrical parameters were analyzed in this work with the goal of studying the diffusion process.

2. BASIC CONCEPTS

2.1. MOS Transistor

Figure 2.1 shows the N channel MOS transistor cross-section where there are two N+ diffusion regions called Source (S) and Drain (D), one P region called Bulk (B) and one Gate (G) composed by Metal-Oxide-Semiconductor (MOS) structure.

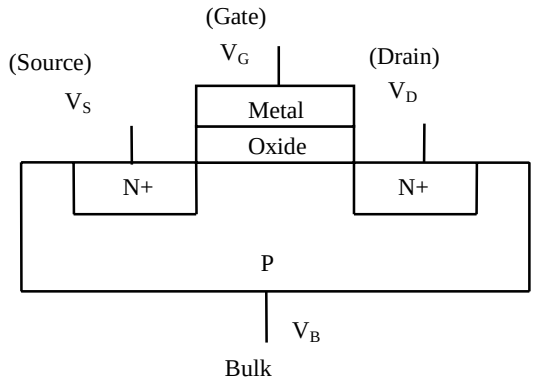

Figure 2.1 - N channel MOS transistor cross-section.

In the MOS transistor there is one gate voltage known as threshold voltage (Vth), which corresponds to the gate voltage where the channel is inverted (minority carriers are higher than majority ones). The Vth depends on substrate doping concentration, oxide thickness, metal work function, oxide quality, among other parameters.

When V_{GS} is smaller than Vth there is not any channel of minority carriers (inversion channel), therefore there is not current between source and drain (or it is negligible) and the transistor is off. For V_{GS} higher than Vth and V_{DS} below the difference between V_{GS} and Vth, there is a continuous channel of minority carriers connecting source and drain regions and the transistor is in triode condition. With V_{GS} higher than Vth but V_{DS} above the difference between V_{GS} and Vth, the channel is not continuous so it does not reach the drain anymore and the transistor is in saturation region. [3]

Figure 2.2 (a) shows the I_{DS} x V_{GS}, (b) the LOG I_{DS} x V_{GS} and (c) I_{DS} x V_{DS} curves of measured T1 NMOS transistor.

2.2. Diode

When a P type silicon gets in contact with an N type silicon there is a majority electron migration from N type silicon to P type silicon and majority holes migration from P type to N type; this majority carriers transport is called diffusion current. When the electrons get in contact with P type silicon, they recombine with holes or holes get in contact with N type silicon they recombine with electrons; therefore in PN junction there are fixes ions. These fixes ions get a region known as depletion region that gets an electrical field and generates a minority current in opposition to diffusion current called drift current.

When a positive voltage is applied to P type silicon, the diode conducts a strong majority current after the conduction voltage (V_{DO}).

When a negative voltage is applied, the current is of minority carriers and it tends to be very small (pA ideally).

Figure 2.3 shows the measured diode I_D x V_D curves in linear and log scales.

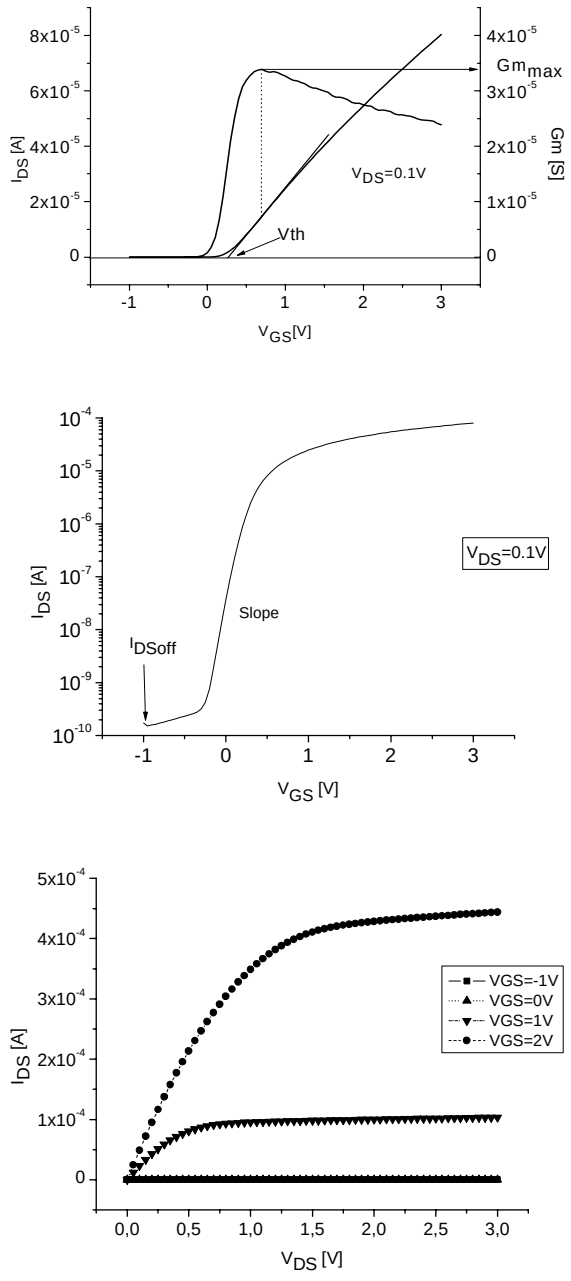

Figure 2.2 - (a) I_{DS} x V_{GS}, (b) LOG I_{DS} x V_{GS} and (c) I_{DS} x V_{DS} curves of measured T1 NMOS transistor.

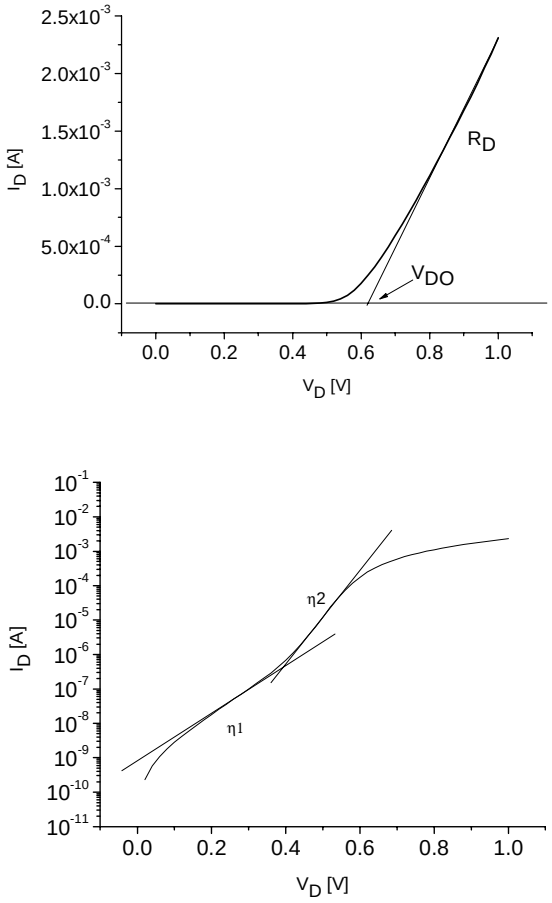

Figure 2.3 - Measured diode linear and log I_D x V_D curves

2.3. Van der Pauw Structures

The sheet resistance is the material resistivity by diffusion depth or film thickness and it is important to control the process. This parameter is measured using the VDP structure (figure 2.4). In this structure a current is applied between two adjacent terminals and the voltage is measured in two others terminals. The sheet resistance is then obtained using equation 1 [3].

$$R_{sh} = \frac{V_{43}}{I_{12}} \frac{\pi}{\ln 2} \qquad \text{equation 1}$$

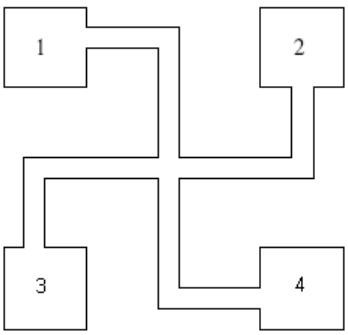

Figure 2.4: Van der Pauw structure.

3. FABRICATION PROCESS

The studied wafers (1 and 2) had the following processes: standard chemical cleaning to remove the contamination on surface wafers; growth of field oxide for the active regions isolation; lithograph to define the active regions; corrosion of the field oxide to open the active regions; removal of the photoresist; gate oxidation to form the gate capacitor MOS to the transistor; Si Poly deposition as metal to the MOS gate; lithograph and corrosion of the Si Poly; photoresist removal; phosphorus SOG deposition; phosphorus diffusion at 1150 ^{o}C with 30 min. for the wafer 1 and 40 min. for the wafer 2; SOG removal; Aluminum evaporation and corrosion for contacts definition; photo resister removal and back wafer metalization which will be bulk contact.

4. CHARACTERIZATION PROCEDURES

Each wafer has more than one hundred chips containing are several transistors, VDPs structures, diodes, alignment errors structures, Kelvin structures and other devices in each chip. Two MOS transistors, with different dimensions, called T1 with L=10 μm and W=50 μm and T9 with L=50 μm and W=10 μm, one diode and two VDP structures for N+ diffusion and N+ Si Poly were measured in 50 chips in each wafer.

From the transistors were extracted the following parameters: Threshold Voltage (Vth), maximum transconductance (Gm_{max}), maximum gain (βmax), carrier mobility independent of the field electric (μ), considering the oxide thickness (tox) 50 or 60 nm because this value is not precisely known, subthreshold slope (Slope) and leakage current (I_{DSoff}).

For diodes: reverse current at -5V (Ir), conduction voltage (V_{DO}), diode resistance (R_D) and ideality factor (η1 and η2 since there was not only one definition region).

From VDP structures were extracted the N+ diffusion and N+ Si Poly sheet resistances.

All parameters were extracted using equations 1 to 7 or graphically as presented in figures 2.2 and 2.3 with the methods shown in reference [3].

$$Gm = \left.\frac{\delta I_{DS}}{\delta V_{GS}}\right|_{V_{DS}=0.1} \qquad \text{equation 2}$$

$$\beta_{max} = \frac{Gm_{max}}{V_{DS}} \qquad \text{equation 3}$$

$$\mu = \frac{\beta_{max}\, tox}{\varepsilon ox}\frac{L}{W} \qquad \text{equation 4}$$

Where εox is the oxide permitivity.

$$Slope = \frac{\delta V_{GS}}{\delta LOG\, I_{DS}} \qquad \text{equation 5}$$

$$R_D = \frac{\delta V_D}{\delta I_D} \qquad \text{equation 6}$$

$$\eta = \frac{\delta V_D}{V_T\, \delta LnI_D} \qquad \text{equation 7}$$

Where V_T is the thermal voltage (25 mV at T=300 K)

5. RESULTS

After measuring the curves and extracting the parameters, the devices were classified as good, regular or bad. The good devices have similar characteristic curves between them and good parameters (for this educational process) in the same defined values range. The regular devices have some anomalies in the curve and some of their parameters are out of defined values range. When the devices simply do not work or do it badly, they were classified as bad.

The defined values range to classify the T1 transistor as good is Vth around 0.25V, subthreshold slope lower than 200mV/dec, I_{DSoff} lower than 10nA and good curve. T9 transistor is defined as good if it has Vth around 0.7V, subthreshold slope lower than 350mV/dec, I_{DSoff} lower than 1nA and the good curve.

In wafer 1 (30 min) all T1 transistors were considered good as defined before and T9 transistors had three considered regular, since they presented some anomalies in the curve but have good values. Therefore 97% of the measured transistors are good.

Tables 5.I and 5.II show the average of parameters extracted from T1 and T9 transistors from wafer 1.

Table 5.I: Average of parameters extracted from T1 wafer 1.

Wafer 1	V_T (V)	Gm_{max} (μA/V)	β_{max} (mA/V²)	μ(50nm) (cm²/Vs)	μ(60nm) (cm²/Vs)	Slope (mV/dec)	I_{Dsoff} (nA)
Good devices	0.24±0.06	34±2	0.34±0.02	858±129	1030±155	134±31	1.4±2.7

Table 5.II: Average of parameters extracted from T9 wafer 1.

Wafer 1	V_T (V)	Gm_{max} (μA/V)	β_{max} (μA/V²)	μ(50nm) (cm²/Vs)	μ(60nm) (cm²/Vs)	Slope (mV/dec)	I_{Dsoff} (nA)
Good devices	0.7±0.3	0.84±4	8.4±0.4	586±31	705±37	319±67	0.7±1
Regular devices	0.7±0.4	0.82±6	8.2±0.6	577±38	692±46	271±65	1±0.8

In wafer 2 (40 min) T1 transistors presented good results in only 5 devices on the right border, 4 considered bad and the others are considered regular. The T9 transistors have similar results but more devices are considered bad. Unfortunately only 17% of the measured transistors are considered good.

Tables 5.III and 5.IV show the average of parameters extracted from T1 and T9 transistors from wafer 2.

Table 5.III: Average of parameters extracted from T1 wafer 2.

Wafer 2	V_T (V)	Gm_{max} (μA/V)	β_{max} (mA/V²)	μ(50nm) (cm²/Vs)	μ(60nm) (cm²/Vs)	Slope (mV/dec)	I_{Dsoff} (nA)
Good devices	0.23±0.09	33±2	0.33±0.02	810±58	972±70	142±17	13±16
Regular devices	1.2±0.4	11±2	0.11±0.02	341±162	312±60	1608±409	287±217

Table 5.IV: Average of parameters extracted from T9 wafer 2.

Wafer 2	V_T (V)	Gm_{max} (μA/V)	β_{max} (μA/V²)	μ(50nm) (cm²/Vs)	μ(60nm) (cm²/Vs)	Slope (mV/dec)	I_{Dsoff} (nA)
Good devices	0.5±0.2	0.9±0.02	9±0,2	616±15	739±240	392±145	7.1±7.7
Regular devices	1.9±0.4	0.3±0.1	3±1	178±72	224±93	1581±563	11±13

The wafer 1 transistors are considered better than the wafer 2 ones, due to smaller I_{DSoff} and Slope.

For diodes, the criterion to consider them good is to have Ir (Vr=-5V) lower than 10nA, V_{DO} between 0.5 and 0.6 V an η below 1.8. In wafer 1, 90% of diodes are considered good, while in wafer 2 30% of diodes are considered good, 56% are regular and the others are bad.

Tables 5.V and 5.VI show the average of good and regular diode parameters extracted from wafers 1 and 2.

Table 5.V: Average of parameters extracted from diode wafer 1.

Wafer 1	Ir(Vr = -5V) (nA)	V_{DO} (V)	R_D (Ω)	η1	η2
Good devices	6.4±9.9	0.61±0.02	205±66	2.6±0.3	1.5±0.2
Regular devices	240±85	0.54±0.03	355±329	2.9±0.4	1.7±0.3

Table 5.VI: Average of parameters extracted from diode wafer 2.

Wafer 2	Ir(Vr = -5V) (nA)	V_{DO} (V)	R_D (Ω)	η1	η2
Good devices	30±19	0.5±0.1	768±296	3.2±0.2	1.69±0.06
Regular devices	268±905	0.56±0.03	757±223	3.6±0.5	2.2±0.3

The wafer 1 diodes are better than wafer 2 because they present smaller Ir (Vr=-5V), R_D and η. This result is likely to be related to the fact that with 30 min of the diffusion the PN junction is more abrupt than with 40 min [4].

N+ diffusion VDP structure presents a good uniformity and the average sheet resistance is around 13 Ω/□ and N+ Si Poly VDP structure presents average sheet resistance around 80Ω/□. These values are considered good for these parameters.

Table 5.VII shows the sheet resistance average for N+ diffusion and N+ Si Poly VDP structure extracted in both wafers.

Table 5.VII: Sheet resistance average for N+ diffusion and N+ Si Poly VDP structure extracted in both wafers.

	N+ diffusion (Ω/□)	N+ Si Poly (Ω/□)
Wafer 1	13.6±0.7	86±19
Wafer 2	13.1±0.6	80±06

6. CONCLUSION

Two wafers with different diffusion time were fabricated and characterized with success.

The wafer 1, with 30 min of the diffusion time, had 97% of the transistors and 90% of the diodes considered good. The wafer 2, with 40 min of the diffusion time, had 17% of the transistors and 30% of the diodes considered good.

Analyzing the results from the two wafers it is possible to see that the process with smaller diffusion time (waffer 1) is better, since it presents good diodes (PN junction) and because the transistors had smaller I_{DSoff} and better Slope.

ACKNOWLEDGMENTS

The authors would like to thank Prof. Luís da Silva Zambom for helping in the devices fabrication.

7. REFERENCES

[1]**http://www.pessoal.cefetpr.br/elisanm/index_arquivos/Fam_logicas.pdf**

[2]http://www.inf.pucrs.br/~petinf/homePage/publicacoes/documentos/artigos/yan.souza_sic_2007.pdf

[3] Martino, João A. Pavanello, Marcelo A. Verdonck, Patrick B. Caracterização Elétrica de Tecnologia e Dispositivos MOS, Editora Thomson.

[4] Callister, William D. Jr. Ciência e Engenharia de Materiais: Uma Introdução “quinta edição” editora LTC.