STUDY OF TRANSCONDUCTANCE FOR DOPED TRIPLE-GATE TRANSISTORS

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ABSTRACT

This work presents the study of the influence of some physical and constructive characteristics of triple-gate SOI-MOS devices on the transconductance. More specifically, the sidewall inclination angle caused by imperfections in process technology and the doping level influences are analyzed through three-dimensional numeric simulation. The current values obtained from simulation are normalized by the total gate width and the transconductance is obtained from the derivative of the normalized drain current. The maximum transconductance showed to be highly dependent on the device cross-section shape. Better transconductances are obtained for devices with larger top-gates.

1. INTRODUCTION

Silicon-on-Insulator (SOI) has been an alternative technology to planar MOSFETs transistors, since the first SOI transistor was introduced in 1964, fabricated on Silicon-on-Sapphire (SOS). SOI technology has achieved excellent results, allowing the scaling down of structures bellow 40nm, with less significant short-channel effects than planar transistors [1, 2, 3, 4].

With the first dual gate transistor developed in 1989, an even better control of the channel charges allowed smaller short channel effects (SCE), better sub-threshold slope (S) and improved transconductance (g_m) [5, 6]. The experience with dual-gate transistors leaded researchers to develop other multiple-gate devices, as triple-gate, gate-all-around and FinFETs [1, 2, 3, 4].

Triple-gate devices may be constructed with two vertical and one horizontal gate. Due to today limitations in process technology, some variations along the transistor side-wall are experienced and, as a consequence, what should be a rectangular cross-section becomes a trapezoidal cross-section, as showed in Fig. 1. Works regarding the influence of side-wall angle (θ) on some electrical parameters have already been published [7] and some current models have also been proposed [8, 9]. This paper presents the study of how transconductance may change for nMOSFETs with doping concentrations of 1×10^{17}, 5×10^{17}, $1\times10^{18}cm^{-3}$ as a consequence of the variation in the side-wall inclination angle caused by imperfections in process technology that can imply in larger or smaller top channel width.

This work is based on three-dimensional device simulation implemented in Atlas [10].

The cross-section of the studied device, with some dimensions, is represented in Fig. 1. The gate-oxide and gate thickness are respectively 2nm and 4nm, the channel length is 200nm, the base channel width (W_{base}) and channel height are fixed in 50nm and the top channel width (W_{top}) ranges from 30 to 70nm, in order to vary the side-wall inclination angle.

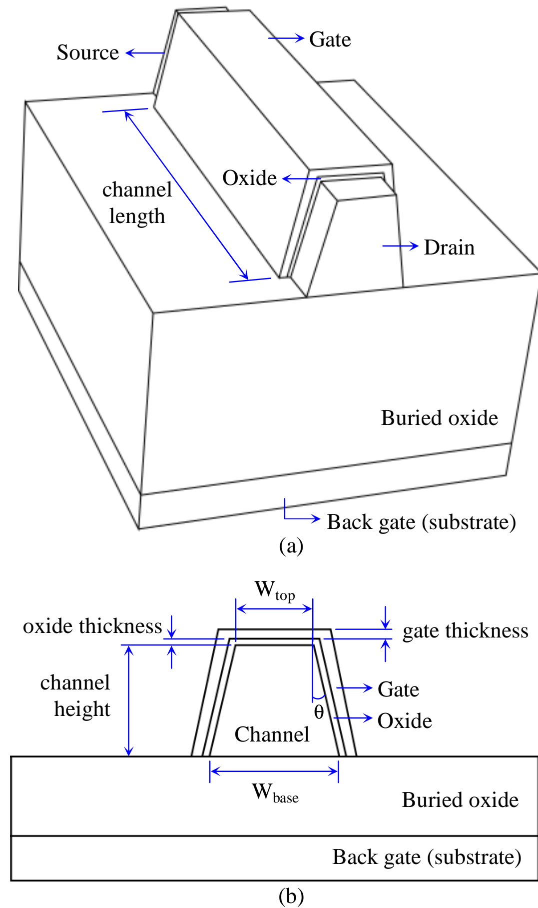


Fig. 1. simulated device description: three-dimensional view (a) cross-section view at middle of channel length (b).

According to previous studies on triple gate FinFETs, up to four different threshold voltages might exist as a result of the three gates plus the back gate [11], but for

lower doping levels, as those of the studied transistors, only one threshold voltage is observed.

2. THREE-DIMENSIONAL SIMULATION

The device transconductance (g_m) analysis has been conducted based on Atlas three-dimensional simulation results. Simulations have been performed using Shirahata (SHI) and Klaassen (KLA) mobility models, a drain bias (V_{DS}) of 0.05 V and base width (W_{base}) of 50nm. The first simulation has the doping level (Na) of $1x10^{17}cm^{-3}$, the second $5x10^{17}cm^{-3}$, and the third $1x10^{18}cm^{-3}$.

For a better analysis of values obtained from simulations on different device geometries, the $I_{DS}xV_{GS}$ curves were normalized dividing the current data by the gate cross-section perimeters W_{total} (see equation (1)).

$$W_{total} = W_{top} + \sqrt{10^{-14} + \left(50\times10^{-9} - W_{top}\right)^2} \quad (1)$$

W_{total} is given in meters.

This normalization procedure is justified by the fact that the current is concentrated near the gate oxide interface, forming a thin layer bellow each gate. Dividing the total current density in the channel by the width of the three gates will result in current density per length, allowing comparisons between the different transistor geometries. Fig. 2 shows the current density at the cross-section for a transistor with doping concentration of $Na=1x10^{18}cm^{-3}$, W_{top}=30nm and gate polarized with 0.76V, that corresponds to maximum transconductance ($g_{m.max}$). As a consequence, all curves resulting from $I_{DS}xV_{GS}$ are also normalized.

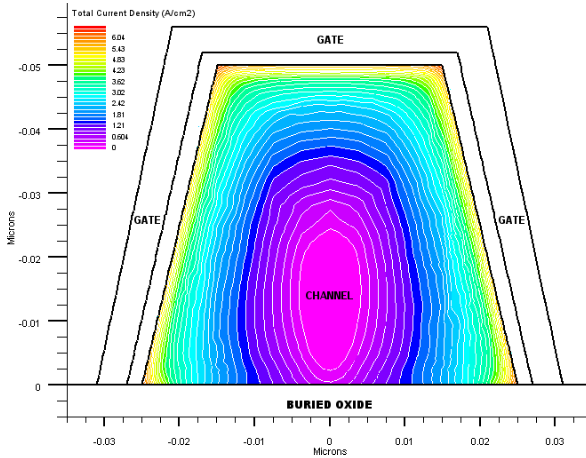


Fig. 2. current density for $Na=1x10^{18}cm^{-3}$, W_{top}=30nm and V_{GS}=0.76V in cross-section view at middle of channel length. The red color near the gates represents higher current concentrations and the pink color at center represents lower current concentrations.

Fig. 3 presents the $I_{DS}xV_{GS}$ curves normalized for each W_{top} values and doping levels of $1x10^{17}cm^{-3}$, $5x10^{17}cm^{-3}$ and $1x10^{18}cm^{-3}$.

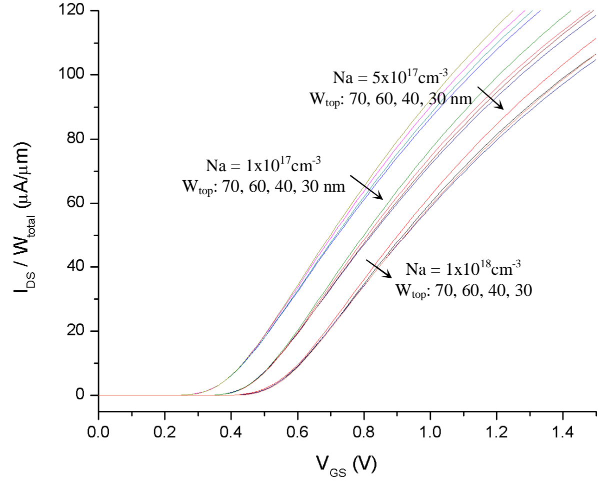
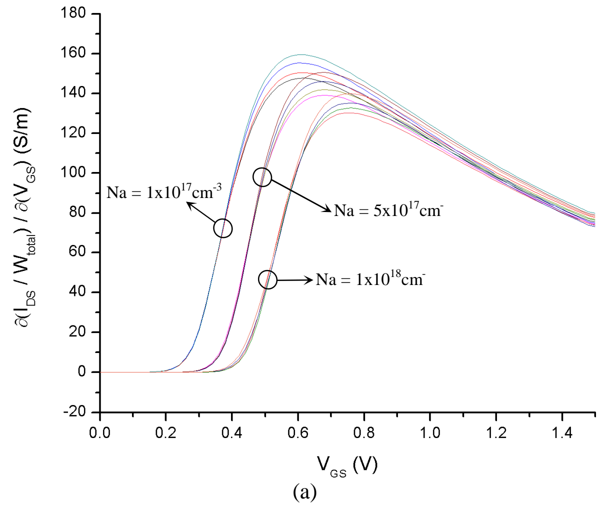


Fig. 3. $I_{DS}xV_{GS}$ curves for all three doping levels studied.

Departing from these curves, g_m can be easily obtained using the first order derivative of drain current (I_{DS}) *versus* gate voltage (V_{GS}) [12] as described in equation (2).

$$g_m = \frac{\partial I_{DS}}{\partial V_{GS}} \quad (2)$$

All g_m curves have been plotted together in Fig. 4 (a) and (b). The value of maximum transconductance increases for higher values of top width (W_{top}). It is also observed that the increase in doping level implies in a decrease of maximum transconductance $g_{m.max}$ values (see Tab. 1).



(a)

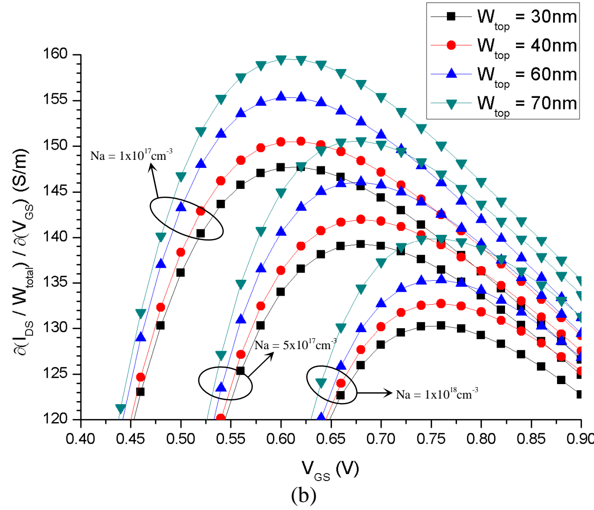


Fig. 4. transconductance curves: (a) and (b).

The observed change in transconductance is due to the change in the coupling between the gate planes, the back gate and the inversion charge. When W_{top} is smaller than W_{base}, back gate will have a greater influence on the channel and consequently top gate control will be reduced, especially on top corners, decreasing $g_{m.max}$. On the opposite situation, where W_{top} is larger than W_{base}, back gate influence will reduce and top gate will raise its control of the channel, raising $g_{m.max}$, especially on top corners.

As maximum transconductance values are in $g_{m.max}$ per length, the increase on $g_{m.max}$ is the result of changing only the channel geometry, independet of gate width influence. Fig. 5 presents $g_{m.max}$ *versus* W_{top} curves for each doping level allowing the transconductance visualization as a function of side-wall angle and its behavior on different doping levels. Notice in the graph the raise on $g_{m.max}$ values for larger top gate widths (larger W_{top}). This variation is greater with lower doping levels than higher ones.

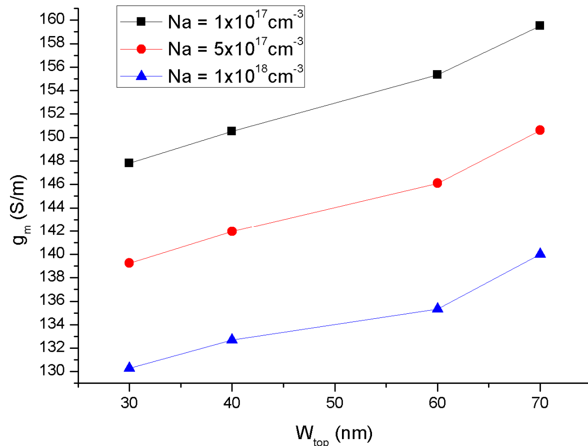


Fig. 5. comparative curves of $g_{m.max}$ *versus* W_{top} for each doping level.

Tab. 1. $g_{m.max}$ values.

doping level (cm^{-3})	W_{top} (nm)	$g_{m.max}$ (S/m)
	30	147.8
$1x10^{17}$	40	150.5
	60	155.3
	70	159.5
	30	139.2
$5x10^{17}$	40	142.0
	60	146.1
	70	150.6
	30	130.3
$1x10^{18}$	40	132.7
	60	135.3
	70	140.0

3. CONCLUSION

This study presented the effects in transconductance caused by variations in the side-wall inclination angles due to limitations in process technology for triple-gate MOS transistors that can imply in larger or smaller top channel width.

The maximum transconductance is increased as the top width of the transistors is increased, because the coupling between the gate and the controlled inversion charge is increased, and lower doped levels have higher maximum transconductance. For smaller top gate widths the channel is more exposed to the influence of the back gate, and the maximum transconductance decreases.

4. REFERENCES

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