MODELING SET PULSE BROADENING IN INTEGRATED CIRCUITS

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ABSTRACT

The propagation of single event transients (SET) in logic gate chains is studied and modeled. SET propagation in logic chains may induce significant broadening or attenuation of the transient pulse width. It is shown that the chain design (propagation delay of high to low and low to high transitions) has a major impact on the transient pulse broadening or attenuation. For the first time a suitable model for SET broadening is provided.

1. INTRODUCTION

The constant advance in the integrated circuits manufacturing process has continuously reduced the transistors geometry and the supply voltages levels. In high density circuits operating at low voltages, the electric charge present at the nodes that store information is becoming steadily small. Unfortunately, a straight consequence is the increase of the circuit vulnerability to radiation, since energized particles that were depositing charges once considered negligible are now producing errors [1, 2].

When a radioactive particle hits a sensitive region in a semiconductor device, it deposits charge that may cause a transient pulse which can change the logical state of the circuit. In a node, this transient pulse is called single event transient (SET). If a particle strike occurs at the internal node of a combinational circuit, the transient pulse may be propagated and be caught by a memory element, producing a transient error (soft error), changing the computing results [3].

If the so-called logical, temporal or electrical masking occurs, the transient pulse will not to be caught by a memory element [4]. Logical masking occurs if a particle hits a node of the circuit whose output gate does not depend on the incorrect input, because its output is determined solely by its other inputs. Temporal masking occurs if a SET propagates through the circuit to a memory element, but a clock transition does not occur during the duration of the SET. Electrical masking occurs if the transient pulse generated by the particle is being attenuated while it's propagating through the logical gates and it is filtered before reaching a memory element.

In recent works, it was experimentally observed that a SET may also suffer a broadening as it propagates through logical chain [5]. Pulse broadening would lead to increased probability of a SET leading to an error. Larger SET pulse width has a higher probability of being capture by a storage element. Experiments in [5] showed that SET may suffer a significant broadening as well as a significant degradation, depending on the topology and loading of the logic chain. However, previous works have not presented the reason of this behavior and a suitable model for that. A model to suitable describe the observed behavior can help designers to predict the broadening and degradation of SETs in integrated circuits and to develop more suitable fault tolerance techniques for that.

In this work, we analyze the behavior of the transient propagations presented in [5, 7] by using Hspice electrical simulations. The goal is to explain the reasons for the occurrence of this behavior and to present an extension of the model considered in [6] to adequately represent this effect. It is an analytical model that can be easily applied in a soft errors analysis tool.

2. RELATED WORK

In [5, 7], experimental studies and characterization of SET propagation in chains of inverters were performed. Two different CMOS technologies were used: a 0.25 µm Bulk CMOS technology and a SOI CMOS 0.13 µm technology.

Two chains of inverters were designed and fabricated for performing the experimental work. The first chain was called Load1, and presents a chain of inverters with fanout 1 at each circuit node. The second chain was called Load3, and presents a chain of invertors in which the odd nodes of this chain are fanout 3 and the even nodes are fanout 1.

In these experiments, SETs have been injected through Laser pulses. The SETs have been injected at four distinct positions in the chain of inverters, as shown in figure 1.

The experimental results showed a behavior that should be reviewed and investigated further, as it was observed at the output node of the chain of inverters that the duration of the transient pulse for each position of the laser strike strongly depends on the struck node and circuit topology.

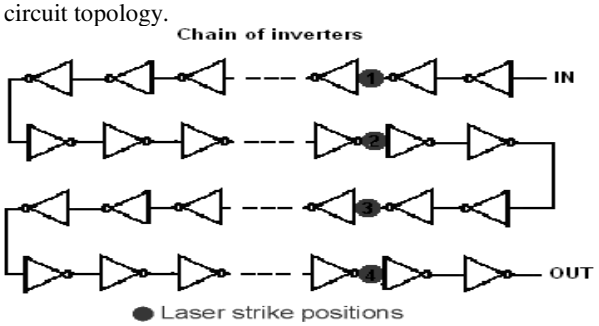

Fig. 1 – Chain of inverters showing the Laser pulse strike positions

In this experiment, it was found that if the laser strikes at a node close to the input node of the chain of inverters, the duration of the SET appearing at the output node is broadened, if compared to the SET injected at other positions. But this phenomenon occurs only if the input of the Load3 chain is kept at the logical value '0', i.e., ground. If the input of the chain of inverters is kept at the logical value '1', i.e., VDD, the transient pulse injected into the circuit has its amplitude and duration degraded. However, the reasons for the observation of such behavior were not explained in that work, and a suitable analysis and model is lacking in the literature. In the next section, we will analyze this behavior by means of electrical simulations, intending to present a suitable model for that.

3. SET PROPAGATION ANALYSIS

In this paper, a SET is defined as a particle strike induced voltage change that changes the node voltage by at least $V_{DD}/2$. The duration of the transient pulse at node *n* (τ_n) is the time during which the voltage change is greater than $V_{DD}/2$ [3]. The propagation delay of the logical gate (*tp*) is evaluated by applying an ideal pulse (high-low or low-high) at the input of the gate. The propagation delay is defined as tp_{LH} for an output transition from logical "0" (low) to a logical "1" (high), while tp_{HL} refers to high to low output transition.

At the circuit level, the charge deposition mechanism can be modeled by a double exponential current pulse at the particle strike site [4]:

$$I_P(t) = I_0 \left(e^{-t/\tau_\alpha} - e^{-t/\tau_\beta}\right) \qquad (1)$$

where I_0 is approximately the maximum charge collection current, τ_α is the collection time constant of the junction and τ_β is the time constant for initially establishing the ion track.

In order to analyze and model the pulse propagation behaviors described in section II, electrical simulations were performed for the 0.25 µm Bulk technology, using Hspice. Two distinct chains of inverters were simulated, as shown in Figure 2. The first chain of inverters is called "Load1". In this chain all nodes have fan-out equal to 1. The second chain of inverters is called "Load3". All odd nodes of the chain have fan-out equal to 3, while all even nodes of the chain have fan-out equal to 1.

The transistors sizes used in the electrical simulations are shown in the Table 1. The first column of Table 1 shows the name used to identify each inverter chain through this work. The second column shows the type of chain used in the simulation, and the third column shows the channel width of the NMOS transistors. The NMOS transistor channel width (W) varies from 0.3 µm to 1.8 µm, and the PMOS channel width is always twice the NMOS channel width. In all cases, the NMOS and PMOS channel length (L) is 0.25 µm. The supply voltage used for the 0.25 µm Bulk technology was 1.8V.

Table 2 shows the values used for the parameters of the double exponential used for charge injection at the electrical simulation level. The parameters I_0, τ_α and τ_β shown in the table refer to simulations performed for both 1→0 and 0→1 transitions.

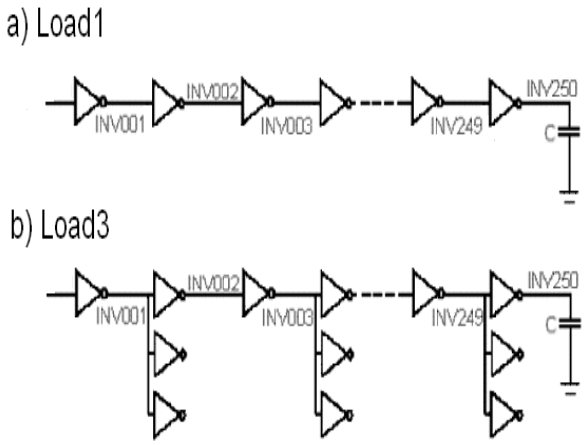

Fig. 2 – Schematic description of the chain of inverters with (a) a standard design, or (b) with every other inverter triplicate to simulate the load of more complex designs

Table 1 – Inverters chains in 0.25 µm Bulk Technology.

Inverter Chains	Load	NMOS width
Chain1	Load 1	0.3 µm
Chain2	Load 1	0.6 µm
Chain3	Load 1	1.8 µm
Chain1-L3	Load 3	0.3 µm
Chain2-L3	Load 3	0.6 µm
Chain3-L3	Load 3	1.8 µm

Table 2 – Parameters of the double exponential used for charge injection at the electrical simulation level

Inverter Chains	I_0	τ_α	τ_β
Chain1	190µA	10ps	360ps
Chain2	380µA	10ps	560ps
Chain3	890µA	10ps	2000ps
Chain1-L3	190µA	10ps	360ps
Chain2-L3	380µA	10ps	560ps
Chain3-L3	890µA	10ps	2000ps

Table 3 presents the results obtained when a transient pulse 1→0 → 1 is injected at the first node, labeled 'INV001' (fig. 2), for the Load1 chain input fixed at logical "0" (ground). We observed that the SET broadening effect did not occur for any of the three chains, regardless of the sizing of the transistors (transistors sizes for chain1, chain2 and chain3 are shown in Table 2). The same behavior is observed if a transition pulse 0→1→0 is injected at the 'INV001' node, with the input of the Load1 circuit fixed at logical "1" (VDD).

Table 3 – Load1 circuit with input at logical "0", τ_n is the transient pulse duration and NOT delay is the delay of the inverters.

	Chain1	**Chain2**	**Chain3**
Node	**τ_n (ns)**	**τ_n (ns)**	**τ_n (ns)**
INV001	0,63	0,73	1,72
INV002	0,65	0,76	1,77
INV067	0,68	0,78	1,81
INV068	0,65	0,77	1,80
INV129	0,68	0,78	1,81
INV130	0,65	0,77	1,80
INV249	0,68	0,78	1,81
INV250	0,65	0,77	1,80
	Delay	**Delay**	**Delay**
***tp_{LH}* (ps)**	86,20	82,60	78,90
***tp_{HL}* (ps)**	70,90	72,10	71,30
Δtp (ps)	15,30	10,50	7,60

Table 4 presents the results obtained if a transient pulse 1→0→1 is injected at the 'INV001' node of the Load3 circuit with its input fixed at logical "0" (ground). It can be seen that the SET broadening effect occurs for all three cases. As shown in Figure 2, the Load3 circuit has two types of nodes: the nodes with fan-out1 and the nodes with fan-out 3. Because of this there is a significant discrepancy between the propagation delays at the different nodes (odd or even), as shown in table 4. The table is divided into three parts. The first part shows the duration of the transient pulse (τ_n) at node *n*, at the specified nodes for the three different chains, where it is possible to verify the existence of broadening in the transient pulse through the chain of inverters. The second part shows the propagation delays of the logical gates for the even nodes and the third part shows the propagation delays of the logical gates for the odd nodes.

Table 5 presents the results obtained if a transient pulse 0→1→0 is injected at the 'INV001' node of the Load3 chain with its input fixed at logical "1" (V_{DD}). It can be seen that the duration of the transient pulse is degraded as it is propagated through the chain, in agreement with the experimental results reported in [5, 7].

Table 4 – Transient pulse 1→0→1 injected at the 'INV001' node with Load3

	Chain1-L3	**Chain2-L3**	**Chain3-L3**
Node	**τ_n (ns)**	**τ_n (ns)**	**τ_n (ns)**
INV001	0,72	0,83	1,95
INV002	0,73	0,84	1,96
INV003	0,77	0,88	2,00
INV004	0,75	0,87	1,99
INV067	1,28	1,33	2,43
INV068	1,27	1,32	2,42
INV128	1,75	1,74	2,79
INV129	1,79	1,76	2,81
INV249	2,76	2,59	3,57
INV250	2,74	2,58	3,56
	Even Node	**Even Node**	**Even Node**
***tp_{LH}* (ps)**	86,20	82,60	78,90
***tp_{HL}* (ps)**	70,90	72,10	71,30
Δtp (ps)	15,30	10,50	7,60
	Odd Node	**Odd Node**	**Odd Node**
***tp_{LH}* (ps)**	129,95	126,28	122,32
***tp_{HL}* (ps)**	101,13	104,46	104,68
Δtp (ps)	28,82	21,82	17,64

Table 5 – Transient pulse 0→1→0 injected at the 'INV001' node with Load3

	Chain1-L3	**Chain2-L3**	**Chain3-L3**
Nodo	**τ_n (ns)**	**τ_n (ns)**	**τ_n (ns)**
INV001	0,37	0,41	1,21
INV002	0,43	0,46	1,30
INV003	0,39	0,43	1,28
INV004	0,41	0,45	1,29
INV017	0,18	0,30	1,20
INV018	0,19	0,31	1,21
INV019	0,08	0,27	1,18
INV020	-	0,28	1,19
INV131	-	-	0,46
INV250	-	-	-

4. THE PROPOSED MODEL FOR SET PULSE BROADENING

The model presented in this section is an extension of the model proposed in [6] adjusting it by the obtained Hspice circuit-level simulation results, described in section III. The technology model uses MOSIS 0.25 μm Bulk chain technology from [8].

The model is divided into four regions, according to the relationship between τn (duration of the input pulse to the n-th stage) and the gate delay *tp*. Where *tp* value will be equal to the tp_{HL} value when the pulse generated at the input node of the logical gate be a transition 0→1→0, otherwise, the *tp* value will be equal to the tp_{LH} value.

First let one consider Δt for 1→0→1, defined as:

$$\Delta t = tp_{HL} - tp_{LH} \qquad (2)$$

and Δt 0→1→0, defined as:

$$\Delta t = tp_{LH} - tp_{HL} \qquad (3)$$

The first model region represents the situation where the transient pulse is filtered out. The model calculates the duration of the transient pulse below or above $V_{DD}/2$, according to the transition. It was made chain of inverters gates and NAND simulations, with different geometry. It was observed that the ratio τn/tp, where τn is the duration of the pulse in the nth stage, it has to be at least τn k times larger in order to propagate to the next stage. For transients inputs with minors tp times of the length so

k*τn, the output voltage changes less than $V_{DD}/2$, that is, the transient pulse is not propagated to (n+1 stage)th. Thus, the model for this region is:

$$\text{if } (\tau_n < k*tp) \text{ then } \tau_{n+1} = 0 \quad (4)$$

Where τ_n is the input transient pulse duration to the nth stage and k = 1.1.

The second region represents the situation where the transient pulse is not degraded and may have its duration broadened through the chain of logical gates of the combinational circuit. This occurs when the input pulse has duration (τ_n) greater than (k+3) times tp. In this case the degradation of the input pulse is negligible. Hence, for modeling purposes no pulse degradation is assumed to occur in this region:

$$\text{if } (\tau_n > (k+3)*tp) \text{ then } \tau_{n+1} = \tau_n + \Delta t \quad (5)$$

The third and fourth regions model the situation in which the pulse is propagated but degraded in amplitude and duration or may have its duration broadened. It is found that the pulse degrades faster in the last stages before being filtered out. Hence, it is appropriate to model pulse attenuation into two regions, with different equations modeling the degradation in each one of these two regions. The model for the third region, obtained by curve fitting, is:

$$\text{if } ((k+1)*tp < \tau_n < (k+3)*tp)$$
$$\text{then } \tau_{n+1} = (\tau_n^2 - tp^2)/\tau_n + \Delta t \quad (6)$$

In the last stages before being filtered out, the pulse duration (tn) decreases or duration broadened, the pulse degrades faster compared to the pulse decreasing in the early stages, and the model for the third region loses its validity to these pulses that are being almost filtered out. The model for the fourth region is obtained:

$$\text{For } (k*tp < \tau_n < (k+1)*tp)$$
$$\text{then } \tau_{n+1} = (k+1)*tp(1 - e^{(k-(\tau_n/tp))}) + \Delta t \quad (7)$$

The model was validated by comparing the results obtained using equations presented in the section III with Hspice level circuit simulation in 0.25 µm Bulk technology node. Several simulations are performed and some results are presented in tables 6 and 7, for Load3 circuit and an one-bit adder circuit, respectively. These tables compare Hspice simulation results with model prediction, as given by equations (4) to (7). Good agreement between circuit simulation and analytical model is found.

Table 6 – SET with T_n (in ns) at Load3 circuit "0" input state.

Chain1-L3	**Inv002**	**Inv068**	**Inv128**	**Inv250**
Hspice	0,73	1,27	1,75	2,74
Model	0,72	1,20	1,66	2,68
Chain2-L3	**Inv002**	**Inv068**	**Inv128**	**Inv250**
Hspice	0,84	1,32	1,74	2,58
Model	0,83	1,25	1,65	2,42
Chain3-L3	**Inv002**	**Inv068**	**Inv128**	**Inv250**
Hspice	1,95	2,42	2,79	3,56
Model	1,91	2,33	2,62	3,40

Table 7 – SET with T_n (in ps) at a one-bit adder.

Simulation-1	**Inv1**	**Nand9**	**Nand4**	**Nand7**	**S**
Hspice	737,91	801,97	823,78	799,60	794,44
Model	737,91	803,45	823,79	794,72	793,46
Simulation-2	**Inv1**	**Nand9**	**Nand4**	**Nand7**	**S**
Hspice	737,91	801,97	800,50	772,44	766,30
Model	737,91	803,45	800,11	771,44	766,30

5. CONCLUSIONS

The broadening of single event transients, as they propagate through the logic gates, is analyzed. To prevent the effect of broadening of SETs in combinatorial circuits the logic gates should be designed to present balanced high to low and low to high propagation delays, since SET broadening may lead to increased soft error rates. A simple model for single event transient propagation is proposed. It is shown that transient propagation can be properly modeled by considering the gate propagation delays and a constant k, which depends on the technology of interest. The model is suitable for automated evaluation of the sensitivity of digital circuits to transient faults and radiation hardening.

6. REFERENCES

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