DESIGN OF A CMOS TEMPERATURE SENSOR USING THE ACM MODEL

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ABSTRACT

A new design approach for CMOS temperature sensors is presented. It uses the Advanced Compact MOSFET (ACM) model equations to establish the transistors inversion levels and obtain transducer's output expression. The technique was used to revise a previous design, showing good accuracy with the original purpose. The design was implemented in a conventional 0.5 μm CMOS process, occupying a silicon area of 0.035 mm². Results show an average responsivity of about -8.5 mV/ºC, a resolution of 0.004 ºC and power consumption of 10 μW. Discussions on the sensor's performance are also presented.

1. INTRODUCTION

Temperature sensors are such important devices, since they are used in many applications like: body temperature measurement, heat controllers, systems performance monitoring, etc. A CMOS temperature sensor (known as proportional-to-absolute-temperature, or PTAT circuit) can be built of MOS transistors operating at weak inversion level, as shown by Vittoz and Fellrath [1]. The CMOS designs have shown to be well suitable for low power operation [2], and they can also be integrated with many other digital stuffs, including memories and data processors, as well as wireless transmission circuits for remote operation (smart sensors) [3].

A good example of a temperature sensor circuit is presented by Ohzone et al [4], which achieves low supply voltage dependence and high responsivity. Just like many other circuits, this one comprises transistors biased at different operating points. Most designs are based directly on strong or weak inversion operation model equations, which requires careful biasing (mostly, the setting of a precise gate overdrive voltage). To avoid this threatment, we may design our circuit using a transistor model valid for any inversion level (also called "universal" model), such as the Advanced Compact MOSFET (*ACM*) model [5]. This technique has been already used on the design of amplifiers, for example [6]. This model is also useful for determining the transistors inversion levels and check if they are biased for correct operation of the sensor.

This paper proposes a temperature sensor design methodology based on the ACM model equations [5,6]. This methodology was used to revise a previous constructed sensor circuit [7], and has shown great accuracy with the original design. It is shown with this method how the responsivity is affected by the use of different topologies proposed by Ohzone [4]. The temperature sensor circuit was implemented on a conventional 0.5 microns CMOS process, and it was obtained an average responsivity of -8.5 mV/ºC, with a power consumption of 10 μW and 0.035 mm² of silicon area.

2. DESIGN EQUATIONS

To simplify our design, we have collected a few equations from the ACM Model. Let's introduce them:

$$\alpha = \sqrt{i_f + 1} - 2 + \ln(\sqrt{i_f + 1} - 1) \qquad (1.a)$$

$$\beta = \sqrt{i_r + 1} - 2 + \ln(\sqrt{i_r + 1} - 1) \qquad (1.b)$$

$$V_P = |V_{SB}| + \phi_t \alpha \qquad (2.a)$$

$$V_P = |V_{DB}| + \phi_t \beta \qquad (2.b)$$

$$V_P = \frac{|V_{GB}| - |V_{TO}|}{n} \qquad (3)$$

$$(i_f - i_r) = \frac{I_D}{I_{SQ} S} \qquad (4)$$

I_D is the drain current;
I_{SQ} is the sheet normalization current ($I_{SQ}=0.5n\mu_n C_{ox}\phi_t^2$);
n is the slope factor;
ϕ_t is the thermal voltage ($\phi_t=kT/q$);
V_{TO} is the threshold voltage;
V_P is the "pinch-off" voltage;
S is the transistor aspect ratio ($S=W/L$);
i_f and ir are the forward and reverse invertion levels;
and V_{DB}, V_{GB} and V_{SB} are the drain-bulk, gate-bulk and source-bulk voltages, respectively.

For design purposes, n was considered constant and equal to 1.4, although it varies slightly with V_{GB}. The

extraction of n's and I_{SQ}'s real value is demonstrated by Ana et al [8].

3. CIRCUIT ANALYSIS

The architecture we have chosen to make our project is shown in figure 1.

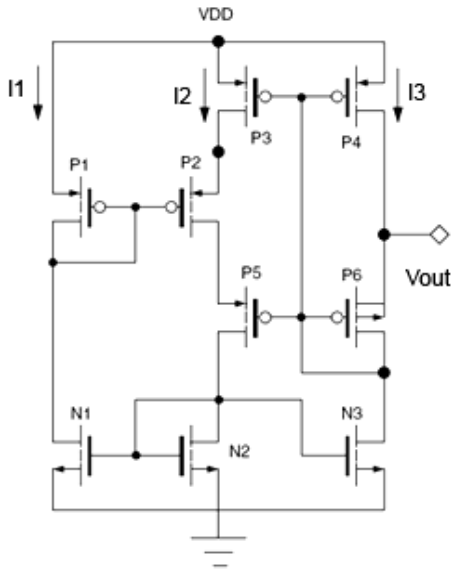

Fig 1. Schematic of the proposed circuit [7].

P1 and P2 are the sensing elements, and must be designed to operate at weak inversion level. Since both gate-bulk voltages are equal, we have that $V_{P1}=V_{P2}$ and

$$|V_{SB2}| = V_{P2} - \phi_t\alpha_2 = \phi_t(\alpha_1 - \alpha_2) \quad (5)$$

The same is valid for P3 and P4 ($V_{P3}=V_{P4}$), and since $|V_{SB2}|=|V_{DB3}|$, we obtain:

$$V_{P3} = |V_{SB2}| + \phi_t\beta_3 = \phi_t(\alpha_1 - \alpha_2 + \beta_3) = \phi_t\alpha_3 \quad (6)$$

$$V_O = V_{DD} - |V_{DB4}| = V_{DD} - V_{P4} + \phi_t\beta_4$$
$$= V_{DD} - \frac{kT}{q}(\alpha_1 - \alpha_2 + \beta_3 - \beta_4) \quad (7)$$

Particularly, P4 is designed to operate at saturation, and so i_{r4} approaches zero. If this statement is true, β_4 tends to infinity, which is undesirable. Equation 7 is then rewritten as function of α_6. From this point, we may consider one of the two cases discussed next:

3.1 Bulk of P6 connected to VDD (body effect)

If this is the case, then $\alpha_6=\beta_4$ and the output becomes:

$$V_O = V_{DD} - \frac{kT}{q}(\alpha_1 - \alpha_2 + \beta_3 - \alpha_6) \quad (8)$$

3.2 Bulk of P6 connected to Source (no body effect)

If this topology is used, then we have that:

$$\phi_t(\alpha_6 - \beta_4) = |V_{DB4}|\left(1 - \frac{1}{n}\right) \quad (9)$$

$$V_O = V_{DD} - n\frac{kT}{q}(\alpha_1 - \alpha_2 + \beta_3 - \alpha_6) \quad (10)$$

One can see that the second topology improves the responsivity a little bit, just as stated by Ohzone et al [4]. For this reason, we have chosen P-channel MOSFETs as the sensing elements, allowing the implementation of this circuit on a conventional CMOS process [7].

The coefficients α's and β's of the output equation (10) can be calculated directly from the design parameters, which are: the drain current (I_D) and the aspect ratio (S) of the transistors. The same I_D can be considered for the whole circuit if we chose a current mirror to match this configuration properly.

At saturation (P1, P2 and P6), $i_r=0$ and then α_1, α_2 and α_6 are found from eq. (4) and (1.a). β_3 is found from the equations (6), (4) and (1). Although we have considered β_4 as infinity, its real value is calculated from the eq. (9). The next session reports the implementation and the simulation results.

4. IMPLEMENTATION AND RESULTS

The temperature sensor described was designed and prototyped on a AMIS 0.5 μm process. Table I shows the values of Width and Length of the transistors utilized on the circuit, and their calculated values of i_f, i_r, α and β. The scale factor is 1μm.

TABLE I. Description of the used transistors.

Transistor	S	i_f	i_r	α	β
P1	45/0.6	0.5624	-	-2.137	-
P2	360/0.6	0.0689	-	-4.351	-
P3	4/25	3649	3391	62.5	60.288
P4	4/350	3610	-	62.174	-36.14
P5	120/1	0.155	-	-3.519	-
P6	400/1	0.550	-	-2.161	-

N1, N2 and N3: three matrices of a 8x4 series-parallel NMOS association, with W=1.2μm and L=1.2μm each one, totalizing 96 MOSFETs.

Figure 2 shows the measured voltage as function of the temperature for both, the theoretical project and the post-layout simulation. V_{TS} is the output voltage. One can observe that the sensor has a linear temperature coefficient between the range of -80ºC and 90ºC, where the slope is nearly constant. The calculated responsivity of the sensor using equation (10) is -7.6 mV/ºC, while the BSIM3v3 model simulations have shown about -8.0 mV/ºC. During the layout stage, the current mirrors were

split into series-parallel associations of MOS transistors (as described in Table I) and it achieved a responsivity of -8.9 mV/ºC. This technique has shown to improve the output conductance characteristics of the transistors [9].

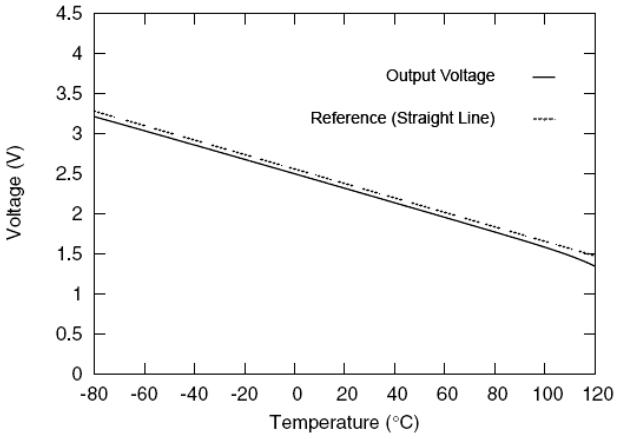

Fig 2. Output Voltage as a function of the Temperature

In order to estimate the accuracy of this circuit, we have provided some Monte Carlo analysis, simulating variations on transistor's dimensions over a gaussian distribution with 3σ equal to 0.18 um (which is 30% of the minimum length allowed for that technology). Figure 3 reports the performances obtained. Mismatch of the current mirrors were also considered, although they have been compensated on the layout disposal.

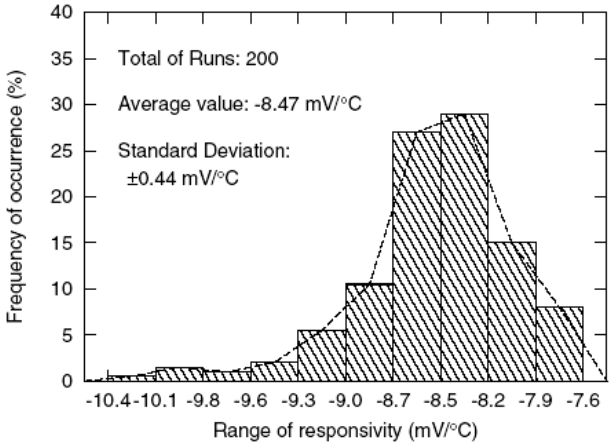

Fig 3. Histogram of Responsivity affected by variations on transistors sizes, using Monte Carlo Analysis

Besides, simulations to show the infuence of others process parameters variations were done using the corner models provided by the foundry for that technology (as can be seen in Figure 4). The results show that this circuit has a strong dependency on the process parameters, also affecting responsivity, but it can be mitigated by a carefully layout design. We can expect a reduction on the measurement range for the Fast-NMOS Fast-PMOS corner (Worst Power case), although it can be compensated by adjusting the power supply voltage.

The influence of the power supply VDD over the responsitivity is shown in Figure 5. It can be observed that the circuit has a safe range of operation from about 10% of it's nominal supply voltage value (5V ± 0.5V), with the possibility of operation at higher voltages. The simulated PSRR at low frequencies is 0.43 dB.

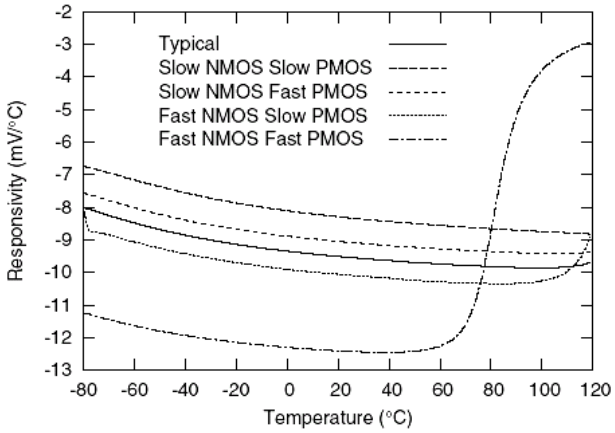

Fig 4. Responsivity for Typical and Corner Cases

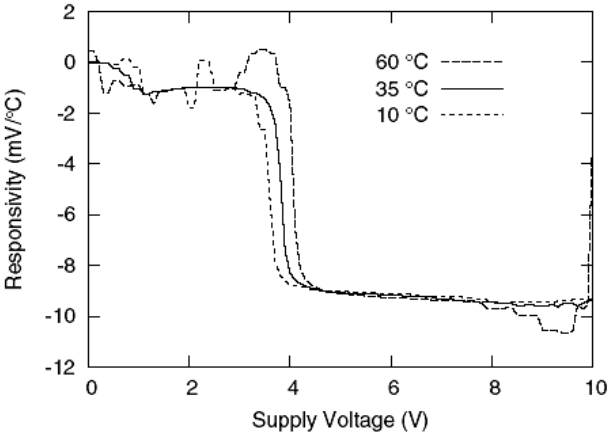

Fig 5. Influence of VDD over the Responsivity

Finally, the resolution of the sensor was observed with noise habilitated simulations, where at low frequencies the Flicker Noise is more relevant than Thermal Noise, and it was obtained a value of 0.004 ºC for the minimum perceived temperature variation at nominal conditions (resolution). Figure 6 shows the final layout, which occupies a 0.035 mm² silicon area. Table II shows a summary of the sensor characteristics, and Table III, a comparison between the different mentioned temperature sensors.

TABLE II. Summary of the sensor characteristics

Responsivity	-8.92 mV/ºC
Resolution	0.004ºC
Output DC Value	2.18 V
Maximum error	1.65% for -30º~80º range 3.74% for -80º~90º range
Supply Voltage (V_{DD})	5.0 ± 0.5 V
Supply Current (I_{DD})	2.1 µA
Power Consumption	≈ 10 µW
PSRR (at low freq.)	0.43 dB
Technology used	*AMIS 0.5 microns*
Silicon die area	0.035mm^2

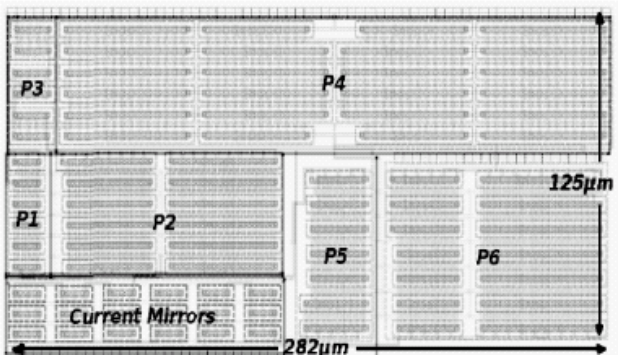

Fig 6. Layout of the implemented sensor

TABLE III. Temperature Sensors comparison

Sensor	Resp. (mV/ºC)	Power (µW)	Technology (µm)	Area (mm^2)
This Paper	-8.92	10	0.5	0.035
Ohzone [4]	5.1	200	1.2	0.18
Rossi [2]	-1.7	0.15	0.8	0.098

The area is about one fifth of the circuit of Ohzone et al [4], mainly due to the technology scaling. The differences between those temperature sensors are due to the distinct choices of the circuit configuration and CMOS process utilized, which becomes a trade-off between power consumption, temperature performance and silicon area.

5. CONCLUSION

We have proposed here a CMOS temperature sensor design methodology based on the ACM Model equations. This approach was used to revise a previous design, and showed good accuracy with the original purpose. Two topologies were discussed using this model, meaning on the choice of the better one. The circuit was implementable on a conventional CMOS process, and it's characteristics include low-power consumption (about 10µW), an average responsivity of -8.5mV/ºC, and its occupies a total silicon area of 0.035mm².

6. REFERENCES

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