Modeling the Impact of NBTI on the Reliability of Arithmetic Circuits

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ABSTRACT

Negative Bias Temperature Instability (NBTI) has become one of the major concerns in the reliability of CMOS circuits in nanoscale designs. However, a few studies of this effect in complex circuits have been done so far. With the goal to demonstrate the impact of this effect in these circuits it will be presented in this paper a comparison of three different full-adders topologies. Since NBTI is an aging effect that causes an increase on the threshold voltage average and standard deviation, it affects the lifetime performance of the cell and its reliability; therefore we will focus in comparing the delays of full-adder topologies.

1. INTRODUCTION

With the recent aggressive scaling of transistors and the increase of operation frequency of digital circuits, NBTI became a major concern in CMOS circuit reliability. Although NBTI is a frequency independent effect [1], it increases the V_t mean and standard deviation as [2] what leads to an increase of the worst case gate delay, highly reducing the maximum operation frequency.

NBTI effect occurs more significantly on PMOS transistors. It is caused by the broke of $Si-H$ bonds in transistors $Si-SiO_2$ interface, and then H diffuses continually generating traps during the stress period. This is related to a negative gate bias, because of the electric field, temperature and holes. If no negative gate bias is applied, a recovery period may take place, when the holes disappear and no more interface traps are generated. Moreover the H diffuses back annealing the broken $Si-H$, so the NBTI degradation recovers [3, 4]. Therefore this aging effect is frequency independent but is duty cycle dependent [1].

In this paper we intend to demonstrate the importance of considering aging effects during the design of digital circuit topologies. Hence we will present a comparison of the NAND-FA, XOR-FA and Mirror topologies considering V_t process variation, NBTI average and standard deviation. The focus of this comparison will be the worst case pathway delay with the 1-bit full-adders cells rippled to form an 8-bit adder (Fig. 1.). For this work we used the Monte Carlo Analysis simulating on HSPICE from Synopsys. Once NBTI is a duty cycle dependent effect and full-adders are complex circuits, their transistors will not stay with the same gate bias all along, so there is a necessity to predict the probability for each transistor to be stressed.

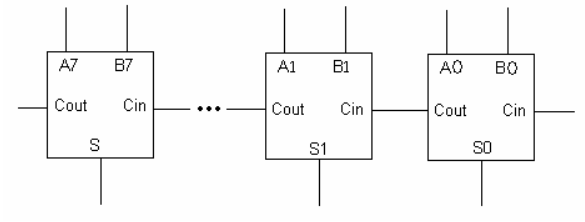

Fig. 1. 8-bit rippled full-adder.

In section 2 we present a statistical model of NBTI effect in threshold voltage of the PMOS transistors considering duty cycle input. Section 3 presents the circuit, the topologies used, the output analyzed and the method to estimate the NBTI stress probability for each transistor. Sections 4 and 5 present, respectively, the simulation results and the conclusion.

2. MODEL

The threshold voltage increase due NBTI is caused by the H diffusion that generates traps (N_{it}). From [1] a static equation is:

$$\Delta V_t = \frac{q \cdot N_{it}}{C_{ox}}, \text{ where } C_{ox} = \frac{\varepsilon_{ox}}{T_{ox}} \quad (1)$$

And N_{it} depends on time as follows:

$$N_{it} = \left(K^2 \cdot t^{1/2} + c^{1/2n} \right)^{2n} \quad (2)$$

Where c is N_{it} at the starting point, n depends of the technology, process and is experimentally determined. In our work we used $n = 1/6$ that refers to the H_2 diffusion [4], considering the H diffusion instead of H_2, $n = 0.25$. K is linearly proportional to the hole density and exponentially dependent on temperature and the electric field.

It is a good approach to set the dynamic ΔV_t equation proportional to the static one with the proportionality constant being dependent of the duty cycle as follows:

$$\Delta V_{t_{dinamic}} = \alpha \cdot \Delta V_{t_{static}} \quad (3)$$

For this paper, α were obtained from [1].

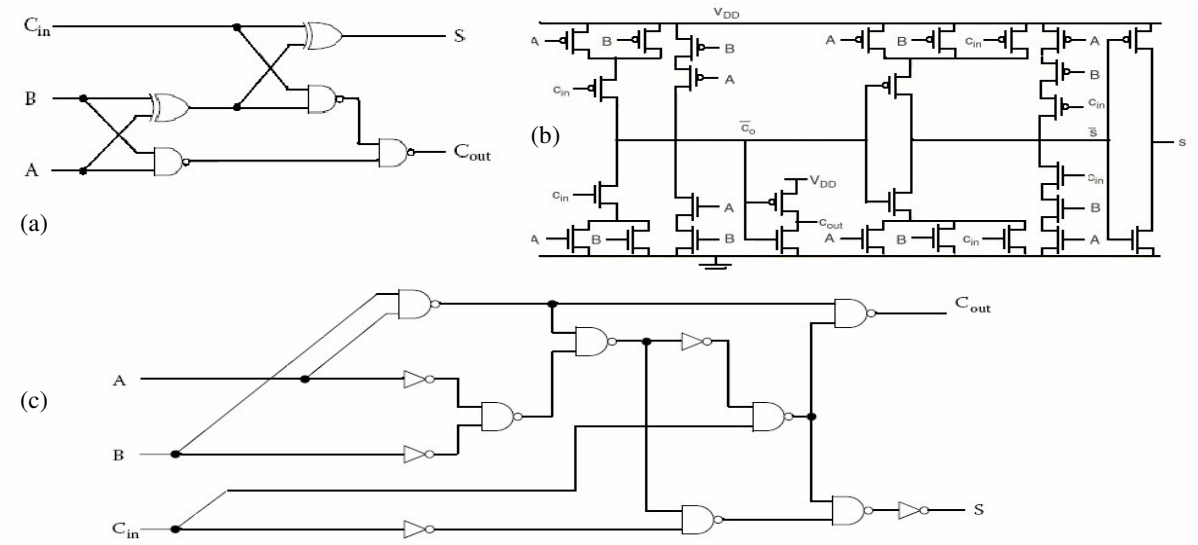

Fig. 2. used topologies of 1-bit full-adder cell. (a) XOR-FA. (b) Mirror-FA. (c) NAND-FA.

Since NBTI is a statistical effect, there is the need to describe the standard deviation in V_t generated. So From [2] the variance is:

$$\sigma^2_{Vt_{NBTI}}(t) = \sigma^2_{NIT} \cdot \left(\frac{q}{C_{ox}}\right)^2 = \frac{q \cdot T_{ox} \cdot \Delta V_t(t)}{\varepsilon_{ox} \cdot A_G} \qquad (4)$$

3. THE CIRCUIT

The circuit analyzed is an 8-bit full-adder made by eight 1-bit full-adder cells as shown in Fig.1. These cells are made using different topologies and it is intended to analyze the efficiency and reliability of adders made using these topologies. Three topologies were used in this comparison, they are the NAND-FA (Fig. 2. a), XOR-FA with transmission gates (Fig. 2. b) and the MIRROR-FA (Fig. 2. c).

Due to the fact that NBTI is duty cycle dependent, we had to estimate the probability, of each PMOS transistor of each topology, to be stressed. To make this estimation we considered all possible combinations at the inputs. Once the stressed period occurs when $V_g = 0$, is possible to know this probability, which were used to obtain the α constant for each transistor.

In a digital circuit, what defines the maximum operation frequency is the worst case delay, in full-adder circuit the carry output can be generated, be deleted or be propagated, in the circuit. The worst case happens when carry propagates over all of the 1-bit cells, because it is the longest pathway from the input to the output. Therefore in our simulation we analyze the NBTI in this worst case output, using the proper inputs. To simulate a real circuit add to have a fair comparison among the topologies, for all full-adder topologies we used as load capacitance, a $w/l = 1.5$ inverter. All the CMOS blocks of all the topologies used were sized to be equivalent to an inverter with wp=72nm and wn=48nm. The slope used in the inputs is 20ps.

4. SIMULATION AND RESULTS

For the simulations it was used the HSPICE from Synopsys. The PMOS and NMOS transistors model used in the simulations are the 32nm PTM model [5, 6, 7].

Once both NBTI and process variations are statistical effects, for its analysis it is needed to make a statistical simulation. These simulations were done using the Monte Carlo method in which are realized a lot of simulations changing the parameters as a probability distribution defined before. In our case the number of simulations was 2500, the process variation, for sake of simplicity, was only considered on V_t (with a 10% standard deviation) and the NBTI was according to the model presented before.

As the results of these simulations we first obtained the average delay and its standard deviation in the worst case transition for each one of the three topologies. From this result it was made the worst case graphic (Fig. 3.). In this graphic is shown the delay average plus three times the standard deviation normalized (to show more clearly the different susceptibilities) by the initial delay's average, what can be considered the worst case delay. In this figure it is possible to see the increase of the delay during the circuit's first 16 years, with this is possible to see the topology's susceptibility to NBTI and its reliability. The mirror-FA presented the major one with an increase of almost 15% in the first eight years while the NAND-FA and the XOR-FA did not pass the 11% margin.

Once the worst case delay increase logarithmically, to evidence each topologies susceptibility the Fig. 4. presents the same data of Fig. 3. but in a logarithmic scale. With this scale it becomes easily to compare which topology have a highly delay increase in time.

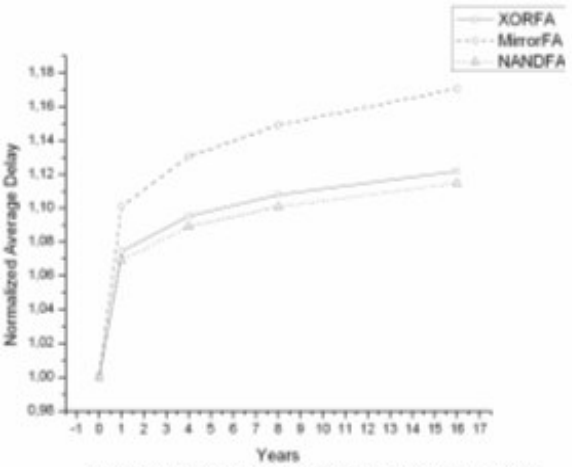

Fig. 3. Worst Case Normalized Delay X Years

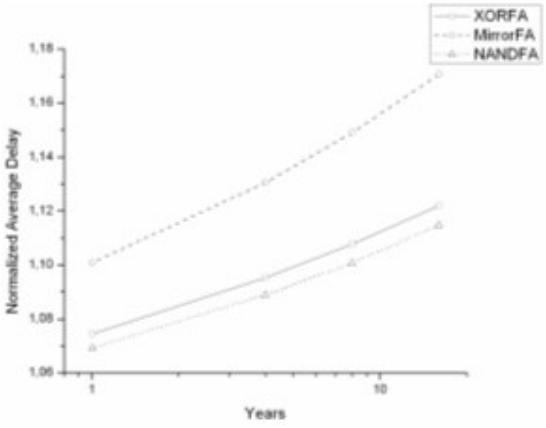

Fig. 4. Worst Case Normalized Delay X Years (Logarithmical scale)

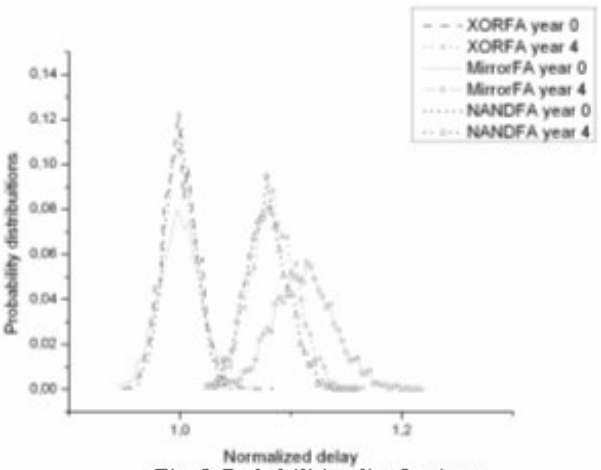

Fig. 5. Probabilities distributions

In Fig. 5. is shown the probability distributions for the topologies in the initial time and in the fourth year. In these distributions it is possible to see the delay's average and the standard deviation effect increasing on time. It is possible to see that the Mirror-FA have a higher increase on both of then, while the NAND-FA and the XOR-FA have a similar behavior.

After these analyses the Mirror-FA appear as the more susceptible full-adder topology while the NAND-FA presented the best results.

5. CONCLUSIONS

In this paper we presented a comparison among three complex arithmetic circuits, demonstrating how important is to consider the aging effects, such as NBTI, during the design of digital circuits. It was also possible to see that NBTI affects different topologies in different ways, hence its effect must be considered in a different manner for each circuit. Therefore, to predict this ageing degradation an analysis must always be done.

10. REFERENCES

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