FAST ALGORITHM TO LEAKAGE POWER REDUCTION BY INPUT VECTOR CONTROL

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ABSTRACT

Power consumption is a crucial parameter in CMOS circuit design. Leakage power is no longer a negligible component in low power circuits design due to the aggressive scaling of CMOS devices. Input vector control is an effective method to reduce leakage power when a circuit is in standby mode. It tries to find a vector that minimizes leakage power to be statically applied to the primary inputs of a circuit. The power consumption in CMOS circuits is evaluated in this work and a fast algorithm to reduce leakage power by input vector control is proposed. Experimental results on combinational circuits of ISCAS'85 benchmarks show this algorithm can accelerate calculation up to 25 times when compared to random vector technique and provides better results.

1. INTRODUCTION

The increasing use of portable devices and wireless communication systems along with continued increases in device density and operating frequency make power consumption a crucial concern in modern VLSI design. The most common technique to reduce dynamic power is scaling the supply voltage. To maintain the transistor driving capability, the threshold voltage has to be scaled, increasing the subthreshold leakage current. The technology scaling reduces the gate oxide thickness increasing the gate oxide tunneling current. Moreover, the leakage current through the p-n junction increase due to high doping profile used to mitigate short channel effects [1].

Leakage currents are the main responsible to static consumption in nanometer technologies and can take up 50% of the total power dissipated in 90nm technology process [2]. To face this new challenge, a great effort has been done in developing models, estimators and reduction techniques for design support.

Several techniques to reduce leakage currents are reported in the literature, such as dual-Vth, power gating and body biasing [1]. However, one of the most used is the known as input vector control [3]. It tries to find a minimum leakage vector (MLV) that can minimize leakage current to be statically applied to the primary circuit inputs. In fact, to find the MLV has an exponential complexity [4]. Consequently, a near-minimal leakage vector is used as the MLV in techniques reported in the literature [3-6].

This work proposes a fast algorithm to search the MLV to reduce leakage power consumption when the circuit is in idle mode.

2. LEAKAGE MINIMIZATION BY INPUT VECTOR CONTROL

Individual CMOS gates show a variation in the leakage power based on different input vectors. Table 1 shows the leakage power for a 2-input NAND gate in 90nm process. The leakage ratio between different inputs can be up to 6. The main reason for this difference is to the transistor stacking effect, where series-connected transistors tends to have lower leakage that the sum of each transistor leakage in isolation.

Table 1 – Leakage power for 2-input NAND gate in 90nm CMOS process.

Input Vector	Leakage Power (pW)
0 0	382.7
0 1	2298.9
1 0	1845.4
1 1	484.2

The minimum input vector leakage reduction technique is used to exploit this behavior applying the properly vector in the primary inputs of the circuit, while it is in standby mode. However, performing an exhaustive simulation for all input vectors to find the MLV is a NP-complete problem, being not feasible for large circuits. The practical solution to find the MLV is perform simulations with a set of random input vector and select the vector with less leakage [3].

An improved algorithm to guide the selection of the set of input vectors is proposed as follow:

1. Fix a circuit input 'i' at '0' logic value;
2. Perform leakage simulations for an 'n' number of random vectors;
3. Calculate the average leakage of these random vectors;
4. Perform the same procedure of steps 2 and 3 when the input 'i' is fixed at '1' logic value;
5. The smaller obtained average defines the logic value of the input 'i' in MLV;
6. Repeat steps 1 to 5 for every single circuit input 'i'.

3. EXPERIMENTAL RESULTS

To evaluate the proposed method, two benchmark circuits from ISCAS'85 were mapped with ABC technology mapping tool [7] using the genlib.44-6 library [8]. The logic cells, obtained during the mapping step, were implemented in standard CMOS logic style, using PTM 90nm technology [9]. All transistors were sized through the Logical Effort method [10]. The estimation leakage approach described in [11] was used to obtain the MLV values. The experimental results were performed in a Pentium D 2.8Ghz CPU with 1Gb RAM memory.

Table 2 shows the results obtained using the random input vectors solution (applying 1000 and 10000 vectors), and the proposed method (applying n=3 and n=5). The proposed method presents better results for the MLV than the random input vector solution. Also, the CPU execution time is smaller if compared to the random approach.

Table 2 – Experimental results.

Circuit	Random Vectors			
	1000		10000	
	MLV (mA)	Time (10^6s)	MLV (mA)	Time (10^6s)
C880	1,072	6,7	1,006	73,8
C1908	1,192	2,5	1,141	53,3
Circuit	Proposed Method			
	n=3		n=5	
	MLV (mA)	Time (10^6s)	MLV (mA)	Time (10^6s)
C880	1,036	2,68	0,979	4,38
C1908	1,271	1,22	1,14	2,08

4. CONCLUSIONS

This paper presented an efficient method to determine the circuit input vector which generates near-minimum leakage power consumption. This approach may be used to define the ideal input vector that sets the circuit for standby mode.

5. REFERENCES

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