A DIDACTIC CHIP FOR USE IN INTRODUCTORY MICROELECTRONICS COURSES

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ABSTRACT

This paper presents the development of an integrated circuit (IC) to be used by undergraduate students of electrical engineering at Universidade Federal do Rio Grande do Norte in introductory microelectronics courses. The IC is composed by field effect transistors, a source follower, a bump-antibump circuit, a differential amplifier, a follower integrator and differentiator and a wide range amplifier. The circuits were simulated and the layout was designed using 0.5μm AMI technology CMOS process.

1. INTRODUCTION

Analog circuits are used in several applications and learning about designing these circuits becomes a very important issue. Students of introductory courses on microelectronics need something more than the theory, allowing them to be in contact with the practice and to gain interest in microelectronics. So, it is very important to have an appropriate set of experiments.

Methods of synthesizing analog and digital circuits are different. In a digital design course, students can depart from the abstract idea of a problem through its validation in hardware in few steps. For instance, high-level model can be described in a Hardware Description Language (HDL) and then synthesized for a reconfigurable device such as a Field-Programmable Gate Array (FPGA) [1]. However for courses involving analog integrated circuits, students usually have a flow of project that can be seen on three levels: behavioral, structural and layout. After following this flow, performing experiments in laboratory, always related as being the most exciting part, is only possible with a long wait and expensive prototype silicon [2].

Because of the difficulty of obtaining integrated circuits, this paper proposes a chip for examining parameters and characteristics of analog circuits by undergraduate students, which is similar to the experiments proposed by the Institute of Neuroinformatics (INI) located at Swiss Federal Institute of Technology (ETH-Zurich) [3]. For example, students can plot characteristic curves of MOSFETs, compare NMOS x PMOS, known characteristic of amplifiers such as input and output impedance, Vout x Vin relationship and learn about current mirror and differential pair circuits. This will contribute to the learning capabilities of students.

In the field of engineering, it is important to contribute with material research and technology development, providing new methodologies for education [4].

2. ANALOG CIRCUITS

In this section, the circuits that constitute the didatic chip will be described and shown in the schematic diagram.

2.1 Field Effect Transistors

The metal-oxide semiconductor field-effect transistors (MOSFET) are the major devices used in the field of microelectronics [5].

In the didatic chip, ten MOSFET transistors can be found: five NMOS and five PMOS.

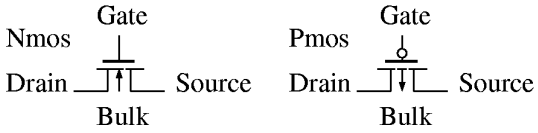


Figure 1: MOSFETs symbol

The PMOS and NMOS transistors have the same width (W = 32 μm) and their lengths are different (32 μm, 16 μm, 8 μm , 4 μm, 2 μm).

2.2 Source Follower

The source follower presents a voltage gain smaller than unity. It has a high input impedance and a low output impedance [5]. The sizes of transistors M1 and M2 (fig. 2) are W = 12 μm and L = 10 μm.

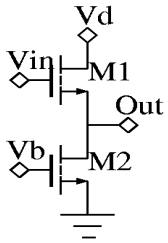


Figure 2: Schematic diagram of the source follower

2.3 Bump-Antibump circuit

The bump-antibump circuit gives three current outputs that are correlated with two input voltages. Output I_{out} is the bump output and when I_{out1} and I_{out2} are combined, they form the antibump output . When the input voltages are equal ΔV = V1-V2 = 0 I_{out} is large and $I_{out1} + I_{out2}$ is small. If ΔV is large, $I_{out1} + I_{out2}$ is large and I_{out} is small [6]. The dimensions of transistors shown in fig. 3 are: W/L = 12 μm /10 μm for M1, W/L = 12 μm /4 μm for M2 and M3, W/L = 6 μm /10 μm for M4 and M5.

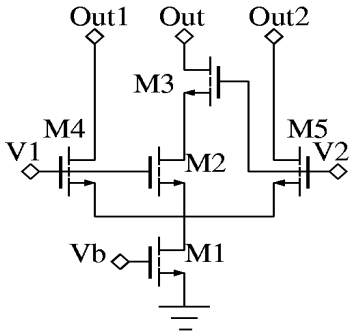


Figure 3: Schematic diagram of the bump-antibump

2.4 Differential Amplifier

In the differential amplifier, the output current depends on the difference between the two input voltages Vp and Vn. It is built with a source-coupled pair and a current mirror. The sizes of transistors in fig. 4 are: W/L = 6 μm /6 μm.

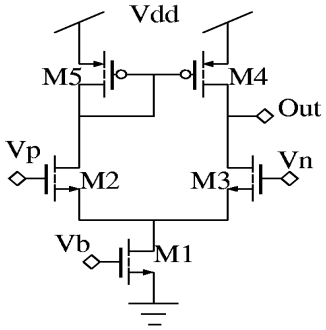


Figure 4: Schematic diagram of the differential amplifier

2.5 Follower Integrator and Differentiator

Integration and differentiation operations are of great importance for engineering. The follower is constructed out of the differential amplifier, described above, a decoupling capacitor in the minus input Vn and negative feedback configuration fig.5 [6]. The follower is implemented with: a capacitor of C = 14 pF and five transistors with dimensions are W = L = 6 μm.

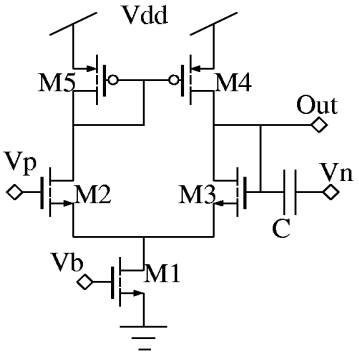


Figure 5: Schematic diagram of the follower integrator and differentiator

2.6 Wide Range Amplifier

If an application requires a wide output range, a simple differential amplifier cannot be used because of its finite minimum output voltage. A solution for this problem is using a wide range differential amplifier. The open-loop gain or large output currents depend on the size W/L of output stage transistors [6]. In the fig. 6, all transistors have the same W = 6 μm and L = 6 μm with the exception of M8 and M9 with L = 51μm.

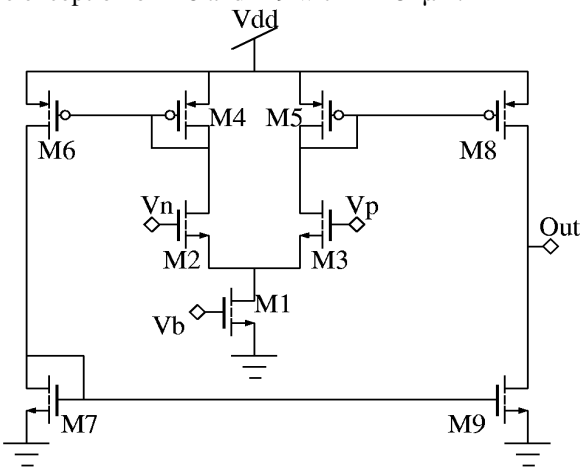


Figure 6: schematic diagram of the wide range amplifier

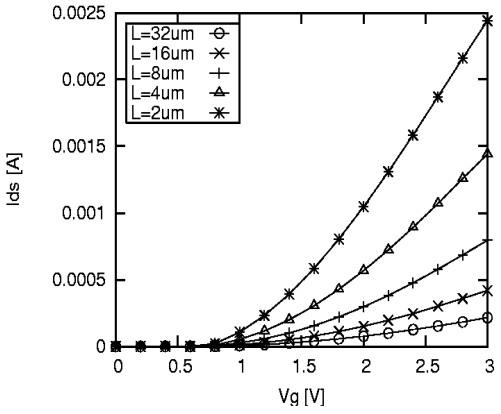
3. SIMULATION AND LAYOUT

The circuits were described with SPICE [7]. Simulations and layout design were performed with Mentor Graphics® tools .

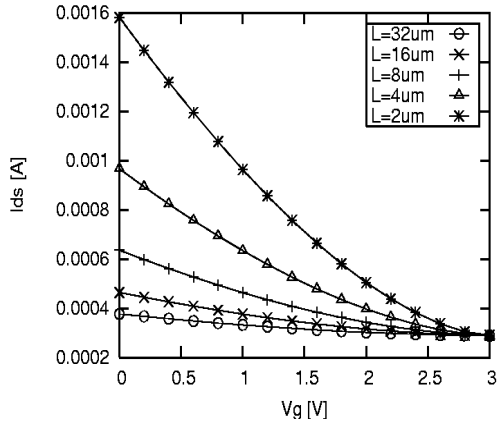
All simulations were done considering all transistors in saturation and disregarding the term of channel-length modulation [5], the transistor's IxV relationship can be written as:

$$I_d = \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{gs} - V_{th})^2 \quad (1)$$

For plotting the MOSFETs characteristic curves, we used same terminal voltages. As shown in (1), there is a current dependence on the geometry of the transistor width W and length L. In the simulations, we observer an inverse relationship between current Ids and length L in fig. 7.



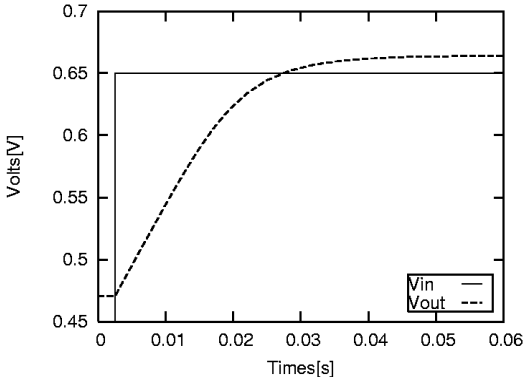
(a) NMOS



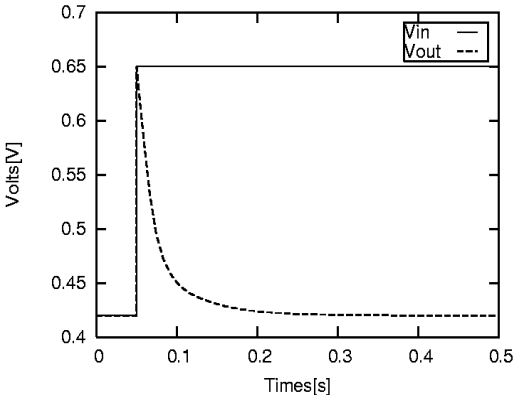
(b) PMOS

Figura 7: Simulation results of the MOSFETs Ids versus Vg characteristic for various L values

The follower integrator and differentiator acts as an integrator by connecting a constant voltage on the capacitor and by applying a voltage Vin (input voltage) on the Vp node. It acts as a differentiator by connecting a constant voltage in Vp and applying a voltage Vin on the capacitor.



(a) Integrator step response



(b)Differentiator step response

Figura 8: Simulation results of the circuit fig. 5

The layout was drawn using design rules of the 0.5μm AMI-C5 tecnology. This n-well CMOS process has 3 metal layers and 2 poly layers. The layout is shown in fig. 9.

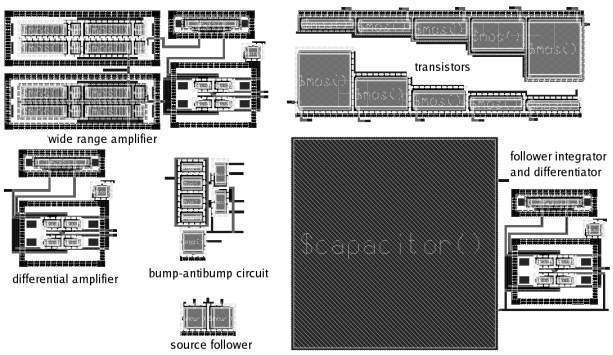


Figure 9: Layout of the didactic chip structures

5. CONCLUSION

This paper proposes a didactic chip containing analog circuits to be used by electrical engineering undergraduate students at UFRN. The goal of the chip is to serve as an academic device, so that the students can have the opportunity to make few experiments with it in the laboratory, and hence learn and get more interests in microelectronics. It was sent to fabrication by MOSIS and will available for use in the second semester of 2008.

It was shown some simulations and layout of the circuits. As future work, we will perform measurements on the circuits and compare the results simulations and theory.

6. ACKNOWLEDGEMENTS

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7. REFERENCES

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