# DESIGN PARAMETERS AND THEIR IMPACTS ON A CMOS APS SENSOR RESPONSE

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## ABSTRACT

This paper presents an analysis of several aspects of the APS (Active Pixel Sensor) model through SPICE simulations. We perform an analysis on circuit response to the variation of few design parameters, such as the output buffer aspect ratio, pixel load effect and photo-generated current levels; as well as modification on the classical APS circuit, by including a transfer-gate transistor.

## 1. INTRODUCTION

Active Pixel Sensors have been widely applied from digital-camera-sensor primary units to position-sensitive detectors. An active pixel is basically a photodiode connected to functional MOS transistors. In its simplest architecture only a reset and a buffer transistor are employed, besides a read transistor in the case of a pixel array [1]. The reset transistor periodically resets the voltage at the photodiode terminals to a reference level, which decays as light impinges on the pixel. If the measurement time is short enough compared to the pixel internal time constant, the voltage variation can be considered linearly proportional to the photo-generated current. The buffer transistor, the gate of which is connected to the photodiode output terminal, reports the signal voltage to the data line. Modeling this kind of sensor is important in order to optimize the sensor design parameters and its response output.

## 2. APS SIMULATION

The APS model is shown in Fig. 1. The photodiode model is composed by a current source, paralleled to a capacitor, a resistor and a diode. The model also includes a series resistor, which is responsible for characterizing contact and conduction losses. M1 is the reset transistor, which resets the voltage on the photodiode to high-level every beginning cycle. As the reset transistor is switched off, the generated photocurrent discharges the internal photodiode capacitance, which voltage is buffered to the output by the source-follower transistor M3. M4 is used for row selection, when the APS is a matrix part. M2 is the transfer gate transistor. By switching it off, we can decouple the photodiode capacitance from the circuit [2].

The simulation of Fig. 2 shows gate and source voltages on the buffer transistor. The voltages are kept constant as long as the reset transistor is on. When it is set off, the voltage on the photodiode cathode terminal drops (by the photocurrent action) to the negative of the parallel diode forward voltage (with reference to ground).

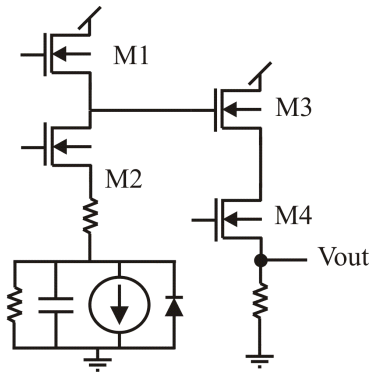


Figure 1. APS Model

In Fig. 2, it can be seen this negative voltage on the buffer input. The continuous photocurrent is sinking charge from one terminal of the capacitor and sourcing to the other. The negative voltage is clamped by the diode, at a voltage $V_D$ (diode forward voltage drop). This behavior is not always noticed on real circuitry because the sense node is rarely available to external world as it can introduce additional capacitance on the sense node (input buffer node). This phenomenon was observed in practice in discrete implementations of the active pixel model.

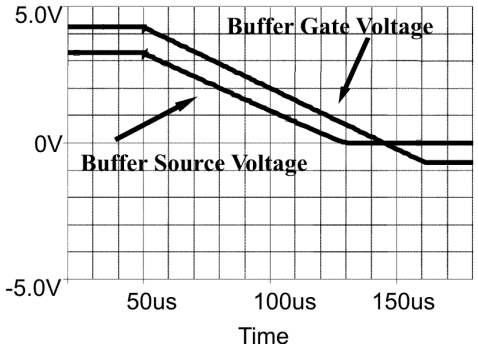


Figure 2. APS Simulation

## 3. OUTPUT DUE TO PHOTOGENERATED-CURRENTS

This pixel is an optical sensor. The photocurrent depends on the incident light intensity. The circuit was simulated using different photocurrents of *200nA*, *500nA* and *800nA*. Capacitance was considered constant as in many APS analysis [3]-[5]. Simulation results are shown in Fig. 3.

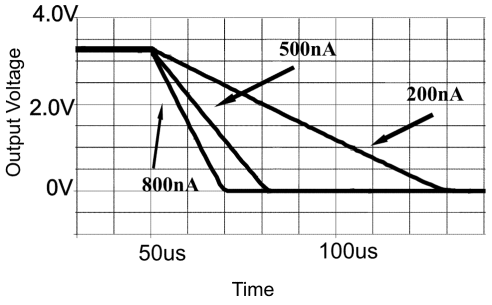


Figure 3. Pixel output voltage due to various photo-generated current

The output voltage is related to the sense node voltage by:

$$V_{out} = V_{sn} - V_{t3} - \sqrt{\frac{2I_{load}}{\mu_n C_{ox}(W/L)_{M3}}}$$

where $V_{sn}$ is the voltage on the photodiode terminals and $I_{load}$ is the imposed load current [2].

One can notice that the greater the photo-generated current, the faster the voltage output will drop, once the capacitor discharges faster.

By measuring the output voltage after an integration time, different values will be found accordingly to the light current, so the output voltage represents the light intensity the sensor was exposed to during the integration time.

## 4. BUFFER-TRANSISTOR ASPECT RATIO

According to the *SPICE2* transistor model, the drain current is direct related to the aspect ratio of the transistor (5). This model was used because it is still suitable to gate lengths above *1μm*. We simulated various buffer aspect ratios for a fixed *L=1.6μm*.

The increase on the buffer output aspect ratio has direct impact on the source-follower transfer characteristics. The most it is increased, the most the buffer acts like an ideal source-follower. There is, indeed, a practical limit where this increase is beneficial in terms of area requirements, which directly impacts the resolution of an APS matrix.

We noticed that when the buffer width increases up to 10μm, the output-input ratio is significantly improved, as can be seen in Fig. 4, and further increases of the width impacts mildly the voltage ratio whereas area requirement increase considerably.

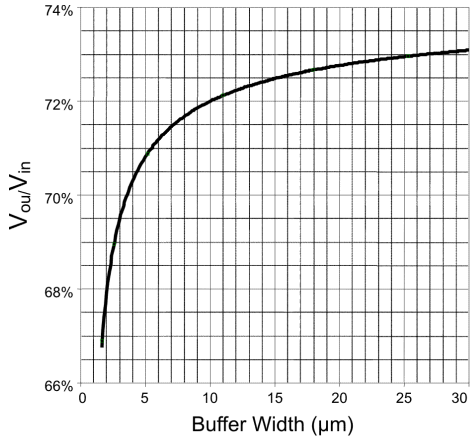


Figure 4. Buffer output-input ratio by the buffer width (fixed buffer length).

## 5. PIXEL LOAD EFFECT

Considering the selected buffer transistor aspect ratio 3:1, the load effect can be more clearly noticed for hard loads (less than 200kΩ). The optimum value seems to lie between 200kΩ and 600kΩ for the maximum signal range. This is the reference load value for a future active load design.

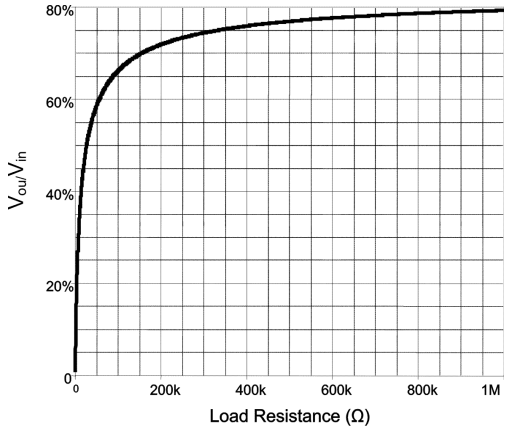


Figure 5. Output-input relation due to various pixel loads

## 6. RESET AND TRANSFER-GATE COMPLEMENTARY TRANSISTORS

By placing complementary PMOS transistors in parallel to the reset and the transfer-gate transistor, we expect to achieve better SNR once the dynamic range is extended (now, the reset voltage on the sense node can reach $V_{DD}$ once there is no effect of the reset transistor threshold voltage which drops the voltage applied to the

sense node by $V_T$ in case of only a NMOS transistor is used). We also keep the NMOS reset transistor in place in order to give flexibility to the reset voltage value.

The simulation results showed that without the complementary transistors, the maximum voltage output was about *3.32V*. By adding complementary parts, the voltage output was increased to *4V*.

The inclusion of PMOS transistors however decreases the pixel fill factor. In this case there is a compromise between signal output and area demands.

Another impact of complementary transistors inclusion is the need of complementary control signals for the reset and the transfer-gate transistors.

## 7. CLOCKING OF RESET AND TRANSFER-GATE

The inclusion of a transfer-gate transistor adds more flexibility to the pixel readout scheme. The clocking of the reset and the transfer gate becomes crucial in order to take advantage of the new structure.

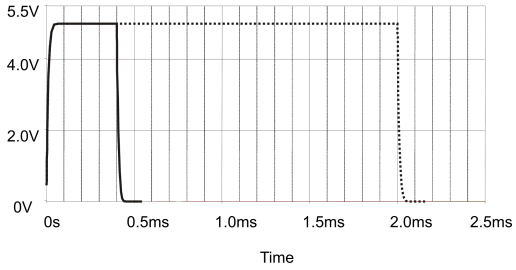


Figure 6. Reset gate voltage (full). Transfer-gate command voltage (dotted).

## 8. TRANSFER-GATED PIXEL RESPONSE

If a transfer-gate is included in the pixel circuit, the pixel response changes. The transfer gate adds some amount of capacitance into the sense node, but this increase is negligibly compared to the photodiode intrinsic capacitance.

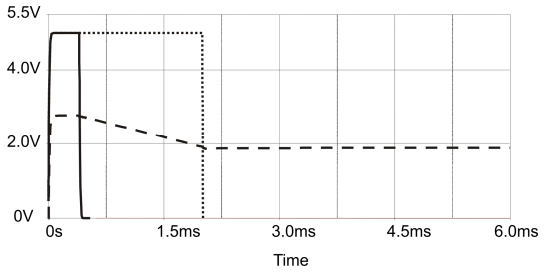


Figure 7. APS response: Reset signal (full). Transfer-gate signal (dotted). APS Output (dashed).

The circuit photodiode is charged by the reset transistor, while the transfer-gate is kept on (to allow charges to flow to the photodiode during reset). Than, the reset pulse is stopped while the transfer-gate transistor is still on. The photo-generated current discharges the photodiode during the integration time. At this time the transfer-gate is switched off and the voltage on the buffer input is kept constant until it is discharged by leakage currents. Fig. 7 shows the response when the transfer-gate transistor is switched off.

The inclusion of the transfer-gate transistors add more flexibility to the readout, as it acts like a sample and hold circuit, keeping the voltage on the output (once it is no more affected by the photocurrent).

## 9. CONCLUSIONS

In this paper we analyzed the impact of various design parameters on the response of an Active Pixel Sensor. An alternative circuit topology was studied, composed by associations of components, such as the transfer-gate transistor, complementary PMOS transistors and a clock scheme. The transfer gate transistor, in contrast to regular APS designs, allows the photosignal to be read in a convenient time. Another design choice consists in choosing complementary NMOS/PMOS transistors for the reset operation, thereby increasing the magnitude of the sense-node reference voltage, and consequently the output signal-to-noise ratio; one setback is the increased pixel area, affecting predominantly high-density arrays. The increase in the buffer-transistor aspect ratio has been shown to improve the output dynamic range. This measure, however, is only advisable within the range where the improvement is steep; beyond this range, the simultaneous area increase is not justifiable. The conclusions drawn in this paper are helpful in the assessment of the compromises among area, signal range and clocking cycles, the demands of which depend on the target application.

## 10. ACKNOWLEDGEMENTS

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## 11. REFERENCES

[1] E. R. Fossum, “CMOS Image Sensors: Electronic Camera-On-A-Chip”, *IEEE Trans. Electron Devices* 44 (10), 1689 (1997).

[2] D. W. de Lima Monteiro, *CMOS-Based Integrated Wavefront Sensor*. Delft Univ. Press, Delft, The Netherlands (2002).

[3] L. G. McIlrath, “A low-power low-noise ultrawide-dynamic-range CMOS imager with pixel-parallel A/D conversion,” *IEEE J. Solid-State Circuits*, vol. 36, no. 5, pp. 846–853, May 2001.

[4] R. Oi and K. Aizawa, “Wide dynamic range imaging by sensitivity adjustable CMOS image sensor,” in *Proc. IEEE Int. Conf. Image*, Sep. 2003, vol. 2, pp. 583–586.

[5] P. B. Catrysse and B. A. Wandell, “Integrated color pixels in 0.18-$\mu$m complementary metal oxide semiconductor technology,” *J. Opt. Soc. Amer. A, Opt. Image Sci.*, vol. 20, no. 12, pp. 2293–2306, Dec. 2003.