DESIGN AND EVALUATION OF A NMOS 90 nm 3D DEVICE

Thiago Assis, Gilson Wirth, Fernanda Kastensmidt, Ricardo Reis

PPGC – Universidade Federal do Rio Grande do Sul

ABSTRACT

This work presents the results of the design and evaluation of a NMOS 90 nm 3D device. Developed using data extracted from 90 nm predictive models and the validation was done comparing the results of current and voltage behavior of the model with a 90nm Predictive Technology Model (PTM) from the Arizona State University (ASU) and data extracted from *ST 90 nm* design rule document. Results show a threshold device of *0.36 V*, a sub-threshold slope of *69.6 mV/decade*.

1. INTRODUCTION

With transistor scaling to nanometer technologies new trends and effects must be analyzed to ensure their proper operation. Nanometer devices are defined as those that are at the range from 100 nm to 1 nm, with that, a n-type transistor of 90 nanometer was modeled and its functional behavior and tunneling effects were analyzed.

The scaling through micrometer technologies to nanometers had imposed the necessity of use several process level techniques to allow the proper operation of the devices. As already known by community the scale is not symmetric to every technology property leading to undesired effects that must be carefully analyzed.

In this work the scale effects due short channel and gate oxide thickness were taken into account to build the device. In the next paragraph hot carriers and tunneling effect will be briefly presented.

Hot carriers effects are caused due abrupt source\drain junctions with channel. The peak of the electric field at the charged region allows an acceleration of the carriers increasing their kinetic energy which is able to create a weak avalanche at silicon. Part of these carriers are able to damage the silicon-oxide interface degrading the device [1].

Another effect is caused due the thin oxide at the oxide/silicon interface. The tunneling consist on a nanometer phenomenon in which carriers (electrons-holes) are able to pass through a potential barrier higher than particle kinetic energy [1]. This phenomenon is strongly dependent of temperature and oxide thickness. The last two effects will be take into account and process level techniques will be used to prevent their effects.

The main contribution of this article is expose to community the modeling of a NMOS 90 nm device in a 3D simulation environment and presents the tunneling of the device over a oxide of 1.5 nm. Simulations were conducted using the tool Davinci from Synopsys [2].

2. PREDICTIVE 90 nm DEVICE

Data extracted from [3] and [4] suggest the topology showed in figure 1. The model presents a NMOSFET using a Super Steep Retrograde (SSR) channel doping, source/drain halo and a Light Doped Drain (LDD) structure. The SSR technique described at [5] and [6] consist of a channel engineering technique used to prevent short channel effects on nanometer MOS devices. The technique proposes to increase the doping of the substrate (prevent short channel effects) and create a thin layer with a lower doping near the surface of oxide and silicon to control the threshold of the device. Using the SSR doping and its thickness (of the channel), it is possible to change the threshold of the device without the necessity of changing the oxide thickness.

The halo implant is also a channel engineering technique used to control short channel effects. This structure will not be used in this work, for more details about halo implants consult [5]. The LDD structure consist of creating a small active region that will be overlapped by the channel using a thickness smaller that the active region (Source\Drain) and with a smaller doping concentration [1]. The LDD is used to limit hot carriers effects, a phenomenon that was showed before in the introduction.

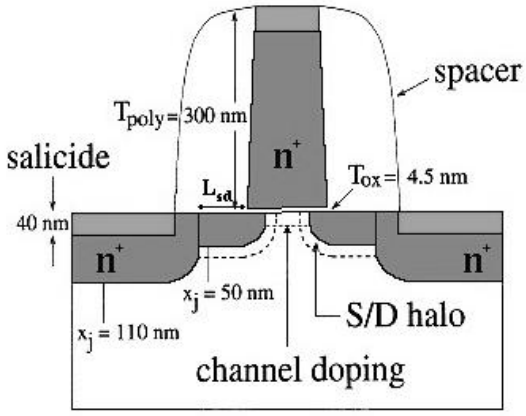

Fig.1- NMOSFET device [3]

In figure 1 the structure of the NMOSFET device is showed. Notice the different thickness form the LDD and source\drain active regions. The source\drain halos are not shown in details and just their positions are indicated. The dash lines over the channel indicate the SSR channel doping.

Another work that presents a 90 nm device is [7]. In that work a device is created to evaluate the soft error

collection mechanism and a technique on process level to reduce soft errors effects is presented. The doping profiles and devices regions dimensions where analyzed with the data from [3] to create the device proposed in this work. At the next section the developed model is presented.

3. MODELED DEVICE

The first step to create a device model is to define a strategy to build the MESH. The MESH is a structure where the device regions are created and their sections and points define where physic calculations are done to evaluate the simulations. If the MESH is defined with too much simulation points will lead to many days of simulation, but if this number is small the results of the simulation will be too far from a real device operation. A good strategy to define the MESH is presented at [7] where the author suggests the creation of a MESH divided on regions with higher and lower concentration of simulation points and with the refinement of the points on areas on which the simulations are more important. In this work these regions would be the active regions and channel.

With the data extracted from [3] and [7] the device where constructed. After simulations the doping profiles and dimensions where calibrated to achieve the desired behavior and electrical characteristics. In figure 2 the developed model.

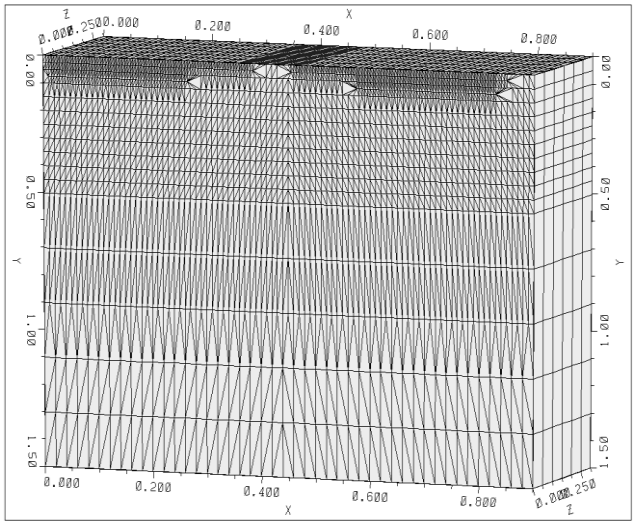

Fig. 2 - Developed NMOS 90nm device

Notice the y axis at figure 2 that from *0.0* to *0.5um* the MESH has more points that from *0.5* to *1.5 um*. Over active regions and channel the MESH is refined to receive more simulation points. This kind of refinement is done during simulations to achieve the desired accuracy.

In table 1 the dimensions of the LDD, SSR, active regions, gate and oxide. The doping profile is also presented.

Region	Width (x)	Width (y)	Width (z)	Doping
LDD	*115 nm*	*30 nm*	*240 nm*	*n-type. Peak: 1e19*
Source\Drain	*240 nm*	*60 nm*	*240 nm*	*n-type. Peak:1e20*
SSR	*90 nm*	*5 nm*	*240 nm*	*n-type. Peak:1.5e18*
Gate	*136 nm*	*300 nm*	*240 nm*	*n-type. Peak:2e20*
Oxide	*136 nm*	*1.4 nm*	*240 nm*	*None*
Substrate	*0.9*	*1.5*	*0.3 um*	*p-type. Peak:5.5e18*

Table 1: Dimensions and doping profiles

The doping has Gaussian distribution. The difference of doping between Substrate and SSR is used to control the threshold of the device. Using an uniform substrate doping the threshold of the device was too high almost near *VDD* (1.2 V for this device) and the SSR was used to reduce its value. The oxide was not adjusted to control the threshold voltage and this value is the same that [7] had been used to 90 nm high performance devices.

4. SIMULATION RESULTS

To validate the NMOS transistor, simulations were conducted to analyze the behavior of the device when a bias is applied at terminals (substrate, source, gate, drain). Over the simulations in figure 3 and 4 the substrate and source where grounded (Vs=Vb=0V). At figure 3 the Vds is fixed on 1.2 V and a bias is applied on the gate terminal.

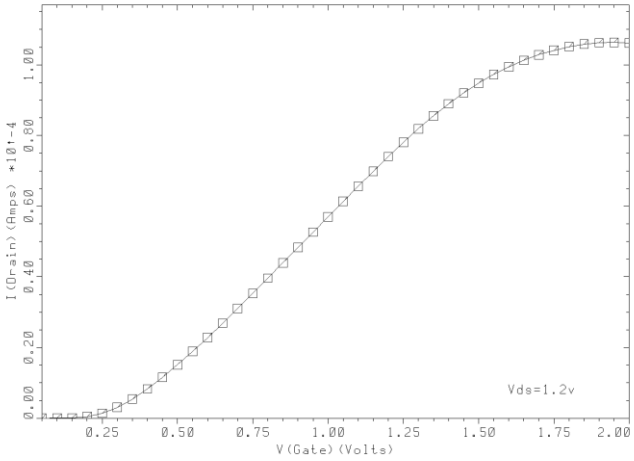

Fig. 3 - Ids vs Vgs

To validate the agreement of the model with electrical parameters of a 90 nm device, simulations where conducted using a PTM available in reference [8]. The threshold voltage of the PTM model was about *Vt=0.29 V*. The document of design rules from ST 90nm [9] indicates a *Vt=0.34 V* for high speed devices of that technology. The threshold voltage of the developed model was obtained by *MOS* parameter extraction command of TCAD and is about *Vt=0.36* V. The sub-

threshold slope of the device was found to be 69.6 mV/decade.

The range of the measure sub-threshold slope also fits with the measurements in reference [10]. At the work mentioned before the author makes an extensive analysis of different parameters (oxide, channel length) and their effect over the sub-threshold.

The scale of the simulation (*Ids vs Vds*) of the PTM model and results from the reference [7] also fits with the results of the developed device. In figure 4 the Vgs is fixed on 1.2 V and the drain bias is varied.

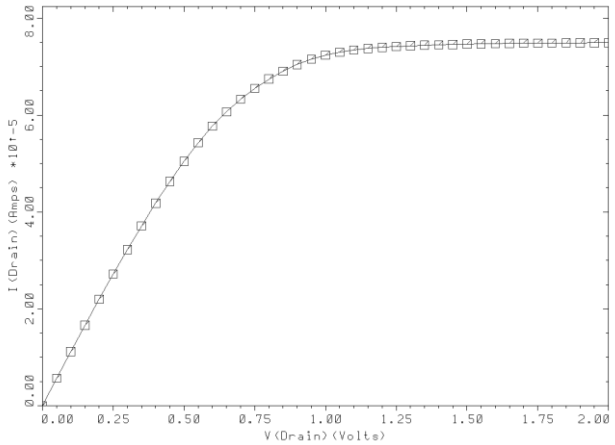

Fig. 4 - *Ids vs Vds* simulation

With these figures the main behavior of the transistor is verified. The last simulations were conducted using Newton and Incomplete Cholesky Conjugate Gradients (ICCG) numerical methods.

As the device has a small oxide (1.4 nm), the effects of the tunnel mechanism were also evaluated.

In Figure 5 the direct tunneling analysis for a Vds=0 V.

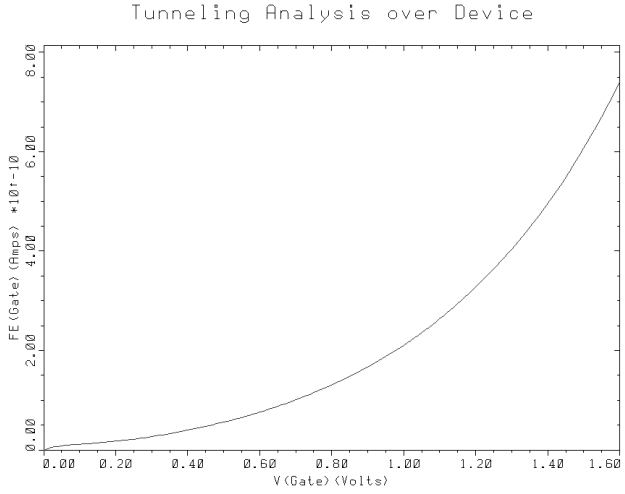

Fig 5 – Direct Tunneling Vds=0 V

At temperature with 300 K and Vds=0V the current at Vg=1.2 V is about 0.32nA. The *FE(Gate)* is the direct tunneling current function used by Davinci. The direct tunneling current was also evaluated for different drain bias conditions. At the next figure the analysis for different bias.

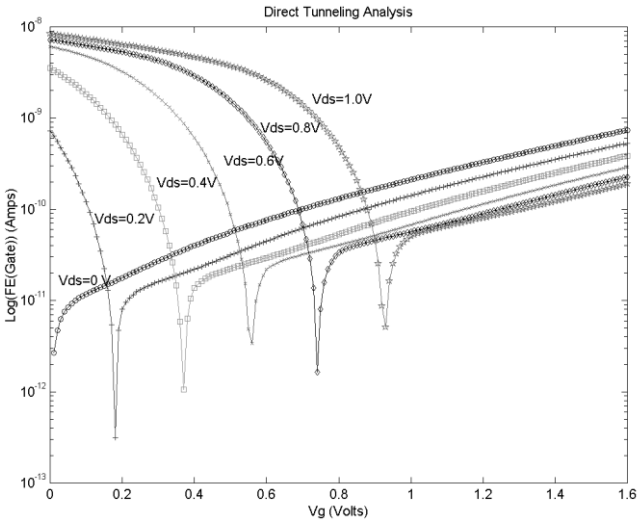

Figure 6: Direct Tunneling Analysis

The figure 6 is in logarithmic scale and shows the current flowing through the channel to the gate and gate to channel. At the left part of the figure from Vds=0.2 V to Vds=1.0 V is possible to notice that the current start to drawn until a certain point near the Vg with a value near the used Vds. At this point the current is negative and is flowing from channel to the gate. After this point the current becomes positive what mean that the current is flowing through the gate to the channel.

In reference [11] the author exposed the main components of the gate tunnel current. The inversion of the current signal in the figure 6 is explained by the increase of the gate current. When Vds bias is greater them Vgs the current is passed from the substrate (channel) to the gate, this behavior is changed when the bias of Vgs reach Vds and the current start to take the inverse path.

These simulations were solved using the numerical integration of the Gundlach Tunneling Coefficient. The direct tunneling analysis combines both direct tunneling regime and the Fowler-Nordheim regime.

In Figure 7 the bias of regions of the device during operation (*Vgs=1.2 V*).

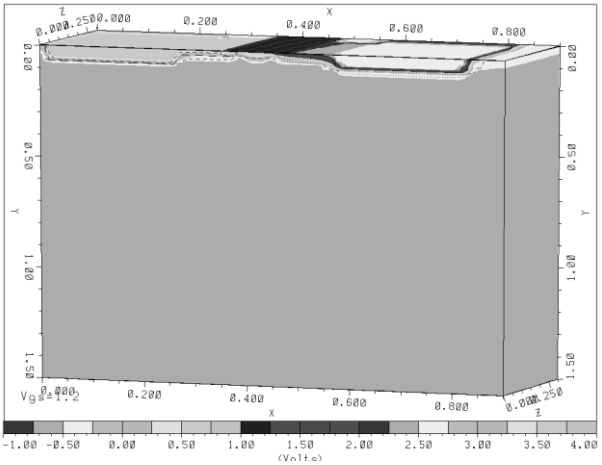

Fig. 7 - Device operation at *Vgs=1.2 V*.

The Figure 7 shows the *NMOS* transistor during operation, its is possible to notice the difference between the voltage of the substrate and source, which is a body effect that changes the threshold of the transistor.

5. CONCLUSIONS

This paper presents the modeling of a NMOS 90nm device in Davinci tool from Synopsys. Results comparing the device with PTM simulations and values extracted from [7] and ST 90 nm shows a good agreement with the model.

The threshold of the device was pretty near the *Vt* of ST 90 nm High Speed device and the sub-threshold slope of the device was measured and is equal to *69.6mV/dec*.

The direct tunneling current was evaluated showing the behavior of the device to the oxide of *1.5 nm*. The measured tunneling current was about *0.32nA* to a *Vds=0V* and *Vg=1.2 V*.

10. REFERENCES

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