IMPACT OF DIFFERENT OP-AMPS IN CMOS BANDGAP REFERENCES IMPLEMENTED IN 0.18µM TECHNOLOGY

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ABSTRACT

One of the most used topologies of CMOS Bandgap Voltage References (BGR) is that one with operational amplifier (op-amp), current source, three resistors and two parasitic bipolar transistors. Besides the simplicity and good performance achieved by this BGR, this topology can be easily modified to achieve high-accuracy. In literature, many different op-amps are employed in this BGR architecture. Since the BGR performance depends strongly on the performance of the amplifier used, the op-amp design deserves attention and its architecture must be careful chosen. Therefore, aiming to achieve the best trade-off between several op-amps used in BGRs, it is necessary to realize a comparative analysis. This work evaluates the performance achieved by one BGR using four different topologies of error-amplifier: OTA, Symmetrical OTA, two-stage Miller and folded-cascode. The BGR with the op-amps were designed in a commercial 0.18µm CMOS technology. Results show that the use of adequate error-amplifier topology can define the performance achieved by the BGR, for example, improving the robustness against variability or noise from the supply lines.

1. INTRODUCTION

Voltage reference circuits are essential building block in the design of several applications, for instance, voltage regulators and data converters. Bandgap references (BGR) are widely used implementation for voltage references [1]. Among the several BGR implementations presented in the literature, one of the most used architecture is the one shown in figure 1, item (a) [1]. Using a simple and low-cost circuit, this BGR topology achieves the performance required by many analog and RF applications. Furthermore, with the addition of only one extra resistor, made of different material compared to the other resistors in the circuit, this BGR topology achieves a temperature performance in the order of 5 ppm/°C [3].

As can be seen in figure 1, the operational amplifier (op-amp) A is employed in the BGR to make nodes “a” and “b” to have the same voltage. In literature, there is a lot of different implementation for the op-amp A used in this type of BGR circuit. Operational Transconductance Amplifier (OTA), Symmetrical OTA, two-stage Miller and folded cascode amplifier are examples of architectures employed – as can be seen in table 1. Figure 1, item (b) to (e) illustrates these op-amps.

Work:	*[5]*	*[7]*	*[3]*	*[4]*	*[6]*	*[8]*	*[9]*	*[10]*
OTA	*X*	*X*						
Sym. OTA			*X*	*X*				
2-Stage					*X*	*X*		
Folded							*X*	*X*

Table 1: Different amplifier employed in BGR´s

Since the performance of the BGR depends strongly on the performance of error-amplifier, the design of the amp-op deserves attention and its architecture must be careful chosen [11]. Therefore, aiming to achieve the best trade-off between several op-amps used in BGRs, it is necessary to do a comparative analysis. This work evaluates the performance achieved by the BGR using four different topologies of error-amplifier: OTA, Symmetrical OTA, two-stage Miller and folded-cascode. Results show that the use of adequate error-amplifier topology can define the performance achieved by the BGR, for instance, improving the robustness against variability or noise from the supply lines. Therefore it is possible to identify which op-amp architecture is adequate for each BGR specification. Moreover, it is also presented several design guidelines for these amplifiers focusing in BGR´s. All circuits were designed in IBM 0.18µm CMOS technology.

This work is organized as follow. The BGR circuit used as case of study is presented in section 2. Section 3 presents the four designed amplifier and several design recommendations. Section 4 shows the simulation results and the conclusions are presented in section 5.

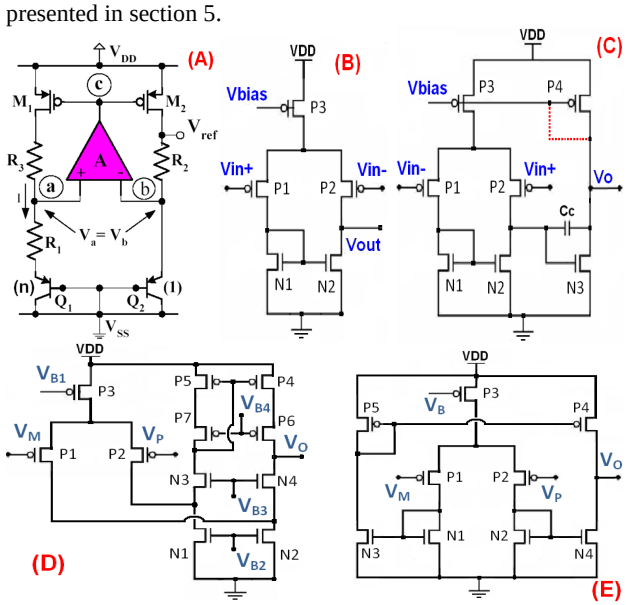

Figure 1. BGR and amplifiers: (a) BGR, (b) OTA, (c) 2-Stage, (d) Folded-cascode and (e) Symmetrical OTA

2. BANDGAP REFERENCE

The Bandgap voltage reference operates by summing the emitter-base voltage (V_{BE}) of the bipolar devices (BJT´s) and a voltage that is proportional to the absolute temperature (PTAT). The BGR shown in figure 1 performs this balanced summing as explained in the sequence. Using an error-amplifier with high gain, it is possible to get equal voltages at the nodes “a” and “b”

- since the negative feedback is provided. The resistor R_1 helps the negative feedback factor (β_N) be greater than the positive feedback factor (β_P). Therefore a current I, given by equation (1), with PTAT temperature coefficient (TC) is generated if the two BJT´s are operating with different current density. In equation (1), ΔV_{BE} is the difference between V_{BE} of the two BJTs; V_{TH} is the abbreviation of Thermal voltage and n is the ratio of emitter areas of Q_1 and Q_2.

$$I = \frac{\Delta V_{BE}}{R_1} = \frac{V_{TH} \cdot \ln(n)}{R_1} \quad (1)$$

When resistors R_2 and R_3 have the same resistance, the V_{DS1} and V_{DS2} can be obtained to provide a good current matching by M_1 and M_2. Therefore, a reference voltage (V_{REF}) described by equation 2 is generated in the drain of M2. The obtained output voltage is equal to silicon Bandgap voltage (≈ 1.2 V) and it is ideally independent of operation temperature.

$$V_{REF} = V_{BE2} + \left(\frac{R_2}{R_1}\right) \cdot \ln(n) \cdot V_{TH} \quad (2)$$

The accuracy of the output voltage may be degraded by different factors. The first one is the variability due the fabrication process. For instance, the mismatches among devices electrical parameters of the amp-op will result in a random offset voltage (V_{ROF}). Besides the V_{ROF}, there is also the systematic offset voltage (V_{SOF}) even if the devices are ideally matched. The systematic offset can be reduced through careful design and an adequate choice of the amplifier topology. Both offset voltages results in the total offset voltage (V_{OS}). The relationship of V_{OS} and the output voltage is given by (3). Once the V_{OS} is amplified by the factor equal to R_2 over R_3, what it is usually on the order of 10, the output accuracy may be really damaged. In fact, V_{OS} is the biggest error source that causes the non-reproducibility in the output voltage temperature coefficient [12]. Verifying equation (3) one can see that the offset error contribution can be reduced by making n bigger and decreasing the factor R_2 over R_3. One way to achieve this is to obtain ΔV_{BE} by taking the difference of two cascaded transistor string [12]. However, even with such recommendation, sometimes the performance achieved by the BGR is not enough for high-accuracy applications, and consequently, V_{REF} must be trimmed to an output voltage which is predetermined to give a near-zero TC [12].

$$V_{REF} = V_{BE2} + \left(\frac{R_2}{R_1}\right) \cdot \ln(n) \cdot V_{TH} + \left(\frac{R_2}{R_1}\right) \cdot V_{OS} \quad (3)$$

Another factor that also degrades the accuracy of the reference voltage is the noise generated by integrated devices and from supply lines. In respect of the noise generated by the devices, the most contribution (in the BGR architecture showed in fig. 1) comes from the op-amp devices, as demonstrated in [13]. This happen because the input-referred noise appears in the output voltage amplified by the closed-loop gain. Therefore, the op-amp design deserves attention to reduce the noise. Moreover, to reduce the noise from supply lines, it is also desired to have BGRs with high power-supply rejection ratio (PSRR) [8].

As discussed above, the op-amp places a critical role in the performance of the BGR, for instance, in terms of DC errors (V_{OS}) and output noise voltage. Therefore, it is important to know the impact of different op-amp architectures in the BGR performance. If the adequate op-amp is chosen for one BGR specification, the error in V_{REF} caused by noise or V_{OS} can be reduced. The next section discusses four types of op-amps frequently employed in the BGR design.

3. INPLEMENTED AMPLIFIERS

This section starts with discussion about the requirements of the op-amp used in the BGR of figure 1. After this, each amplifier topology is analyzed separately and some design guidelines are presented.

The first and probably the most important requirement is the DC open-loop gain. Ideally it is desired that the op-amp has infinite DC open-loop gain, and in such way, the two nodes “a” and “b” are exactly equal. In this ideal case, the current I will be exactly given by equation (1) and its TC will be proportional to the absolute temperature if one neglects the resistor TC and V_{OS}.

However, in fact the gain is not infinite and exist an error ε_A between the two inputs. The well known op-amp behavior is defined by $V_0/A_0 = (V_P - V_M) = \varepsilon_A$; where A_O is the open-loop gain; V_P and V_M are the positive and negative input respectively. Note that how big is A_0, less will be the error ε_A. This error will be also propagated to the output amplified by R_2 over R_1, - similarly to the V_{OS} – and for this reason, it should be reduced. Gains A_0 in the order of 50 dB are enough to guarantee good temperature compensation [15].

It is also relevant to add that the total error (ε_T) between the V_P and V_M will be the addition between the offset voltage and εA (due to finite gain). The total error must be smaller than ΔV_{BE}. In different way, the TC of current I will be severely damaged and this will result in V_{REF} with poor temperature performance.

In respect of the common mode input range (CMIR), as one can see in figure 1, the voltage in the input terminals of the op-amp are equal to V_{BE} for a given current. For example, for I equal to 50 µA, the V_{BE} of the parasitic vertical bipolar transistor of IBM 0.18 µm CMOS technology varies approximately from 0.6 V to 0.85V, in the military temperature range of operation (-55 to 125°C). Such variation is equivalent to a TC ≈ 1.5 mV/°C. Nevertheless, these values depend on type of parasitic BJT and the technology used. It is possible that for another technology, where the BJT has large emitter area, the value of V_{BE} be smaller than 0.6 volts at 125 °C. In this case, the CMIR requirement will make difficult to accommodate a n-channel input differential stage; if any level shift does not be used.

In respect of the output swing, the op-amp should provide the output (V_O) not bigger than VDD – V_{TP}, to keep the current source transistors (M_1 and M_2) on; where V_{TP} is the PMOS threshold voltage. Once the drain-source voltage (V_{DS}) of these devices is equal to VDD – V_{REF}, the amplifier output should be bigger than $V_{REF} - V_{TP}$ to ensure M1 and M2 in saturation.

In literature is usually presented that the op-amp used in BGR´s has not bandwidth constraints [2]. However, sometimes the output of the amplifier is used to bias other circuits in the system [1], and in this case, it is need to increase the op-amp speed (at cost of power consumption) to avoid large transient changes in V_{REF}.

Another desired feature that was already commented in section 2 is the PSRR. It is not only desired to have high values of PSRR at DC, but also over the whole bandwidth in which the application that uses V_{REF} is operating. Once this robustness against the noise from supply lines are strongly depend on the amplifier design, consequently it is important to choose the best op-amp architecture when the noise coming from the supply is a problem. Besides of the careful op-amp design, there are also

others techniques used to increase the PSRR of the Bandgap reference [8].

To end, it was already discussed that the offset voltage is the biggest error source in the BGR circuit. Therefore, one fundamental recommendation for the input stage is to design devices with big sizes and with a common centroid configuration layout, decreasing in this way, the random offset voltage.

3.1. Amplifier 1: OTA

The simplest amplifier that can be used in the BGR design is the operational transconductance amplifier (OTA) - shown in figure 1. In work [5] it is stated that the use of this amplifier architecture is an excellent choice because there are only two pairs of matched devices to consider on the random offset voltage. Moreover, as the number of devices in this amplifier is small, lower is the number of error sources (mismatching and noise) presented in the circuit.

For this 0.18 IBM CMOS technology it is possible to design both n-input and p-input OTA. The minimum value of the common-mode voltage (VCM) for the n-input version amplifier is $V_{CMMIN} = V_{GS\_Input} + V_{DSsat\_Isource}$; where the first term is the gate-source voltage of the input transistor and the second one is the overdrive voltage of the current source transistor. Nevertheless, as already commented, in some cases may be difficult to keep the current source transistors in saturation mode.

The gain provided by this amplifier is given approximately by $gm_{P1}*(ro_{P2}//ro_{N2})$. Thus, to achieve high gain the only solution is to increase the output resistance, what means use very low currents, in the order of few µA, and big channel lengths devices (around 30 times the minimum channel length of the used technology). The transistor output resistance is inversely proportional to the drain-source current. Following these recommendations, it is possible to achieve the desired 50 dB of open-loop gain.

Once small current are needed to achieve the required gain, this amplifier is slow. Hence it is desired to avoid connection between the amplifier output and nodes that are heavily disturbed.

In respect of the offset voltage and the noise generated by integrated devices, one recommendation that must be followed is to reduce the ratio of gm_{LOAD}/gm_{INPUT}; that is, the transconductance of load devices must be much smaller than that of input [1]. Doing this the noise and offset error gain to the output is reduced. Moreover, since the transistor area is inversely proportional to the mismatching and flicker noise, the input and load devices must be design with big areas. This recommendation should be follow in any topology amplifier.

The last comment in this sub-section is about the stability of the BGR using OTA amplifier. Since there are positive and negative feedbacks, compensation capacitor is needed to guarantee the stability. According to work [5], the best approach to ensure stability is to insert a compensation capacitor between V_O and op-amp positive input. Small sizes are enough due to the Miller multiplication effect.

3.2. Amplifier 2: Symmetrical OTA

Another type of error-amplifier that is frequently used is the symmetrical OTA shown in figure 1. Accordingly to work [4], this op-amp presents less systematic offset, since the two input transistors have the same load (a diode-connected transistor) and the same V_{DS} voltage.

The gain in this configuration is approximately given by $K*gm_{P1}*(ro_{P4}//ro_{N4})$, where K is the current ratio between the output and the input branch. Due to the factor K, this circuit can achieve gains a little bit bigger than the simple OTA.

One artifact to avoid the bias circuitry for the amplifier and also helps the stabilization of this circuit [4], it is to mirror the current of the BGR to bias the own amplifier. In summary, all recommendations given in section 3.1 are also valid here.

3.3. Amplifier 3: Two-Stage Miller

The typical two-stage Miller amplifier is also used in the design of BGR´s. As the gain of this topology is approximately given by $gm_{P1}* gm_{N3}* (ro_{P2}//ro_{N2})* (ro_{P4}//ro_{N3})$, it is easy to achieve high gains. As consequence of high gain, the first impact in the BGR performance is the reduced εA error. As already discussed, this error tends to damage the temperature performance of V_{REF}. The second impact is the bigger PSRR (at low frequency) achieved. The power supply rejection at low frequency is directly proportional to the open-loop gain [1]. Nevertheless, the bandwidth of the PSRR decreases with open-loop gain. Another solution to further increase PSRR, is to use the transistor P4 (figure 1, item (c), dashed line) in a diode connection [6]. With this modification, no extra pin is required for current bias and higher PSRR is achieved at the cost of lower voltage gain.

In respect of stability, this op-amp has its own Miller compensation capacitor, what defines the dominant pole. Accordingly no capacitors must be connected in the amplifier output, like the case of the BGR using OTA amplifier.

The speed of this op-amp can be configured as desired, once even with high-currents, high open-loop gain is achieved. If it is more important to reduce power consumption than speed performance, the compensation capacitor can be increased to guarantee good phase margin while the second stages has low currents. At end, for its input stage, the recommendations presented in section 3.1, are also valid.

3.4. Amplifier 4: Folded-Cascode

The last type of amplifier analyzed in this section is the folded-cascode. The gain achieved by this circuit is defined by gm_1*RO, where RO is given by $[gm_{N4}*ro_{N4}*ro_{N2}]//(gm_{P6}*ro_{P6}*(ro_{P2}//ro_{P4})$ [1]. To achieve high gain and PSRR, the output resistance seen by the output node must be big; what means big sizes of transistor channel length.

Extra pin for bias current can also be avoided if the PTAT current from BGR is mirror to the amplifier. In respect of stability, the BGR using this amplifier also need a compensation capacitor connected between the amplifier output and the positive input.

4. RESULTS

Following the recommendations listed in previous sessions, it was designed one BGR using the four discussed amplifiers. After this, the performance achieved by the BGR using each amplifier was investigated. Temperature coefficient, line regulation, the susceptibility to the fabrication process effects, and robustness against the noise (generated by integrated devices and from the supply lines) were studied for each case. Table 2 presents the first part of these results, and table 3 shows the impact of the variability.

The reference voltage variation over the temperature variation (ΔV_{REF_TEMP}) was measured in the range of -55 to 125 °C. The line regulation performance or output voltage variation

over VDD fluctuation (ΔV_{REF_VDD}) was measured considering VDD variation of 1.7 to 1.9 V. In addition, the impact of the noise (generated by integrated devices) on the reference voltage (ΔV_{REF_NOISE}) was estimated to be three times the RMS output noise integrated over a bandwidth of 10MHz – that is much more than the noise corner frequency [13].

As can be seen in table 2, the ideal value of the V_{REF} is practically equal to the Bandgap silicon voltage for all cases as we expected. The ideal temperature performance is also equal for all cases and its value is about 20 ppm/°C. All TC are equal because in all cases only the first order term of V_{BE} is temperature compensated.

The best performance in terms of noise generated by the integrated devices is the BGR using OTA amplifier. Although the recommendation to reduce the ratio of gm_{LOAD}/gm_{INPUT} was followed in all amplifiers, the reduced number o devices and the smallest open-loop gain make this topology less noisily.

However, in respect of noise from the supply voltage, the OTA op-amp is less efficient, while the folded-cascode presents the best performance. Due to the biggest output resistance in the folded-cascode op-amp, the impact of the supply noise at the output is reduced.

Parameter	*Amp1*	*Amp2*	*Amp3*	*Amp4*
Vref(V)	*1.179*	*1.172*	*1.169*	*1.170*
ΔV_{REF_TEMP}(mV)	*2.0*	*2.1*	*2.1*	*2.2*
ΔV_{REF_VDD}(mV)	*3.4*	*0.30*	*0.28*	*0.2*
ΔV_{REF_NOISE}(µV)	*801*	*1032*	*1902*	*1200*
PSRR(Min)(dB)	*25*	*25*	*20*	*23*
PSRR@DC(dB)	*34*	*69*	*70*	*80*

Table 2. Performance parameters of the BGR

Parameter	*Amp1*	*Amp2*	*Amp3*	*Amp4*
m: V_{REF} (V)	*1.179*	*1.173*	*1.171*	*1.174*
σ: V_{REF} (mV)	*6.89*	*8.60*	*18.86*	*16.01*
m: ΔV_{REF_TEMP} (mV)	*3.18*	*3.66*	*4.02*	*6.03*
σ: ΔV_{REF_TEMP} (mV)	*1.67*	*1.58*	*2.01*	*2.80*

Table 3. Impact of the variability

Another comparison that can be done is in respect of the susceptibility to the fabrication process effects. This is realized through Monte Carlo analysis including Mismatch and process variations. The number of sample used was five hundred and two parameters were analyzed. The value of the output voltage and the temperature performance were both investigated to verify the degradation caused by the variability. Table 2 presents these data, where "m" and σ stand for mean and sigma respectively.

As can be seen in table 3, the OTA version presents a small value of sigma for V_{REF}, and consequently, the smallest degradation in ΔV_{REF_TEMP}. But even in this case, TC of the BGR fabricated may be in the order of 80 ppm/°C, what represents a poor performance. For some applications maybe it will be needed to trim the output voltage. But comparing the four amplifier possibilities, trimming V_{REF} of the BGR using the simple OTA it will require reduced trim range (number of bits), thus resulting in less area overhead and reduced test time.

5. CONCLUSIONS

This work presents an investigation about the impact of different op-amps used in a typical Bandgap voltage reference. The amplifier topologies: OTA, Symmetrical OTA, two-stage Miller and folded-cascode were compared from the Bandgap reference point of view. From this analysis, it is possible to verify which amplifier architecture is adequate for each Bandgap specification. For example, BGR using OTA amplifier is less susceptible to the fabrication process effects. Moreover, several design guidelines were provided to help the design of op-amps focusing in BGR´s.

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