A PHASE AND FREQUENCY DETECTOR AND CHARGE PUMP FOR LOCAL OSCILLATOR IN A ZIGBEE TRANSCEIVER

Guilherme Mauch de Freitas, Sergio Bampi
{gmfreitas, bampi}@inf.ufrgs.br

PGMICRO – Graduate Program on Microelectronics at Federal University of Rio Grande do Sul – Porto Alegre – Brasil

ABSTRACT

This paper describes the design, layout and simulation of a phase and frequency detector, based on D flip-flops, and a charge pump. The circuits were designed using Cadence 90nm CMOS process, with 1.2V of power supply, and follow the actual techniques to improve the performance and reduce the power consumption. These blocks are employed in an integer-N frequency synthesizer responsible by the synchronization of a 900MHz ZigBee transceiver. The results of simulations were obtained, with layout extracted view, considering the parasitic resistance and capacitance. The design, layout and simulations were made in the software tools provided by Cadence Design Systems.

1. INTRODUCTION

The frequency synthesizers are employed in an ever-wider variety of electronic products to generate any one of a number of operating frequencies [1]. The output frequency is determined by a programmable frequency divider, at the feedback loop. The most used method for the synthesis is based on Phase-Locked Loop (PLL) techniques, because they have excellent performance and can be totally integrated on the same chip. In this work, the frequency synthesizer provides the local oscillator (LO) signal for transmit and receive modes. The frequency synthesizer needs to change frequency in going from transmit to receive. This synthesizer is a part of a 900 MHz ZigBee transceiver, the block diagram is depicted in Figure 1.

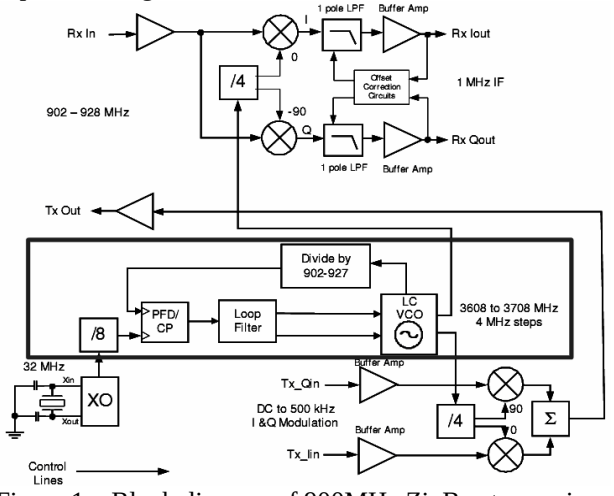

Figure 1 – Block diagram of 900MHz ZigBee transceiver.

The loop consists of a phase and frequency detector (PFD), charge pump (CP), an on-chip loop filter (LPF), a LC voltage controlled oscillator (VCO), an integer-N feedback divider, reference divider and a 32 MHz crystal oscillator circuit with external CMOS input drive capability.

The synthesizer was designed in Cadence 90nm CMOS process, with 1.2V of power supply. And was used a direct-conversion, as showed in Figure 1. This architecture directly down-converts the radiofrequency (RF) signal to baseband (BB) and the low-pass filters are used to realize the channel selection.

2. PHASE AND FREQUENCY DETECTOR

The purpose of the phase detector is to produce a signal that is proportional to the difference in phase between two signals, namely the reference frequency (F_{REF}) and the divided frequency (F_{DIV}) from the VCO. There are several types of phase detectors, the most popular for frequency synthesizer applications is the phase and frequency detector (PFD) [1].

The PFD implemented in this work was based on modified D flip-flops [4], as showed in Figure 2. The output of this type of architecture depends not only on the phase difference, but on the frequency difference between reference and divided frequencies. The outputs of D flip-flops are labeled UP and DWN, since there are two outputs, four different states are possible. The operation of the PFD requires only three states, so one is left unused. The PFD is designed such that when the fourth state is reached, the AND gate resets the outputs to a valid state. This tri-state architecture is edge-triggered, which makes it duty cycle insensitive. To eliminate the dead-zone and guarantee that the PFD can detect all the differences of phase and frequency, are putted delay cells on the reset flow.

In the Figure 3 is showed a result of simulation when the divided frequency from the VCO is leading reference frequency by 50ns. In this case, the DWN output of the PFD goes to high level and charge is extracted from the loop filter, which decreases the control voltage of the VCO, reducing its output frequency. Then the frequency reduction in the VCO reduces the phase difference between divided frequency and reference frequency. The opposite happens when the divided frequency input lags the reference frequency input.

When the phase and frequency of both inputs are the same, the synthesizer is in lock state. The AND gate detects that both inputs are high, which is the fourth and undesired state, and resets both outputs. This generates small pulses at both outputs of the PFD.

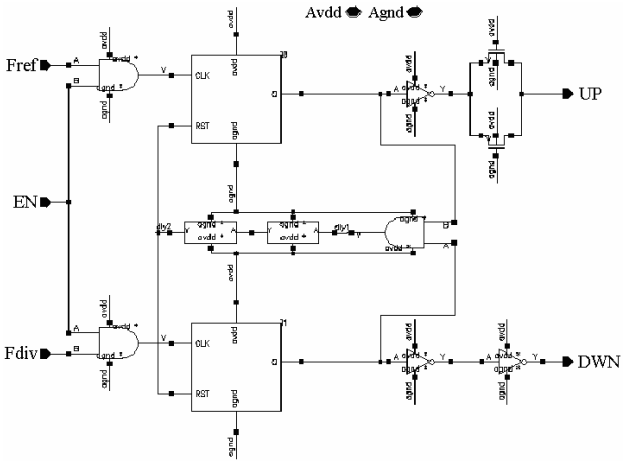

Figure 2 – Phase and frequency detector.

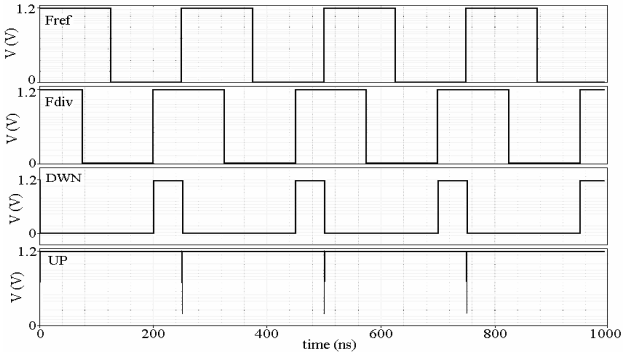

Figure 3 – F_{DIV} is leading F_{REF} by 50ns.

Since the PFD is a digital circuit we can use automatic tools to make the layout. In this work the cells was positioned manually and the connections was made automatically. Then we obtained a very compact layout with 33.78um by 5.88um of dimension, as showed in the Figure 4.

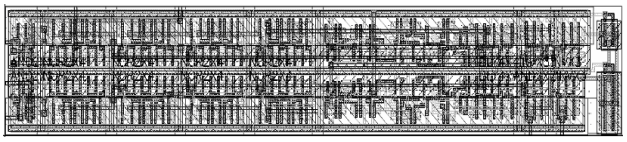

Figure 4 – Layout of phase and frequency detector.

3. CHARGE PUMP

In general, the charge pump (CP) is composed of two current sources that are switched by the control signals coming from the PFD. The amount of charge delivered from the loop filter necessary to achieve and maintain loop lock is determined by the time the current source/sink are turned on and off to set a proper voltage in the control terminal of the VCO. The CP receive a 50uA bias current become from another block, and reduced to 30uA to be injected or extracted from the loop filter through the current mirrors, as showed in the Figure 5.

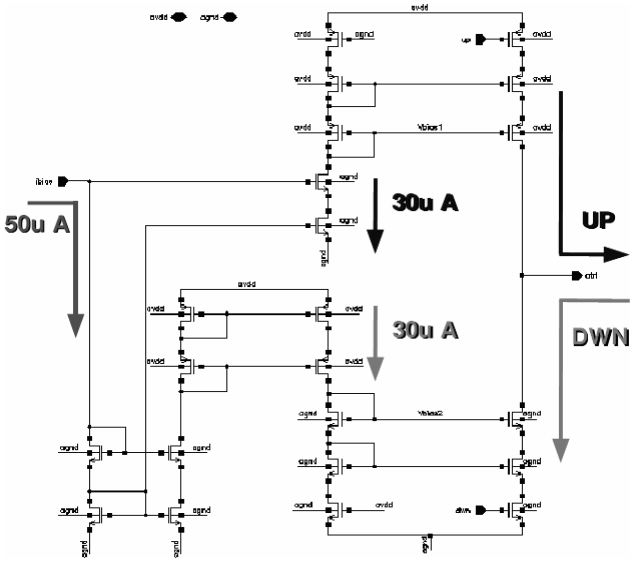

Figure 5 – Charge pump.

In this circuit is used a cascade current mirrors to reduce the mismatch errors in the charge pump. Mismatch in the current sources leads to an unwanted amount of charge that is injected in the loop filter every reference cycle. The result of UP and DWN current DC simulation is showed in the Figure 6, and is proved that with this architecture we have a minimum current mismatch, less than 1%, between the charge and discharge of loop filter. This behavior allows a very high precision on the VCO control voltage. When the loop is lock, the noise of the current sources of the CP is only injected into the loop filter during the small pulses generated by the PFD to eliminate the dead-zone.

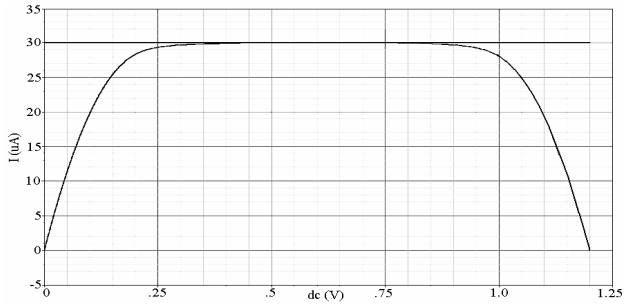

Figure 6 – UP and DWN current at the output of CP.

The layout of analog blocks requires a careful design, position, orientation, and connections of transistors. Specially, in the CP, needs a great attention on the layout of current mirrors, to minimize the effects of mismatch. In this work, we use the common-centroid technique on the current mirrors layout, to have almost the same current flowing in the different branches of circuit. In the Figure 7 is showed, in detail, the layout of one NMOS transistor pair, with common-centroid, to implement a current mirror.

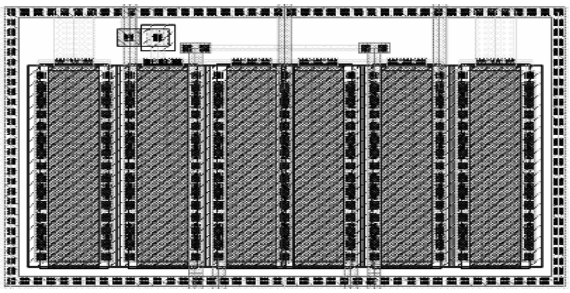

Figure 7 – NMOS current mirror.

The layout of CP was totally made with common-centroid technique, and using a guard-ring for each transistor pair. It reduces the interference of other blocks, especially digital blocks with much switch activity. To minimize the process effects and reduce the risk of gate rupture, is used an antenna diode connect between the gate of transistor and power supply. Then the circuit has a flow to discharge the electric charge that is accumulated during the fabrication process. Also is used dummy transistor at the side of first and last active transistor. The entire layout of CP has 36.59um by 41.97um of dimension, and is showed below in the Figure 8.

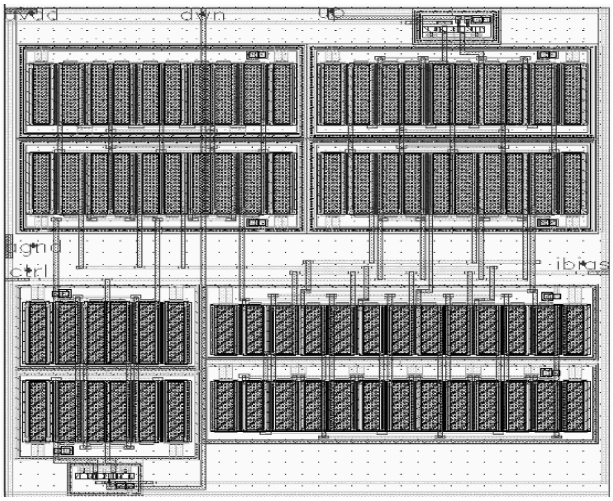

Figure 8 – Layout of charge pump.

4. RESULTS

To be possible the entire loop simulation of the frequency synthesizer, we need to have at least the PFD, CP, LPF, VCO and divider. Since we have the electrical specifications, we can describe the behavior of other blocks, with more high level language. For this, was used the Verilog-A language to describe the VCO and the loop divider. The loop filter was dimensioned with the mathematic tool help.

The result of closed loop simulation is showed in the Figure 9. The settling time for this PLL is less than 30us, it is very fast and much better than was specified. In the Figure 10 is depicted the maximum ripple after the filter, with 3.4uV of amplitude. Consequently the spurious level attenuation at the VCO output is very high, as showed in the Figure 11. In this case, we achieve -80 dBc/Hz.

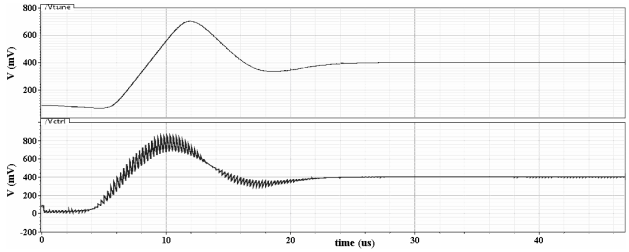

Figure 9 – Closed loop simulation.

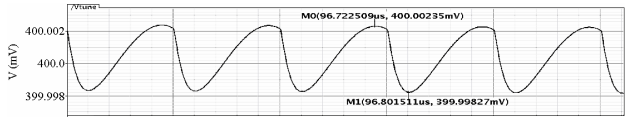

Figure 10 – Ripple at the loop filter output.

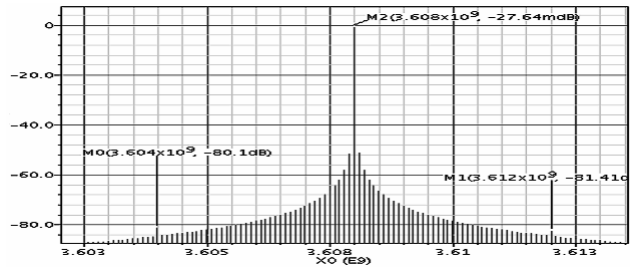

Figure 11 – Spurious level at the VCO output.

5. CONCLUSIONS

This work enriches the knowledge about frequency synthesizer and their challenges, because is used in a real application with commercial specifications. The design and layout of frequency synthesizer, to synchronization of a 900MHz ZigBee transceiver, has been realized with a 90nm CMOS technology. The PFD was designed to detect all the phase and frequency differences, without dead-zone. Since was implemented with a modified D flip-flop, using only four NOR gates, the PFD area is very small, about 200um^2. The reduced current mismatch in the CP, makes the settling time and the noise very low, 30us and -80dBc/Hz respectively, in the entire closed loop. The frequency synthesizer occupies an area of 0.62mm^2 and draws 14.6mA from a 1.2V power supply.

10. REFERENCES

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