ANALYSIS OF POWER CONSUMPTION USING A NEW METHODOLOGY FOR THE CAPACITANCE MODELING OF COMPLEX LOGIC GATES WITH DOGBONE TRANSISTOR

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ABSTRACT

This study presents a proposal to estimate the power consumption of the complex logic gate with topology dogbone transistors, which reduces the effects of radiation, by of the estimate of input and output capacitance of gate. The simulation tools have been implementation and SIS and comparator with the Hspice Synopsys. The first results show approximately an error of 5% between the proposed and simulated method.

1. INTRODUCTION

The development of new technologies in the recent years has made decrease the channel of the CMOS transistor, and the effect of ionizing radiation (eg alpha, beta, neutron) passed to have great influence in its operation. This resulted in the appearance of some problems that were only found in the circuits used in space, but started to appear and cause failure of operation or even damage electronic circuits not protected against the effects of ionization radiation. Considering the degrading effect that radiation has on CMOS integrated circuits shall require the use of technology to manufacture specially developed to reduce these effects [4]. Some processes and structures for shielding entail additional costs and end up limiting their use because of weight and size that prevents the implementation cost. Thus, it is necessary to provide new layout of the circuit topologies. The optimization of delay and power consumption has also been a very relevant and integrated circuits. With the development of new anti-radiation topologies it is necessary to have mechanisms to build ever smaller devices with maximum performance [8]. Thus it is essential that new studies for design of transistors for optimizing delay and power consumption be made to accommodate those new processes.

This paper proposes the analysis of the power consumption in complex logic gates (SCCG) with topology dogbone at the logic level, by means of using a new methodology of capacitance modeling.

This methodology considers a mathematic model of equivalent concentrated capacitance in each external node of the gate. This model analyzes all the possible combinations of transitions at the gate inputs and their capacitive effects. In the present work, the capacitances of interconnections and crosstalk are yet disregarded.

The paper is divided in the following parts: in section II presents a review of anti-radiation circuits, in section III presents the methodology applied in the analysis of the topology of the construction of gates, while in unit IV presents the results and finally, in section V presents the conclusions related to work.

2. TOPOLOGY OF TRANSISTORS RADIATION-HARDENED

In recent years several techniques have been proposed for layout, but it cannot eliminate the damage, significantly reduces the effects caused by radiation [1] and [2]. Devices designed using these techniques are called resistant to radiation (Radiation-Hardened) [3], [4] and [5].

There are manufacturing processes completely immune to radiation effects. But there are those that are less susceptible to such phenomena as the processes SOI (Silicon-On-Insulator). There are also cases where sub-micron layer of oxide on the already thin transistors, provides greater resistance to the accumulation of charges. Some techniques for solving the layout problem by looking for structures geometrically designed to naturally ease the physical processes corresponding to the effects of radiation.

When a transistor is exposed to the radioactive effects accumulates some charges in the oxide. These accumulations of charges in the oxide do not occur only

on the channel of the transistor, but in every area of the circuit. This effect causes changes in the characteristics of the circuit devices may lead to changes in the operation of the circuit. Some of these changes can be very difficult to set without the completion of extensive simulations. In some cases, changes can be so severe that the circuit or parts of them may stop working or do so only at lower frequencies of operation [5]. Each circuit responds in a different way to a given condition of radiation, as are the design of the circuit and the intrinsic behavior of devices manufactured in the corresponding technology [7].

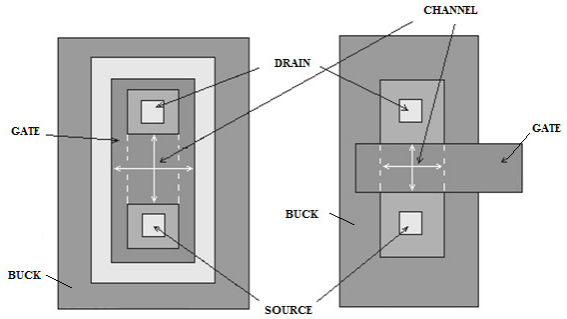

Figure 1. Channel de conduction: dogbone and transistor conventional [8].

In the dogbone transistors of the Figure 1 the region of p+ diffusion that restricts the device eliminates the influence of the thick oxide in the width of the device. However, according CARNEIRO [8], the p+ implant can spread it on the terminal gate and interact with the substrate p on it, changing the effective width of the transistor.

The dogbone topology was chosen for study because their immunity to radiation and the possibility to be used in the construction of complex logic gates.

3. PROPOSED METHODOLOGY

The model proposed for the power estimation of complex logic gates estimates the intrinsic capacitances of each dogbone transistor through the linear model and dimensions of design: width (W) and length (L) of the channel[8]. These capacitances are concentrated in the external nodes of the logic gate, being computed using a mathematical model that considers the effect of all possible transitions of input vectors for the considered input. One similar idea was used and for standard gates CMOS with promising results[9], [10] and [11]. It now is necessary to analyzer other parameters, due the different structure of the dogbone transistor.

The dynamic power of static CMOS circuits is defined in equation (1) as:

$$P_{dyn} = \frac{1}{2}.f_c.V_{dd}^2.\sum_{i=1}^{n} C_i.\alpha_i \qquad (1)$$

Where: P_{dyn} is the dynamic power consumed by the circuit, f_c the clock frequency, V_{dd} is the voltage of the circuit, n the total number of gates of the circuit, C_i the equivalent capacitance of node i and α_i the switching activity of each gate.

The models of dogbone transistors are considered linear. The complex logic gate dogbone analyzed is AOI21.

3.1. Modeling of complex gate AOI21

The complex logic gate AOI21 with topology dogbone transistor that realizes the logical function of equation (2), has 6 external nodes and 2 internal nodes, as demonstrated in Figure 2(a).

$$X = \overline{AB + C} \qquad (2)$$

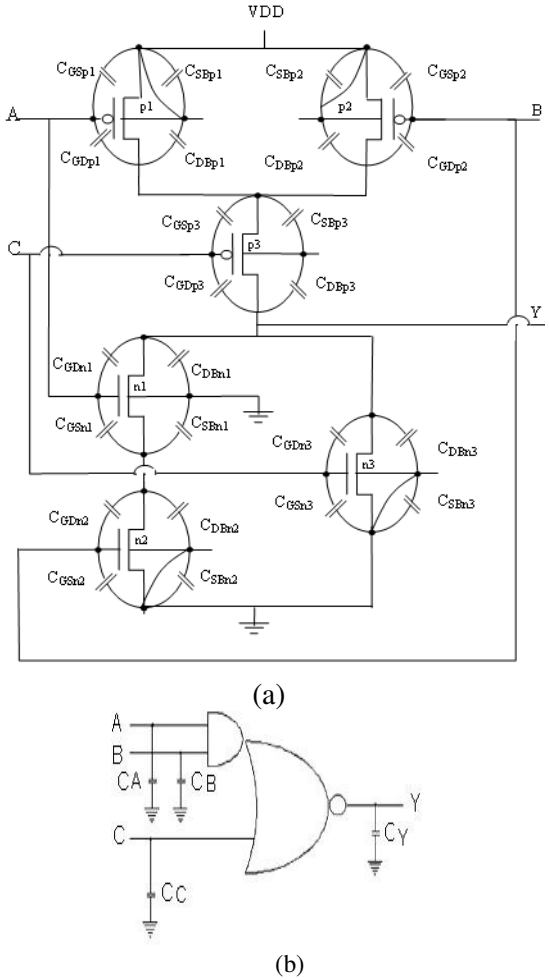

Figure 2. Complex gate AOI21: a) Model with intrinsic capacitances; b) Logic Model with concentrated capacitances.

Where $C_{GD(n,p)}$, $C_{DB(n,p)}$, $C_{GS(n,p)}$ and $C_{S,B(n,p)}$ are defined respectively as gate-drain capacitance, drain-bulk capacitance, gate-source capacitance and source-bulk capacitance of the transistor n(p). C_{JB}, it is capacitance of shielding which depends the switching activity.

The three inputs of the gate allow the pairwise combination of input vectors **000, 001, 010, 011, 100,**

101, 110 and **111** and that they act in the transistors switching PMOS and NMOS, resulting in the equivalent capacitance. However, the equivalent capacitance of each internal node is determined by the effect of the transition of the signals (external and internal) related to the node analyzed; the number of capacitive components is equal to the number of analyzed vectors. In this way, the number of components is reduced to 4, as in equation (3):

$$C_n = C_1 + C_2 + C_3 + C_4 \quad (3)$$

Where C_n is the equivalent capacitance of the node being analyzed and $C_1....C_4$, are the capacitances due to the transition of the input states.

3.1.1. Equivalent capacitance model for input A

In the analysis of the equivalent capacitance of the input A of the SCCG AOI21, it is verified the transition of input B and C. From the equation (3) above, the C_1 component is the capacitance due to the signals of input 0**00** and 1**00**, C_2 is the resulting capacitive component of the transition of signals 0**01** and 1**01**, C_3 is the capacitive component which had signals 0**10** and 1**10** and C_4 resulting of signals 1**11** and 0**11** is the capacitive component.

Therefore, C_A is:

$$C_A = C_{AX1} + C_{AX2} + C_{AX3} + C_{AX4} \quad (4)$$

C_{AX1} corresponds to the signals of input 0**00** and 1**00** where the transistors *n2* and *n3* of Figure 1, are in OFF state whereas the transistors type *p2* and *p3* are in conduction. In such a way C_{AX1}:

$$C_{Ax1} = 0{,}25\left(\frac{C_{GSn1}.C_{TAx1}}{C_{GSn1}+C_{TAx1}} + C_{GDn1} + C_{GDp1} + C_{GSp1} + C_{JB}\right) \quad (5)$$

Where C_{TAx1} is:

$$C_{TAx1} = C_{GDn2} + C_{DBn2} + C_{SBn1}$$

C_{AX2} corresponds to the input signals 0**01** and 1**01** where the transistors *n2* and *p3* are in OFF state, and the transistors *n3* and *p2*are in conduction, what results in the capacitive part of C_{AX2}:

$$C_{Ax2} = 0{,}25\left(\frac{C_{GSn1}.C_{TAx2}}{C_{GSn1}+C_{TAx2}} + C_{GDn1} + C_{GSp1} + \frac{C_{GDp1}.C_{TAX2}}{C_{GDp1}+C_{TAX2}} + C_{JB}\right) \quad (6)$$

Where C_{TA21} is:

$$C_{TAx2} = C_{SBp3} + C_{GDp3} + C_{SBp1}$$

The transistors n2 and p3 enter in conduction and the transistors p2 and n3 in OFF state for the excitement of input 110 and 010. Thus the capacitive component for these vectors of input results in C_{AX3}:

$$C_{Ax3} = 0{,}25\left(C_{GSn1} + C_{GDn1} + C_{GDp1} + C_{GSp1} + C_{JB}\right) \quad (7)$$

Finally, when the signals equal 011 and 111 transistors n2 and n3 enter in conduction and the transistors p2 and p3 enter in OFF state, what results in C_{AX4} equal to:

$$C_{Ax4} = 0{,}25\left(\frac{C_{GDp1}.C_{TAx4}}{C_{GDp1}+C_{TAx4}} + C_{GDn1} + C_{GSn1} + C_{GSp1} + C_{JB}\right) \quad (8)$$

Where C_{Tax4} is:

$$C_{TAx4} = C_{GDp2} + C_{DBp1} + C_{SBp3} + C_{DBp3} + C_{GDp2}$$

For the B, C, inputs and Y output the same analysis is made in terms of the influence for the combinations of the input vectors in the transistors.

4. RESULTS THE SIMULATIONS

This section presents the simulations with results of the power consumption and the CPU time, using the proposed methodology integrated into the SIS tools [13]. The results of power estimation consumption at logical level are compared to the electric level through the Hspice of the Synopsys [14]. All the simulations have been performed in a PC Pentium IV, 3 GHz processor and 1GB of RAM. The parameters of technology used were from the AMS08. The circuits were simulated with 5V voltage, frequency of 20MHz and 50, 100 and 150 input vectors.

In Figure 3 it is presented the flow of analysis for simulation:

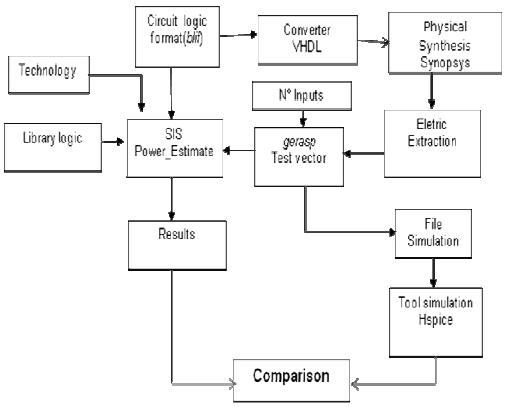

Figure 3. Flow of Simulation.

In the table 1 are presents the results of the simulations of power estimation.

Table 1. Power consumption estimation of SCCG with electric parameters AMS08.

Vectors	*Power SIS (μW)*	*CPU (s)*	*Power Hspice (μW)*	*CPU (s)*	*Error (%)*
50	0.660	0.14	0.691	10.6	4,6
100	0,857	0,18	0,899	14,6	4,9
150	1,220	0,23	1,268	19,3	3,9

5. CONCLUSIONS AND FUTURE WORKS

The method of power consumption estimation using the modeling of the capacitance that computes the equivalent concentrated capacitance to external nodes of each logic gate obtained in the logical level present an error smaller than 5% in comparison with the obtained in the electric level for the considered circuits, with the advantage of the simulations being faster. Considering the analysis of the proposed method, which yet does not consider information of interconnection capacitances and crosstalk, the results were quite satisfactory.

The next step is to test the methodology in others complex gates and mainly different technologies, as DSM, for developing a tool of power estimation of circuits with dogbone transistors.

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