DESIGN OF AN ANALOG-TO-DIGITAL CONVERTER

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ABSTRACT

This paper describes the development of a ten-bit successive-approximation ADC. This type of converter comprises many internal blocks, such as: a digital-to-analog converter (DAC), a successive-approximation register (SAR), an analog comparator, and a sample-and-hold circuit (S/H). Each block was developed and simulated in (ELDO and ADMS from Mentor Graphics). The ADC design was implemented in 0.5 micron CMOS technology and the simulation results show the performance of the converter and the specifications achieved are presented.

1. INTRODUCTION

Electrical signals from sensors are often processed by digital circuits, as this signals are of analog nature it is necessary the use of A/D converters. The most important goals in ADC design are conversion time, linearity, and resolution. There is a great need for A/D converters in the medium resolution range (10-14 bits) for communication systems, and others applications [2].

There are many techniques used for A/D conversion, among them the successive approximation [3], [4], described in section 2. One of the main advantages of this technique is the speed at which the circuit performs the signal conversion. In the worst case it will find the correct digital value for the sample in n^{th} clock pulse, where 'n' is the number of bits used.

This paper describes the implementation of an A/D converter of 10 bits using the technique of successive approximations. It was written by students of the third and fourth year of electrical engineering undergraduate, participants of the Brazil-IP program, sponsored by CNPq.

2. GENERAL DESCRIPTION OF THE ADC

The ten-bit successive-approximation ADC designed has four main internal blocks: a digital-to-analog converter (DAC), a successive-approximation register (SAR), an analog comparator, and a sample-and-hold circuit (S/H). In the technique of successive approximation, an algorithm is used to convert analog input into digital. This algorithm sets the most significant bit (MSB) to 1 and all other bits to 0, performed by register. The comparator evaluates the output of the DAC with the sampled analog input signal. The SAR keeps updating the digital values, from MSB to least significant bit (LSB), until it approaches the desired output. The block diagram of the converter can be seen in Figure 1.

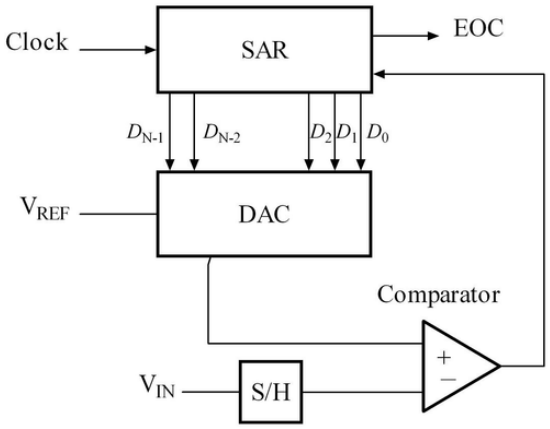

Figure 1: Successive-Approximation ADC Block Diagram

According to Nyquist's theorem, the frequency of the sampled signal must be twice smaller than the sampling frequency. Thus, the clock frequency must be at least equal to 20 times of the maximum input signal's frequency and are necessary a total of 10 clock pulses to perform the complete signal conversion. The detailed performance of each block, as well as its architecture is described below. Table 1 identifies the specific design.

Table 1
A/D Converter Characteristics

Process	0.5μm CMOS
Resolution	10 bits
Conversion time	5μs
DNL	± 1 LSB
INL	± 1 LSB
Offset error	± 1 LSB

2.1. SAR

The SAR must send a digital value of "1000000000" (512 in decimal) to the DAC at the beginning of each conversion. At each clock step, the SAR must update the current bit accordingly to the value obtained from the comparator (1 or 0), select the next bit to be "1" and send as a new guess to the DAC. The bits are selected from MSB to LSB. After ten clock pulses, the SAR must update the ADC output with the last obtained values and start another conversion, sending the initial guess to the DAC. The register was written in Verilog, and prototyped in a FPGA (Field Programmable Gate Array) board for evaluation purposes.

2.2. DAC

The DAC has as main function to convert the digital signal stored in the register and provide a corresponding analog signal to the comparator, starting a new cycle in the successive approximation process. The DAC has 10 bits and must perform the conversion in the same voltage range of the ADC.

In the choice of the D/A converter architecture was taken into account the area of silicon that the converter will hold on the chip. Then, C-2C architecture was chosen and can be seen in Figure 2. This architecture uses capacitors to perform the division of the reference voltage in weighted parts, unlike of the architecture of redistribution charges that is often used in the implementation of D/A converters with the capacitors [6].

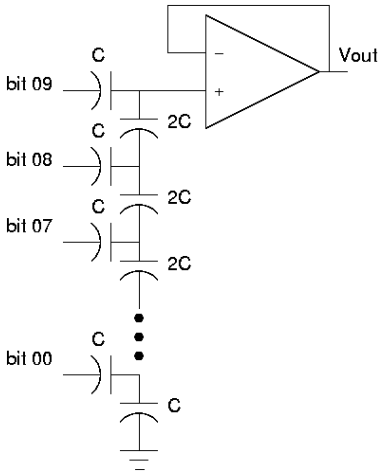

Figure 2 – C-2C 10 bits digital-to-analog converter

This architecture does not require that the last capacitor be 1024 times greater than the first, because the C-2C converter uses the same logic that the R-2R DAC [7], where a combination of series and parallels capacitors are used for conversion. Then, if a capacitance C is used, the maximum value of capacitance in the circuit would be 2C, thereby reducing the area used.

2.3 Comparator

In the A/D converter design, the signal to be converted is sampled and introduced in one of the inputs of the comparator. The other input is provided by the D/A converter. The output of the comparator at logical level high or low will be delivered to the register (SAR) which will provide the new word to the D/A converter. After 10 cycles of comparison, the register will have stored a word whose digital value refers to the analog input.

The architecture of the comparator was determined through the input voltage range parameter. The comparator of the converter circuit should be able to receive inputs ranging from 0 to 5 Volts, i.e., VSS to VDD. Standard topologies use a differential pair of NMOS transistors (or PMOS) at the input stage, seen in figure 3. However, it is necessary that a minimum of Vgs – 2Vt (or maximum of VDD - (Vgs – 2Vt)) voltage be applied at the transistors gates so they remain operating properly.

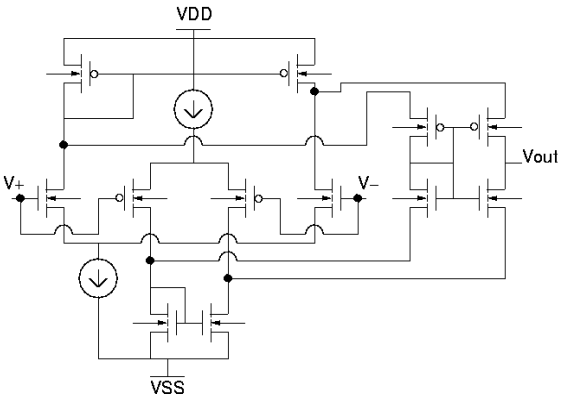

Figure 3 – Rail-to-Rail Comparator

To circumvent the input voltage range limitations it was used a rail-to-rail amplifier [8]. In this topology parallel PMOS and NMOS differential input stages are used, which allows that the applied input voltage be as low as VSS and as high as VDD.

2.4. S/H

The Sample and Hold circuit should make a new sample at each clock step. The basic architecture used in the S/H circuit can be seen in Figure 4.

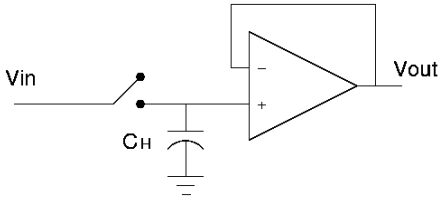

Figure 4 – Basic sample-and-hold circuit

All high quality sample-and-hold circuits must meet certain requirements: the analog switch must have both

low ON resistance and extremely low OFF leakage currents. The holding capacitor must charge up and settle to its final value as quickly as possible. The unit gain and high impedance buffer should have a high ability to control the stability with capacitive loads of the circuit.

3. RESULTS

The ADC design was designed for 0.5 micron CMOS technology. The simulations shows below were performed in Eldo simulator from Mentor Graphics. The converter has a conversion speed of 200 KHz.

The resulting static differential nonlinearity (DNL) of a 10-bit converter is shown in Fig. 5. For 10-bit linearity, the DNL needs to be between 0.5 LSB.

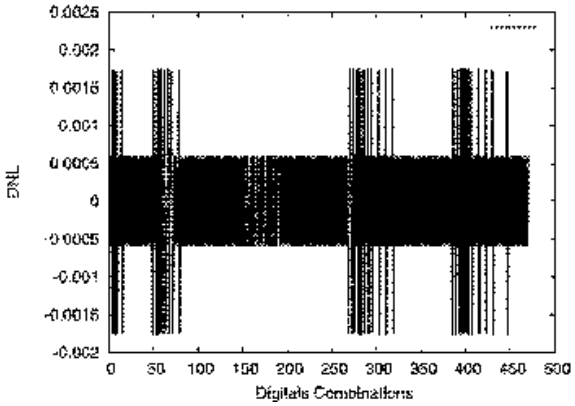

Figure 5 – Differential nonlinearity (DNL)

Note that the DNL of the device is consistent with the design specification (± 1 LSB).

4. ACKNOWLEDGMENTS

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5. CONCLUSION

The ten-bit analog-to-digital converter of successive-approximations was presented. Simulations results show that ADC has a DNL consistent with the specification (between 0.5 LSB), to a conversion speed of 200 kHz. The architecture chosen in the D/A converter block (C-2C), demonstrate that the design is good choice to embed larger systems, where the area occupied by the circuit is a determining factor.

The layout is still in progress. The device is designed to provide a total Silicon die area (including pads) of $4mm^{2.}$

6. REFERENCES

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