EFFECT OF COMPLEX CELL FUNCTIONS IN THE TECHNOLOGY MAPPING PROCESS

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ABSTRACT

The composition of cell libraries is crucial to the quality of the technology mapping process. Commercial cell libraries usually contain only simple logic functions available as combinational cells. However, this paper shows that by using complex function cells (6 or more inputs) in the library composition, there is a tendency to decrease the area and leakage of the mapped circuit.

1. INTRODUCTION

Technology mapping is an important part of the design process of digital VLSI circuits. The library based approach is the usual method for technology mapping. This methodology is based on a set of pre-designed cells that are instantiated to compose the final circuit during the technology mapping process.

The development of a circuit design targets some optimization goals and design constraints, as for instance the minimization of delay or power consumption while respecting maximum area. To achieve this optimization under constraints, it is necessary to choose the best possible combination of cells. Obviously, this choice is restricted to the cells available in the library.

Commercial cell libraries usually contain only simple functions available as combinational cells. This work defines small functions as cells with up to 4 inputs. These libraries limit the mapping tool choices; by adding complex cell functions (6 or more inputs) to these libraries, it is possible to evaluate the effect of complex cells in the mapped circuits.

This paper presents an analysis focusing on the usability of complex functions inside standard cell libraries and the improvement that these complex cells functions can give on circuit characteristics after mapping.

2. MOTIVATION AND PROPOSITION

In previous studies performed by the author[1], it was noticed that when using famous benchmarks[2] and a big group of cell functions[3], there was, in the mapping analysis, a high concentration of a small set of cells. This set of cells was mostly composed of cells of 1 to 4 inputs, except for 2 cell functions of 6 inputs.

These results depend on a number of factors, such as the cells that composed the library, whether the benchmarks used in the analysis had a logical structure that would permit the use of complex cells in the mapping process, whether the mapping algorithm had capacity to see non-simple cell functions, etc.

Looking at the numerous possibilities for which the mapped circuit didn't use the other cells in the mapping process, more specifically the complex cells, it was made a simple analysis that was the motivation for this work. It was made a circuit with 7 inputs that had a complex cell equivalent characterized.

The circuit was mapped using two libraries and focusing on minimum area. The first library, called ComplexCells, included the equivalent complex function cell, and the other, called Basics, had only 1 and 2-input cell functions from Genlib[3]. Figure 1 shows the mapped circuit schematic for the ComplexCell library and Figure 2 shows the mapped circuit schematic for Basics.

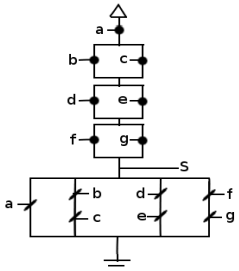

Figure 1 – Mapped circuit schematic with ComplexCell library

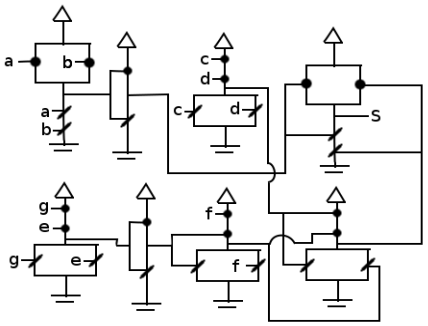

Figure 2 – Mapped circuit schematic with Basics library

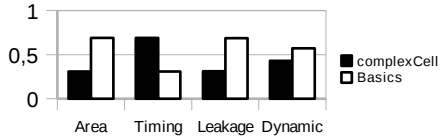

Figure 3 – Characteristics x Percentage over a total
Total area = 10,03 µm²
Total timing = 139 ps
Total leakage = 109,61 nW
Total dynamic = 555,71 nW

The mapping results for area, timing, leakage and dynamic power can be seen in Figure 3. As can be

noticed, the results were better for the mapping with the complex cells for area and, consequently, leakage and dynamic power.

As a main proposition, this work will evaluate the influence of complex cells over the circuit mapping through a large library (all functions from Genlib up to 7 inputs). Also, this work will show a performance comparison between this large library with complex cells, a library based on the most usual functions in commercial libraries and a library composed only of 1 and 2-input functions from Genlib.

Unlike the previous work, the benchmarks will be built with a logic structure that is previously known to have the possibility of accepting these complex cells in its mapping process.

3. METHODOLOGY

The analysis will use three kind of libraries and two kinds of benchmarks, each one with its main feature.

3.1 Libraries

Basic Library: A library composed of all 1 and 2-input cells from Genlib functions.

Commercial Library: Composed of 31 cell functions based on commercial libraries, more specifically from FreePDK[4] functions. Also included were some cells used often in the previous work[1].

AllFunctions Library: Composed of all cells from Genlib up to 7 inputs. Also added were others important cells: HA, XOR2, NXOR2, MUX2 and FA. The cells with 6 or more inputs are considered complex cells, and they will be the focus of the analysis.

All libraries described above have X1, X2 and X4 drive strength for all their functions. The cells were characterized by Nangate Library Creator[5] and their layouts were generated by Encounter[6].

3.2 Benchmarks

The main focus of this paper is to analyze the use of complex cells. Therefore, the benchmarks are designed in a way that their structures allow the use of complex cells in the mapping process. The benchmarks will be divided in two sets.

In the first set of benchmarks, each benchmark has the same logic structure as a complex cell from the AllFunctions library. The purpose is to analyze the effect of the mapping with all libraries when the circuit to be mapped is exactly a complex cell.

In the second set of benchmarks, each benchmark will be logically composed of all functions of all complex cells available in the AllFunctions library.

In both sets of benchmarks, all benchmarks will be described by NAND/INV cells, with the objective of maintaining a neutral description of the circuits.

3.2 Analysis Methodology

The mapping tool is RTLCompiler[7], with the mapping tool set to maximum effort.

The analysis will be divided in 4 steps. In each step, the influence of the library on the mapping process will be analyzed with a different optimization focus. The optimization focuses are: area, timing, leakage and dynamic power. In each step, 2 benchmarks will be analyzed, 1 from each set of benchmarks.

The first benchmark, that we will called B1, will be a logic circuit equivalent to the described boolean function in equation 1.

S = not(((a and b) and (c or d)) and ((e or f) or g)) (Eq. 1)

The second benchmark, which will be called B2, belongs to the second set of benchmarks.

In each step, each benchmark is mapped to the 3 libraries, generating 3 mapped circuits.

The results of each benchmark in this work are equivalent to the other benchmark of each respective group. Because of this, the study will be based only on these benchmarks.

Aside from the 3 mapped circuits with the 3 libraries described before, the mapped circuit of B1 and B2 were created using only complex cells and inverters. These circuits will be called BigCells.

4. ANALYSIS AND RESULTS

4.1 Minimum area analysis

In this analysis the mapping focus is the minimum area. A main constraint that forces the mapping tool to obtain the minimum area (respecting others intrinsic constraints from the tool) is used.

Figure 5 shows the mapping results of B1 for minimum area. The mapped circuit generated for AllFunctions resulted in the same circuit as BigCells. This result means that the minimum area was reached by the complex cells.

Figure 6 shows the mapping results of B2 for minimum area. In this case, the mapped circuit that showed the minimum area was BigCells.

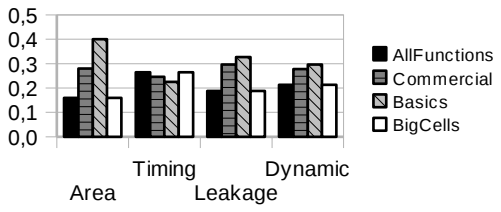

Figure 5 – Characteristics x Percentage over a total
Total area = 17,289 µm²
Total timing = 329 ps
Total leakage = 238,623 nW
Total dynamic = 1157,485 nW

Instead of containing all cells used in the mapping of BigCells, the circuit mapped with the AllFunctions Library didn't reach the minimum area. Some explanations would be that the heuristic used by

RTLCompiler didn't find the best result, or the intrinsic constraints of the tool for power and timing didn't allow this mapping with only complex cells.

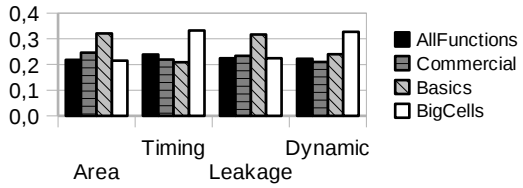

Figure 6 – Characteristics x Percentage over a total
Total area = 5746,159 µm²
Total timing = 27610 ps
Total leakage = 71687,318 nW
Total dynamic = 442461,204 nW

4.2 Minimum Time Analysis

In this analysis the mapping focus is the minimum worst delay. The main constraint is minimum delay. The minimum area constraint is the second to be respected by tool, and it will be applied in the subsequent analysis.

Figure 7 shows the mapping results of B1 for minimum delay. There was a small improvement in timing using the AllFunctions library, but its mapped circuit didn't use any complex cells. The mapped circuit is composed only of cells with 1 to 4 inputs.

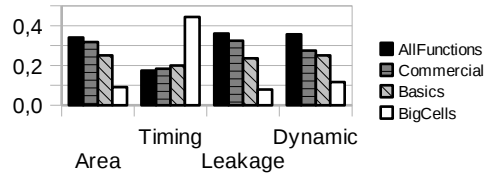

Figure 7 – Characteristics x Percentage over a total
Total area = 30,43 µm²
Total timing = 196 ps
Total leakage = 572,11 nW
Total dynamic = 2109,596 nW

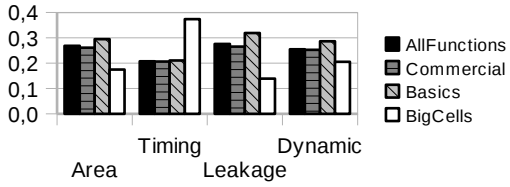

Figure 8 – Characteristics x Percentage over a total
Total area = 9149,523 µm²
Total timing = 17879 ps
Total leakage = 189747,956 nW
Total dynamic = 901363,192 nW

For the B2 benchmark, the Figure 8 shows the mapping results for minimum delay. The AllFunctions library had the same performance as the Commercial library and this one had almost the same performance as the Basics library. The complex cells weren't used by AllFunctions' mapped circuit. This shows that the cells with 1 to 4 inputs tend to have a better performance for minimum delay than complex cells.

4.3 Minimum Leakage Analysis

In this analysis, the main mapping focus is minimum leakage. The main constraint in the mapping tool is minimum leakage.

Figure 9 shows the mapping results of B1 for minimum leakage. This focus was reached by the AllFunctions library's mapped circuit. It used the equivalent complex cell for circuit B1, implying that it has the same composition as BigCells.

Figure 10 is shows the results of the mapping of B2 for minimum leakage. Like B1, B2 obtained the best result in leakage with the AllFunctions mapping. The AllFunctions mapped circuit used a good quantity of complex cells in its structure.

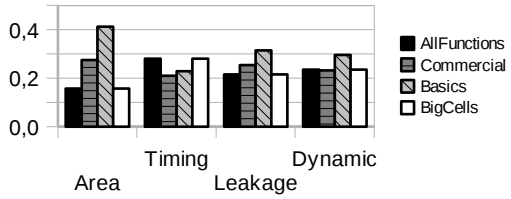

Figure 9 – Characteristics x Percentage over a total
Total area = 17,635 µm²
Total timing = 310 ps
Total leakage = 208,501 nW
Total dynamic = 1045,739 nW

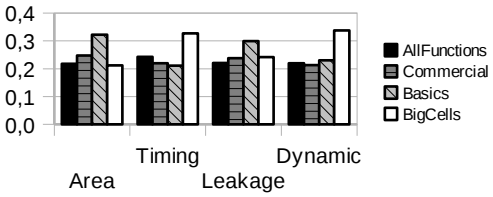

Figure 10 – Characteristics x Percentage over a total
Total area = 5865,113 µm²
Total timing = 27846 ps
Total leakage = 67391,574 nW
Total dynamic = 428160,295 nW

4.4 Minimum Power Dynamic Analysis

In this analysis, the main constraint defined in the mapping tool was minimum dynamic power.

Figure 11 shows the mapping results of B1 for minimum dynamic power. The performances in dynamic power by the mapped circuits for AllFunctions and Commercial are identical. It shows that for an isolated complex cell, there was no improvement with its use.

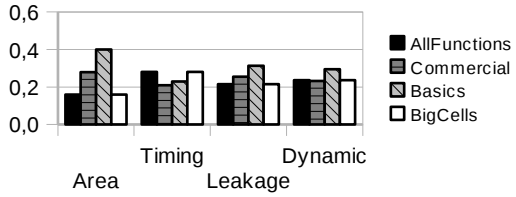

Figure 11 – Characteristics x Percentage over a total
Total area = 17,289 µm²
Total timing = 310 ps
Total leakage = 208,238 nW
Total power = 1043,826 Nw

Figure 12 shows the results of the mapping of B2 for minimum dynamic power cost. The best

performance in dynamic power was achieved by the Commercial library's mapped circuit.

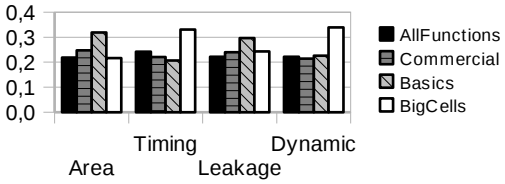

Figure 12 – Characteristics x Percentage over a total
Total area = 5734,401 µm²
Total timing = 27471 ps
Total leakage = 66815,154 nW
Total dynamic = 423868,962 nW

The AllFunctions library contains all cells that compose the Commercial Library, but the Commercial library showed a better performance. It shows that if there are many cells in a library, it can decrease the mapping process quality. This result had been noticed in previous works[1].

5. GENERAL ANALYSIS

5.1 Complex cell influence in mapped circuits

Through the analysis applied, mapped circuits that had used complex cells suffered a reduction in area and an increase in worst delay.

A complex cell is logically equivalent to a set of smaller cells but, being an unique cell, it tends to have less transistors than the set of smaller cells. With less transistors, almost always, it will have less area.

Complex cells have a high parasitic capacitance and resistance, caused by its large size. The power supply is the same for all cells, so if the cell has a high capacitance, it will take more time to be charged and discharged. Therefore, the circuit's worst delay can be increased when complex cells are used in its mapping.

The leakage suffered a certain decrease when complex cells are used, as can be seen in the analysis. The distance in number of transistors from Vdd to Gnd in a complex cell is, almost always, superior to that of smaller cells. Each transistor contains a parasitic resistance. Also, the leakage is inversely proportional to the resistance between Vdd and Gnd, so with more transistors deactivated between Vdd and Gnd, there is less leakage in the cell.

Like the leakage, the dynamic power suffered an influence, but in this case, dynamic power is increased when complex cells are used. Mapped circuits with only small cells presented less dynamic power than mapped circuits composed by complex cells.

5.3 Large libraries can make the mapping process in the commercial tool more difficult

The algorithm used by the commercial tool isn't known, but it's easy to conclude that it is a heuristic, because the mapping problem is NP. As any heuristic, there is a probability to find the optimized solution. In this mapping tool, the probability tends to be dependent on the number of cells in the library. When there are more cells in the library, it is more difficult for the mapping algorithm to find the cells that will give the optimal solution.

5.4 Complex cell usability limitations

The benchmarks used in this paper were created with the purpose of including the complex cells available in the library in the mapping process, but it doesn't happen in an actual case. There is a crucial problem, given a circuit, the library used need to be composed of complex cells that can be mapped to that circuit, otherwise the complex cells will not be used.

6. CONCLUSION AND FUTURE WORKS

Technology mapping is an important step in the design of VLSI circuits. Through this work, it was shown that there is a high dependency between the result achieved by the technology mapping process and the composition of the target cell the library; including the number of cells, what functions are available, etc.

The work also evidenced that there may be advantages in the use of complex cells. These gains appear under the condition that the mapping algorithm has to be able to cope with these large cells and that the complex cells exist in the logic structure of the circuit that is mapped.

As a future work, it is necessary to analyze the impact of complex cells inside a mapped circuit when routing is also taken into account[8]. Another future work is to evaluate the efficiency of the mapping using the concept of libraryFree mapping [9] to complex cells. Using this concept, the mapping algorithm is not limited by the available cells in a library, but it can generate new cells on the fly.

7. REFERENCE

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