DIRECT DETERMINATION OF THE MOSFET PARAMETERS MEASURTING I_D IN THE LINEAR REGION AS A FUNCTION OF THE SOURCE VOLTAGE

T. de Oliveira, G. Naspolini and. C. Galup-Montoro

Department of Electrical Engineering, Federal University of Santa Catarina, Florianópolis, SC, CEP 88040-900, Brazil
e-mail: thiago.oliveira@ieee.org

ABSTRACT

This paper presents a new procedure for MOSFET transistors characterization. It is based on expressions that are valid in all regimes of operation, from weak to strong inversion levels and have direct physical meaning. The proposed procedure is insensitive to mobility degradation and channel length modulation since it is based on the measurement of a transconductance-to-current ratio in the linear region of operation of the MOSFET.

1. INTRODUCTION

There are a large set of methods for extracting the basics dc parameters of a MOSFET, particularly the threshold voltage V_{TO}, but few of them respect the desirable properties summarized in [1]: to be valid for all technologies, to be easily applicable, and to have a clear physical-based definition of V_{T0} [2]. In the next section the methodology presented in [2] is revisited, and in the third section it is improved in order to extract V_{T0}, the specific current I_S, the mobility μ, and the slope factor n in a direct way and without making any simplifying assumptions. In the last section the extraction procedures of sections 2 and 3 are applied to experimental and simulated data.

2. THE EXTRACTION METHODOLOGY USING TRIODE LINEAR REGION

The method of V_{T0} extraction in the linear region was conceived based on an equation of the MOSFET valid for all region of transistor operation, *i.e.* from the weak inversion where the current is exponential with respect to the gate voltage to the strong inversion crossing through the moderate inversion.

The drain current can be defined in terms of direct i_f and reverse i_r normalized currents.

$$I_D = I_S\left(i_f - i_r\right) \tag{1}$$

where I_S is the normalization current

$$I_S = \mu_n C'_{ox} n \frac{{\phi_t}^2}{2}\frac{W}{L} \tag{2}$$

The Unified Current Control Model (UICM) is

$$\frac{V_P - V_{S(D)}}{\phi_t} = \sqrt{1 + i_{f(r)}} - 2 + \ln\left(\sqrt{1 + i_{f(r)}} - 1\right) \tag{3}$$

where V_P is the pinch-off voltage which is commonly approximated by [3]

$$V_P \cong \frac{V_G - V_{T0}}{n} \tag{4}$$

In our extraction procedure we do not use this approximation and we determine in principle the exact value of the pinch-off voltage

The slope factor $n = dV_G/dV_P = 1+C'_b/C'_{ox}$ is not dependent only of technological parameters, but also of biasing since the majority carrier (bulk) capacitance C'_b depends on the gate-to-substrate voltage V_G.

Form the equations above the transconductance over drain current is given by [2]:

$$\frac{g_{mg}}{I_D} = \frac{2}{n\phi_t\left(\sqrt{1+i_f} + \sqrt{1+i_r}\right)} \tag{5}$$

2.1. The extraction procedure of [2]

When performing the measurements of drain current, if the drain to source voltage V_{DS} is set be very low, *i.e.,* linear region of transistor operation, the effects of longitudinal electric field, short-channel, and parasitic resistances can be neglected.

Due to that bias technique the transistor works electrically as a piece of a long channel transistor, and the expressions can be then simplified with $i_f \cong i_r$. In this case, according to [2] the V_{T0} voltage is the gate voltage for which g_{mg}/I_D is just a half of its maximum value (see Fig. 1).

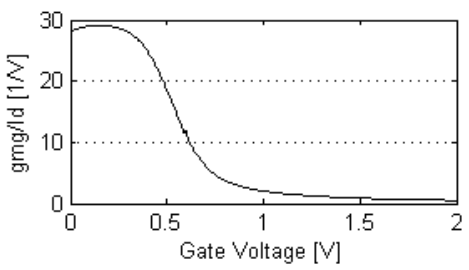

Fig. 1 BSIM simulation of g_{mg}/I_D of a NMOS transistor

The procedure proposed in this work is analogous, since it also based on the measurement of the drain

current in the linear region and taking advantage of the behavior of the transistor in moderate inversion.

2.2. The new extraction circuit

The circuit of Fig. 2 was conceived to make use of the same set of basic expressions, although now the transconductance is a little bit different of g_{mg} since the gate voltage is fixed at a constant value.

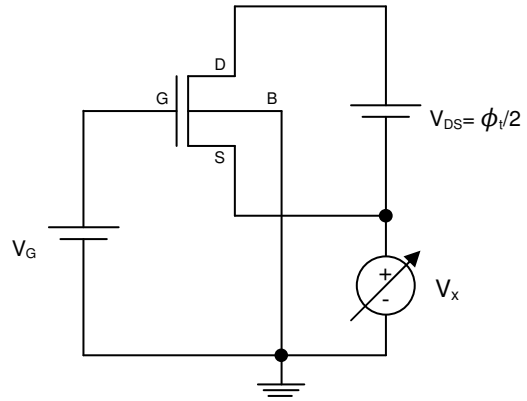

Fig. 2 NMOS methodology configuration in triode region for current derivation

The circuit in Fig. 2 is such that the gate voltage is defined by the constant voltage V_G and the substrate bulk terminal is tied to the reference node. The voltage at the inversion channel is defined by the constant voltage V_{DS}, which in this case bias the channel in the linear region with half of the thermal voltage ϕ_t to minimize short-channel effects. The variable voltage source V_X is then linear increased from the reference where the drain current is at the maximum, up to the gate voltage cutting the current in the transistor, as shown in Fig. 3

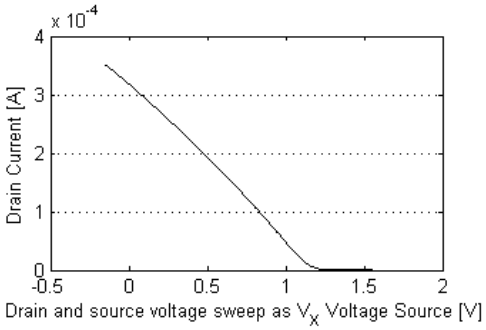

Fig. 3 Commom drain current curve for the circuit proposed

The current variation on the transistor is

$$\Delta I_D = g_{mg}\Delta V_G - g_{ms}\Delta V_S + g_{md}\Delta V_D + g_{mb}\Delta V_B \quad (6)$$

The substrate and gate voltages do not vary thus $g_{mb}\Delta V_B$ and $g_{mg}\Delta V_G$ results are zero.

For the circuit in Fig. 2 the variation of the drain voltage is equal to the variation of the source voltage

$$\Delta V_S = \Delta V_D = \Delta V_X \quad (7)$$

The derivative of transistor current with respect to V_X is defined as:

$$\frac{\partial I_D}{\partial V_X} = -g_{ms} + g_{md} = G_{no} \quad (8)$$

From [4], the transconductances as function of the inversion levels for all-regions are:

$$g_{ms(d)} = \frac{2I_S}{\phi_t}\left(\sqrt{1 + i_{f(r)}} - 1\right) \quad (9)$$

Substituting (9) into the G_{no} definition (8) it is easy to find that:

$$G_{no} = -\frac{2I_S}{\phi_t}\left(\sqrt{1 + i_f} - 1\right) + \frac{2I_S}{\phi_t}\left(\sqrt{1 + i_r} - 1\right)$$

$$\frac{G_{no}}{I_S(i_f - i_r)} = \frac{-2}{\phi_t\left(\sqrt{1 + i_f} + \sqrt{1 + i_r}\right)} \quad (10)$$

Finally solving for (1) we have:

$$\frac{G_{no}}{I_D} = \frac{-2}{\phi_t\left(\sqrt{1 + i_f} + \sqrt{1 + i_r}\right)} \quad (11)$$

In opposition to eq. (5) equation (11) is not affected by the slope factor because of the fixed gate voltage.

The Fig. 4 shows the noise of an experimental extraction in dashed line and the smoothed curve in solid line.

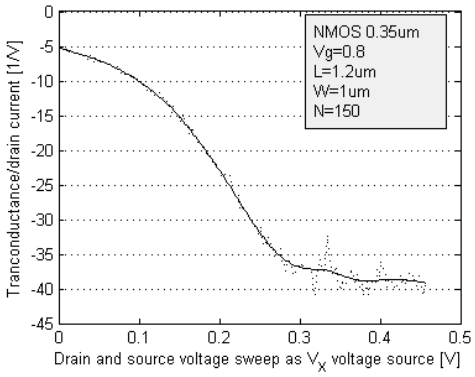

Fig. 4 - The smoothing of noisy extraction of tiny currents at triode region

Comparing both methods plotting the two curves together as function of transistor's current, the influence of the slope factor is clearly noticed. (See Fig. 5)

In Fig. 5 the dashed line represents the g_{mg}/I_D and the solid line is the G_{no}/I_D. This figure corresponds to BSIM3v3 simulation of a NMOS 0.35µm with the effective aspect ratio of 125 at 25ºC.

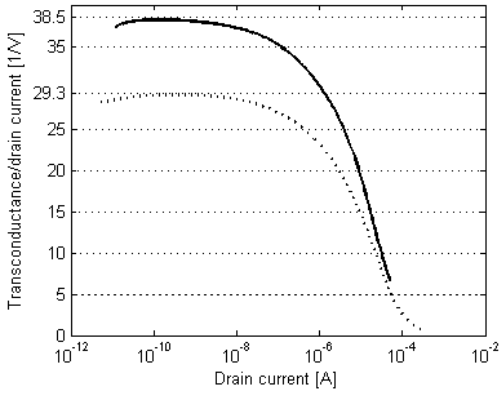

Fig. 5- BSIM simulation of g_{mg}/I_D X G_{no}/I_D of NMOS MOSFET transistor

3. PROCEEDINGS FOR PARAMETERS EXTRACTION

Recalling the triode condition imposed before the expression (11) can be reduced to:

$$\frac{G_{no}}{I_D} = \frac{-1}{\phi_t\left(\sqrt{1+i_f}\right)} \tag{12}$$

The maximum transconductance happens at peak of G_{no}/I_D where the current is in its minimum value, hence the direct normalized current i_f tends to zero, and the point is calculated simply by:

$$\left.\frac{G_{no}}{I_D}\right|_{max} = \frac{-1}{\phi_t} \tag{13}$$

Observing the UICM (3) and using the same methodology adopted in [2], if $i_f = 3$ the right term of the equation is equal to zero and the UICM returns the pinch-off voltage like eq.(14). To experimentally find the pinch-off voltage for $i_f = 3$, the maximum value of the curve must be measured and divide it by two.

$$V_P = V_X \tag{14}$$

Thus, we can perform the main parameters extraction using only the circuit of Fig. 2. The exact extraction of the pinch-off voltages as a function of the gate voltage is the utmost information provided by the circuit. To capture this information a set of V_G spaced extractions need to be made and thus the value of n shows up by deriving V_P as function of V_G because:

$$n = \frac{1}{dV_P/dV_G} \tag{15}$$

The threshold voltage is from (4):

$$V_{T0} = -nV_P + V_G \tag{16}$$

Fig. 6 shows the BSIM3V3 V_P as a function of the gate voltage, and Fig. 7 shows the slope factor simulated also.

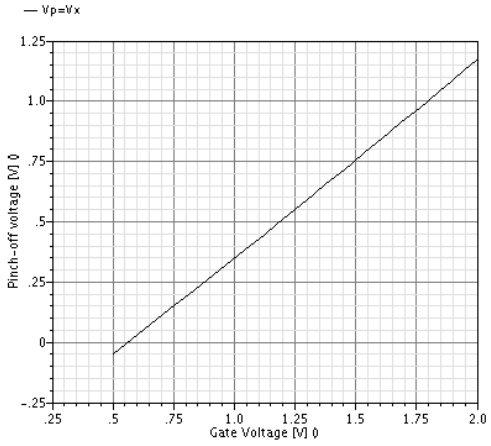

Fig. 6 Pinch-off voltage as function of gate voltage BSIM simulation

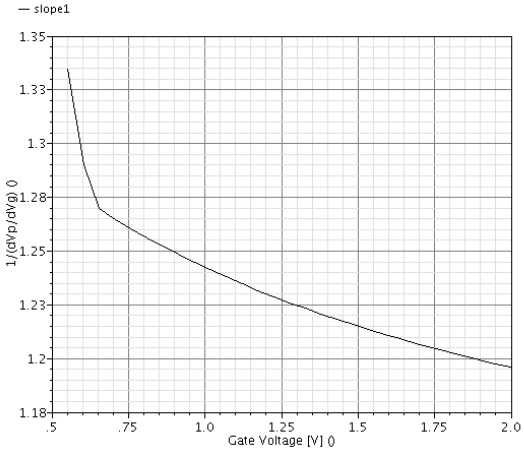

Fig. 7 Slope factor as function of gate voltage BSIM simulation.

In fact i_f is slightly different from i_r in triode region. From UICM applied to source and drain eq.(17) evaluate the exact i_r for a given V_{DS}. Applying for $i_f = 3$ and $V_{DS} = \phi_t/2$, the i_r equals to 2.12, and using this in the eq.(11) the G_{no}/I_D results in 0.53 times the max value of the extracted curve.

$$\frac{V_{DS}}{\phi_t} = \sqrt{1+i_f} - \sqrt{1+i_r} + \ln\left(\frac{\sqrt{1+i_f}-1}{\sqrt{1+i_r}-1}\right) \tag{17}$$

Knowing that for low V_{DS}, $i_f \to i_r$, the eq.(17) becomes

$$\frac{V_{DS}}{\phi_t} \cong \frac{1}{2}\frac{(i_f - i_r)}{\sqrt{1+i_f}-1} = \frac{1}{2}\frac{{}^{I_D}/_{I_S}}{\sqrt{1+i_f}-1} \qquad (18)$$

The specific current extraction obeys the same proceeding as in [2]. For the values of i_f, i_r and V_{DS} found before, the I_S in the eq.(18) results in 1.13 times de drain current measured at $V_X = V_P$.

The mobility may also be extracted as a function of V_G from (19)

$$\frac{Is}{n} = \frac{\mu_0 C'_{ox} {\phi_t}^2}{2}\frac{W}{L} \qquad (19)$$

4. RESULTS

The result table below summarizes the extraction using the ${}^{g_{mg}}/_{I_D}$ and the ${}^{G_{no}}/_{I_D}$ methods simulation and experimental measures.

The measurements were taken using the Agilent 4156C precision semiconductor analyzer and the data acquired was processed using MATLAB. The test chip used and the BSIM models were from TSMC 0.35µm standard CMOS process.

W/L	N	V_{T0} [V]	I_S [A]	Method	Process
1µm / 1,2µm	150	0.566	10µ	G_{no}/I_D	BSIM3v3
1µm / 1,2µm	150	0.564	9.6µ	G_{no}/I_D	Experimental
1µm / 1,2µm	150	0.575	12µ	g_{mg}/ I_D	BSIM3v3

Table 1 Simulated and experimetal characterizations of 0.35µm TSMC standard CMOS process.

5. CONCLUSIONS

Table 1 shows the consistency of the two methods of extraction in the linear operation region. The noise of the low currents can be minimized with some simple signal processing. The ability to determine the main MOSFET parameters as a function of the gate voltage without having the influence of longitudinal electric field, short-channel, and parasitic resistances effects turns the procedure very interesting. The threshold voltage was evaluated in a physical bases using charge-based model and with this method applied the proceeding is not affected by the slope factor and the specific current variations because the gate voltage is kept constant.

6. REFERENCES

[1] M. Tsuno, M. Suga, M. Tanaka, K. Shibabara, M. Miura-Mattaush, and M. Hirose, "Physically-based threshold voltage determination for MOSFETs of all gate lengths," *IEEE Trans. Electron Devices*, vol. 46, pp. 1429–1434, July 1999.

[2] A. I. A. Cunha, M. C. Schneider, C. Galup-Montoro, C. D. C. Caetano, and M. B. Machado, "Unambiguous extraction of threshold voltage based on the transconductance-to-current ratio", *Workshop on Compact Modeling*, Anaheim, USA, in Proceedings of Nanotech 2005, pp. 139 - 141, May 2005.

[3] C.Enz, F.Krummenacher, and E. Vittoz, "An analytical MOS transistor model valid in all regions of operation and dedicated to low-voltage and low-current applications," *Journal of Analog Integrated Circuits and Signal Processing*, vol. 8, pp. 83-114, July 1995.

[4] M. C. Schneider and C. Galup-Montoro *CMOS Analog Design Using All- Region MOSFET Modeling*, Cambridge, Cambridge University Press, 2010.