INTEGRATED THREE STAGE OPERATIONAL AMPLIFIER IP

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ABSTRACT

This paper is result of a conclusion work of an Integrated Circuit Project course in Electronic Engineering graduation. The course introduces digital and analog design techniques. The main goal of this work is to explore some of these techniques used in circuit characterization and layout design. The circuit studied here is an integrated CMOS operational amplifier due to it´s applicability and versatility which make it the most used electronic circuit in analog electronic systems. The specifications of the operational amplifier include voltage gain, opamp compensation, frequency response, slew rate and gain bandwidth product.

1. INTRODUCTION

The operational amplifier (opamp) has become a basic analog building block of a multitude of electronic integrated circuits performed in instrumentation, computation and control. Due to the influence of integrated circuits, operational amplifier design and application techniques are becoming essential tools of the linear circuit design [1]. Another key technical development has been a maturing of the state of the art in the implementation of operational amplifiers in MOS technology. These amplifiers are key elements of most analog subsystems, particularly in switched capacitor filters, and the performance of many systems is strongly influenced by op amp performance [2]. Operational amplifiers are designed using a wide variety of fabrication techniques. Originally they contained only bipolar transistors, but now there are a host of devices that use filed-effect transistors within the opamp [3].

Indeed many applications today are best addressed by mixed-mode integrated circuits (mixed-mode ICs) and systems, which rely on analog circuitry for processing and control. Even though the analog circuitry may constitute only a small portion of the total chip area, it is often the most challenging part to design as well as the limiting factor on the performance of the entire system. In this respect, it is usually the analog circuit designer who is called to devise ingenious solutions to the task of realizing analog functions in decidedly digital technologies [4]. In this way the choose for the opamp layout lead us to a variety of techniques learning and experience concerning analog integrated circuits design.

2. OPAMP DESCRIPTION

The configuration that we work here is the three-stage opamp, where we have 2 gain stages – differential pair and common-source amplifiers – and a output buffer stage. Following we have the schematic of the circuit.

2.1. Schematic

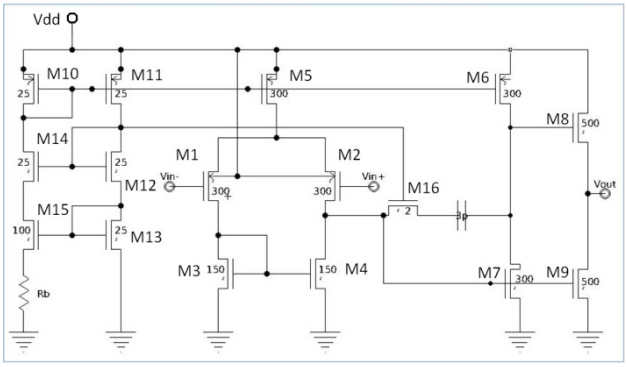

Figure 1: Three-stage opamp schematic.

In this schematic we have the biasing circuit composed of a current mirror and a biasing resistor R_b. The second stage is a differential pair with a n channel active load. The next circuit is the compensation circuit with a transistor acting as a resistor together with a compensation capacitor. The following circuit is the common-source amplifier followed by a source follower output stage.

2.2. Voltage gain

The first stage is a differential pair and it´s voltage gain expression, A_{v1}, according to [5] is:

$$A_{v1} = -g_{m1} * (r_{ds4} || r_{ds2}).$$

where g_{m1} is the transcondutance of the transistor M_1 and r_{dsi} is the drain-source resistance on the small-signal equivalent circuit. The second stage is a common-source amplifier and it´s voltage gain according to [5] is:

$$A_{v2} = -g_{m7} * (r_{ds6} || r_{ds7})$$

in analogy to previous gain expression. The third stage is source-follower and it´s voltage gain in according to [5] is:

$$A_{v3} \cong \frac{g_{m8}}{G_L + g_{m8} + g_{ds8} + g_{ds9}}$$

where $G_L, g_{m8}, g_{ds8}, g_{ds9}$ is the load conductance being driven by the buffer stage, the trascondutance of the transistor Q_8, the drain-source conductance respectively. Then we have the overall gain of the opamp:

$$A_v = A_{v1}A_{v2}A_{v3}$$

In this work we are using a MOS transistor model offered by **MOSIS** (*Mosis wafer acceptance* tests – *technology SCN035*). The parameters used were the product of the charge-carrier effective mobility μ and the gate oxide capacitance C_{ox}, $\mu_p \frac{C_{ox}}{2} = -31.8 \frac{\mu A}{V^2}$, $\mu_n \frac{C_{ox}}{2} = 92.7 \frac{\mu A}{V^2}$, and the threshold voltage $V_{tn} = 0.58V$ and $V_{tp} = -0.72$V.

The biasing circuit is designed to $I_{d5} = I_{d7} = 100\mu A$, $I_{d8} = 167\mu A$ and the load is considered to be resistive with value $R_L = 10k\Omega$, where $V_{dd} = -V_{ss} = 3.3V$. First we will obtain the value for A_{v1}. The transcondutance expression in according to [5] is:

$$g_{m1} = \sqrt{2\mu_p C_{ox}(\frac{W}{L})_1 i_{d1}} = \sqrt{2 * (62\frac{\mu A}{V^2})(\frac{300}{2})50\mu A}$$

$$g_{m1} \cong 0.96\ {}^{mA}/_{V}$$

where $\mu_p, C_{ox}, W, L, i_{d1}$ are the hole mobility, the capacitance of the gate oxide, width, length and current drain respectively. For r_{dsi} according to [5] we have:

$$r_{dsi} = \alpha \frac{L_i}{I_{di}} \sqrt{v_{dgi} + v_{tp}}$$

where $\alpha, L_i, I_{di}, v_{dgi}, v_{tp}$ are a technology-dependent parameter that is around $5 * 10^6\ {}^{\sqrt{V}}/_{m}$, the length of the transistor, the current drain, the drain gate voltage and threshold voltage of the p channel transistor respectively. Then we have:

$$r_{ds1} = 5 * 10^6 * \frac{2 * 350nm}{50\mu A} \sqrt{2.6 + 0.72} \cong 120k\Omega$$

since $r_{ds2} = r_{ds4} = r_{ds1}$ we have $r_{ds2} || r_{ds4} = {}^{r_{ds1}}/_{2}$. Then for the voltage gain A_{v1} we have

$$A_{v1} = -0.96\ {}^{mA}/_{V} * 60k\Omega \cong -57.60$$

For the voltage gain A_{v2} in analogy with the previous calculation we need to obtain the parameter g_{m7}:

$$g_{m7} \cong 2.33\ {}^{mA}/_{V}.$$

For $r_{ds6} || r_{ds7}$ we have:

$$r_{ds6} = 5 * 10^6 * \frac{2 * 350nm}{100\mu A} \sqrt{2 + 0.58} \cong 56k\Omega$$

since $r_{ds6} = r_{ds7}$ we have $r_{ds6} || r_{ds7} = {}^{r_{ds6}}/_{2}$.

Then for the voltage gain A_{v2} we have

$$A_{v2} = -2.33\ {}^{mA}/_{V} * 28k\Omega \cong -65.24$$

To calculate the voltage gain A_{v3} we obtain:

$$g_{m8} \cong 4\ {}^{mA}/_{V}.$$

And calculating r_{ds8} *and* r_{ds9} we have

$$r_{ds8} = 5 * 10^6 * \frac{2 * 350nm}{167\mu A} \sqrt{3 + 0.58} \cong 40k\Omega$$

since $r_{ds8} = r_{ds9}$ we have $g_{ds8} = g_{ds9} = 25 \frac{\mu A}{V}$. finally $G_L = {}^{1}/_{R_L} = 10^{-4}\ {}^{A}/_{V}$ gives:

$$A_{v3} \cong 0.96$$

The overall voltage gain is

$$A_v = 0.96 * 57.60 * 65.24 \cong 3.607\ {}^{V}/_{V}.$$

which is approximately $\mathbf{71.15dB}$.

2.3. Opamp compensation

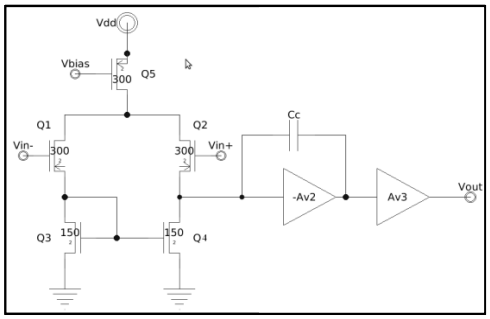

Figure 2: Compensation analysis equivalent circuit.

Operational amplifiers are generally (almost always) used in a negative feedback configuration, and then we must ensure that the closed-loop behavior of the opamp is stable. When we are looking for the transfer function of the closed-loop opamp configuration at high frequencies we have the influence of additional poles (no dominant poles) and zeros. The analysis of the small-signal circuit yields:

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{g_{m1}g_{m7}R_1R_2\left(1 - \frac{sC_c}{g_{m7}}\right)}{1 + sa + s^2b},$$

where one of the poles of the denominator is the first dominant pole and after solving the second order expression the expression to this pole is

$$\omega_{p1} = \frac{1}{g_{m7}C_cR_1R_2}$$

where $R_1 = r_{ds4}||r_{ds2}$ and $R_2 = r_{ds6}||r_{ds7}$ and the compensation capacitor is known in the order of units of picofarads (we have chosen $C_c = 5pF$). Using these values to calculate f_{p1} we obtain

$$\boldsymbol{f_{p1} = 8.3kHz}.$$

Through the expression for ω_{p1} we can see clearly the role of the capacitor C_c that is to compensate the dominant first pole, i.e. to control the frequency of this pole.

2.4. Frequency response

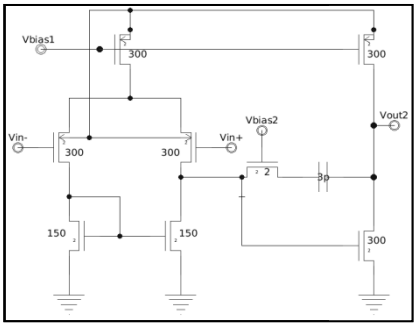

Figure 3: Equivalent circuit to frequency analysis.

To calculate the frequency response we will use the simplified model and using the Miller´s theorem we can show that:

$$C_{eq} = C_c * (1 + A_{v2}) \cong C_c * A_{v2}.$$

We know that the first stage gain is $A_{v1} = g_{m1} * z_{out}$ where $z_{out} = r_{ds4}||r_{ds2}||\frac{1}{sC_c * A_{v2}}$ because the second stage introduce a capacitance C_{eq} due to the compensation capacitor. For midband frequencies the impedance of C_{eq} is too smaller than the others so we have $z_{out} \cong \frac{1}{sC_c A_{v2}}$. For the overall gain we have

$$A_v(s) = A_{v1}A_{v2}A_{v3} = A_{v2}A_{v3}\frac{g_{m1}}{sC_c A_{v2}}.$$

Now considering the approximated voltage gain of the third stage $A_{v3} \cong 1$ and assuming that we are looking for the unit-gain frequency or $|A_v(j\omega_{ug})| = 1$ we have:

$$A_v(j\omega_{ug}) = \frac{g_{m1}}{j\omega_{ug}C_c}$$

what give us $|A_v(j\omega_{ug})| = \frac{g_{m1}}{\omega_{ug}C_c}$, then we have

$$f_{ug} = \frac{0.96\ {}^{mA}/_{V}}{2\pi * 5pF} = 30.6MHz$$

2.5. Slew rate

We can define *slew rate* as the maximum rate of change of the output voltage.

$$SR = \frac{dV_{out}}{dt}|_{max} = \frac{I_{C_c|max}}{C_c} = \frac{I_{d5}}{C_c}$$

Since $I_{d5} = 2I_{d1}$ and recovering the expression for C_c from the last section we have

$$SR = \frac{2I_{d1}\omega_{ug}}{g_{m1}} = \frac{2I_{d1}}{C_c} = \frac{2 * 50\mu A}{3pF} = 33.3\frac{V}{\mu s}$$

3. OPAMP LAYOUT

We have here a layout of the three stage operational amplifier made in the CAD software *Electric* [6]. The first stage is a differential-input single-ended output stage. The second stage is a common-source gain stage that has an active load.

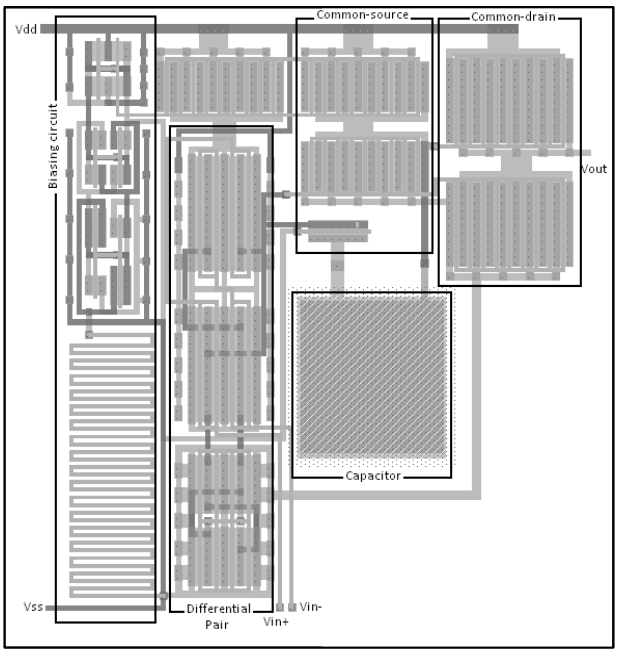

Figure 4: Opamp layout.

MOS transistors are vulnerable to gradients in temperature, stress and dioxide thickness, so matched transistors (differential pair and current mirrors) should have a *common-centroid* layout to minimize offset.

As we can see this technique was used by cross-coupling the differential pair and it´s active load. The current sources of the three stages were implemented by the biasing circuit and a p-channel MOS transistor that has an *interdigitated* configuration. The biasing resistor was implemented in poly1 because it has greater sheet resistance than poly2 and the metal layers ($poly1\ sheet\ resistance\ 8.9\ {}^{\Omega}/_{square}$). The capacitor

is a poly1 surface/plate above a p+ active diffusion which shows the greater capacitance per area (4481 $^{aF}/_{\mu m^2}$) than the poly2/p+active-diff capacitor. To achieve a capacitance of $5pF$ the capacitor area must be $1.116\mu m^2$ that give us $9216\, units^2$ (on layout) since we are working with a $350nm$ technology.

4. SIMULATION RESULTS

The simulating program used was $Ngspice-circuit\ simulator$ [7] on Linux (Ubuntu distribution). The netlist was extracted from layout and the *MOSIS* transistor model (technology SCN035) was used for simulation. All of the parameters were obtained in these simulations, as voltage gain, unit-gain frequency, slew rate, phase margin and gain bandwidth.

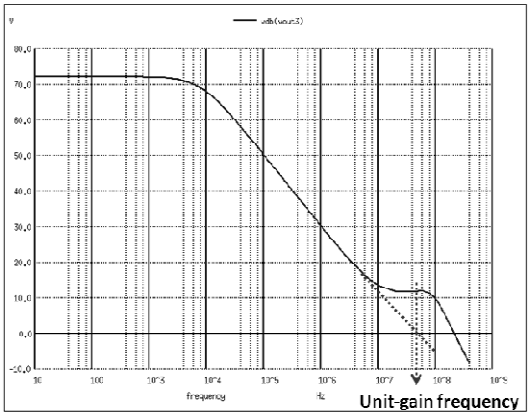

Figure 5: Frequency Response.

As we can see in the figure the voltage gain in dB´s is close to **72dB** which is very near to the value that we obtained on the previous section *Voltage gain***.** The $3dB$ frequency is near to $8kHz$ as foresee. We have a little discrepancy for the unit-gain frequency: the theoretical value is $f_{ug} = 51MHz$ and the simulation value is $f_{ug} = 225MHz$. This can be explained by the influence of both zero and pole around the unit-gain frequency which were neglected when we were calculating f_{ug}. As can seem in the frequency response figure, continuing the $-20dB/decade$ curve (after the 3_{dB} frequency) and crossing the frequency axis we obtain a value near that obtained previously in the calculation

$$f_{ug_{sim}} \cong 30MHz.$$

To the simulated *Slew rate* we have the following waveform (figure that show us the voltage variation rate). We can obtain the SR by observing the time that the output takes to go from minimum to maximum value in response to a step input. Analyzing the figure 6 we obtain a value close to that obtained in the section *Slew rate*

$$SR = \frac{3.3-(-3.3)}{175ns} \cong 37.7\frac{V}{\mu S}$$

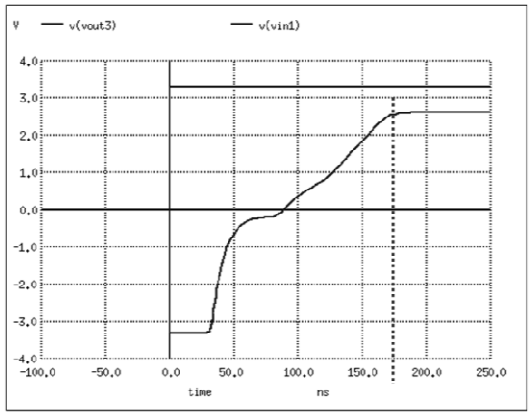

Figure 6: Simulated slew rate.

The gain bandwidth product *GBWP* is the product between the voltage gain and the bandwidth and can be easily obtained when the gain is unitary, i.e. the unit-gain frequency has the same numerical value of the *GBWP*, then we have $\boldsymbol{GBWP = 30 * 10^6}$.

5. CONCLUSION

We consider that the results were satisfactory since the parameters values obtained were very near to that calculated. These results encourage us to keep exploring the wide variety of techniques of analog integrated designs.

6. REFERENCES

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