INFLUENCE OF THE LDD LENGTH IN SOI MOSFET DEVICES

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ABSTRACT

In this paper the influence of the LDD (*Lightly Doped Drain*) length in a planar SOI LDDMOSFET (Silicon-on-Insulator Lightly-Doped-Drain Metal-Oxide-Semiconductor Field-Effect-Transistor) structure is verified through bidimensional numerical simulations. It was observed that the series resistance (R_{SD}) increases linearly with the increase of the LDD length except for devices without the use of LDD, which presented smaller values of R_{SD} than the trend. It was noted that this influence is more evident in shorter devices.

Another behavior analyzed was its influence on the SCE (short channel effects). The devices with the LDD region began to suffer from the SCE for smaller channel lengths.

Finally, a range of LDD lengths that minimizes the SCE and the series resistance was obtained.

1. INTRODUCTION

In order to follow the trend of the Moore's Law, the integrated circuits industry has developed devices with shorter dimensions. However, this reduction give rises to the short channel effects, which limit the smallest channel length that a technology can achieve.

A solution to decrease these short channel effects is to add a source and drain extension region with lower doping concentration, called LDD. Figure 1 shows the planar SOI LDDMOSFET structure with its regions, thicknesses, voltages, mainly dimensions and interfaces defined in this work.
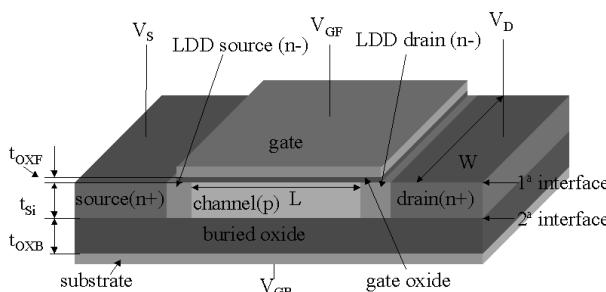
Figure 1: SOI LDDMOSFET structure.

Although these devices have better short channel effects due to the lower potential applied in the channel and a lower lateral diffusion [1,2,3], an increase in the series resistance is observed, due to reduced carrier.

In this work, the influence of different LDD lengths on the series resistance is analyzed. Parameters as maximum transconductance, threshold voltage and subthreshold slope were extracted to evaluate the short channel effects. Besides, the series resistance joined with the minimum channel length without the SCE was obtained to optimize the LDD length, resulting in a range of LDD values that decrease the series resistance and the short channel effects.

2. DEVICES CHARACTERISTICS AND SIMULATION DETAILS

The planar SOI MOSFET structures were implemented using DevEdit, ATLAS [4] bidimensional device editor. Table 1 presents the dimensions of these structures.

Table 1: Devices dimensions.

Dimensions	Values
Channel Length (L)	100nm; 200nm; 300nm; 500nm; 1000nm
LDD length (LDD)	0nm; 25nm; 50nm; 100nm
Buried oxide thickness (t_{OXB})	145nm
Silicon thickness (t_{Si})	60nm
Gate oxide thickness (t_{OXF})	1.5nm
Source length (=drain length)	50nm
Thickness gate contact	5nm
Thickness drain, source and substrate contacts	10nm

The devices simulated were nMOS and so, their channels were P-type, being the source, drain, and LDD, N-type regions. The doping concentrations were 10^{15} atoms/cm^3, 10^{19} atoms/cm^3 and 10^{20} atoms/cm^3 for channel, LDD and S/D regions, respectively. The work functions used were 4.7eV and 4.95eV for gate and substrate respectively, with a temperature of 300K and the source and drain voltage (V_{DS}) of 50mV.

The lateral diffusion phenomenon in the stationary conditions follows the Fick's Law whereby the species flux is directly proportional to the concentration gradient [3]. Then, it was considered a smaller lateral diffusion in the LDDMOSFET than in devices with no LDD. A lateral diffusion of 20nm was used each side for the SOI LDD MOSFETs and of 80nm for SOI MOSFETs devices with abrupt junctions.

The doping concentrations in the structures of planar SOI MOSFETs considered in this work can be seen without using LDD regions in the Figure 2 and using it in the Figure 3. The doping concentrations in the lateral diffusion regions were 10^{20} atoms/cm^3 and 10^{19} atoms/cm^3, respectively.
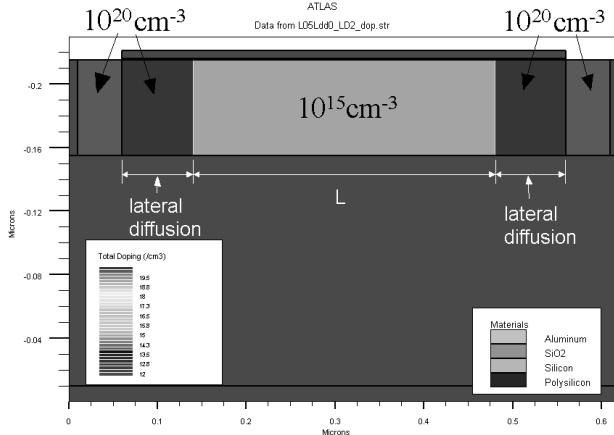
Figure 2: Doping concentration of SOI MOSFET structure without using LDD regions obtained by simulations.
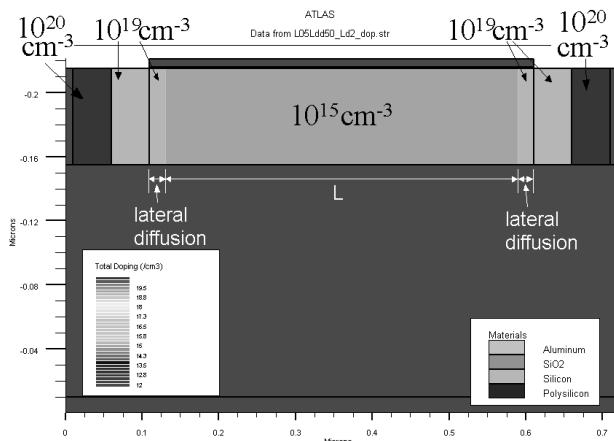
Figure 3: Doping concentration in SOI LDD MOSFET structure obtained by simulations.

3. RESULTS AND ANALYSIS

The main parameters needed to evaluate the short channel effects and the series resistance were obtained by the simulation of the structure presented before, through the drain current (I_D) versus gate voltage (V_{GF}) curves for different channel and LDD lengths studied.

3.1. The transconductance

Figure 5 shows the transconductance (gm) as a function of the gate voltage for different LDD lengths and channel length equal to 0.1µm and Figure 4 shows the maximum transconductance (gm_max) as a function of channel lengths. They were extracted by the derivative of the drain current versus gate voltage curve and its peak, as indicated in equation 1 [5]:

$$gm = \frac{dI_{Dsat}}{dV_{GF}} \qquad (1)$$
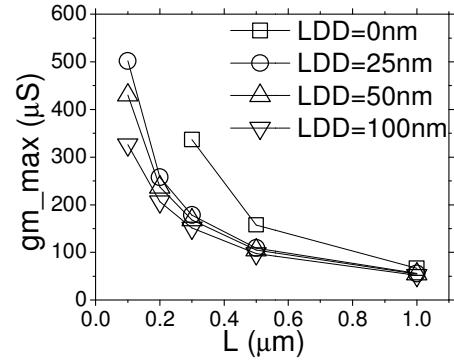
Figure 4: Maximum transconductance versus channel length for different LDD length.
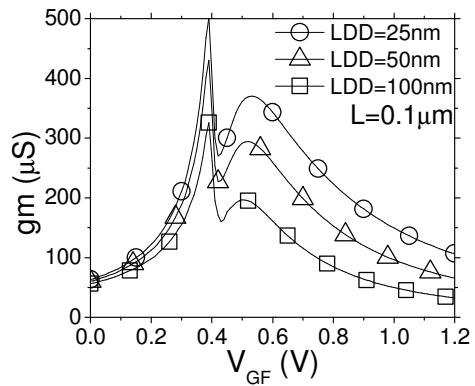
Figure 5: Transconductance as a function of gate voltage for different LDD lengths and channel length equal to 0.1 µm.

The higher values of gm_max are observed for the structures with L=0.1µm (in all cases) and for L equal to 0.3µm without LDD, as Figure 4 shows. Figure 5 indicate the existence of SCE for L equal to 0.1µm, since, there was a second peak in the transconductance versus gate voltage curve. In other words, these cases presented an inversion of the second interface by the gate voltage due to the loss of control of the channel carriers by the gate, resulting in a greater acceleration of the channel carriers and thus in a higher transconductance, or in a lower channel resistance.

Figure 4 also demonstrates a more influence of the LDD in short channel devices. This behavior is due to the increase of the series resistance caused by the addition of the LDD region, becoming this resistance more evident when compared to the channel resistance that has lower values for short channel devices.

3.2. The subthreshold slope

To confirm the SCE in the devices mentioned before (structures with L=0.1µm, considering or not the presence of LDD, and L=0.3µm and 0.2µm without LDD), it was extracted the subthreshold slope (S) of the studied devices, yielding the Figure 6, where this parameter was plotted as a function of channel length for different LDD lengths.

This parameter was also obtained by it definition, given by equation 2, in the subthreshold region, in this case, $V_{GF}=0.2V$ [5]:

$$S = \frac{dV_{GF}}{d(\log I_D)} \qquad (2)$$
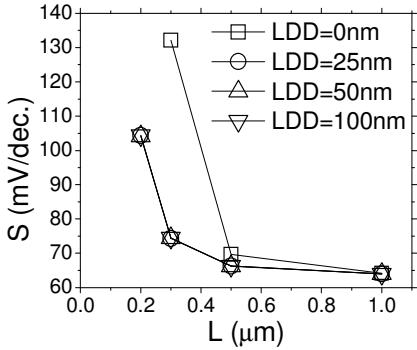
Figure 6: Subthreshold slope versus channel length for different LDD lengths.

This method yields 132.18mV/decade for channel length equal to 0.3μm without LDD and values about 105mV/decade for channel length equal to 0.2μm, confirming the existence of SCE in these devices and in that with lower channel length. For channel lengths equal to 0.3μm with LDD, 0.5μm and 1.0μm, this parameter resulted in values between 63 and 75mV/decade being closer to the ideal value of the 60mV/decade.

3.3. The threshold voltage

To quantify the SCE in the different dimensions, the threshold voltage (V_T) was extracted, using the second derivative of I_DxV_{GF} curves method [6], and the minimum length (L_{min}) with a decrease of 10% of the long channel V_T [7]. Figure 7 shows the threshold voltage as a function of channel length for different LDD lengths.
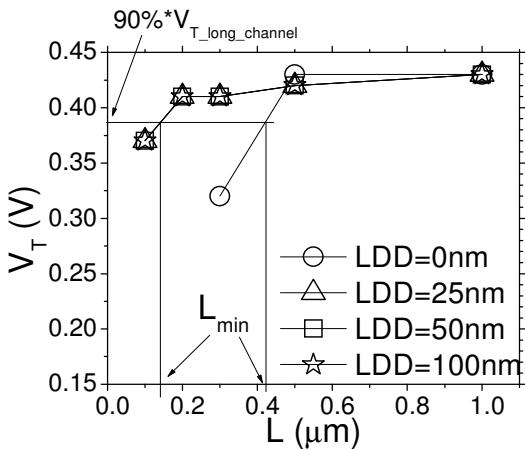
Figure 7: Threshold voltage as a function of channel length for different LDD lengths allowing the extraction of the L_{min} value.

It is possible to realize that, while the devices without LDD suffered the SCE before, presenting this effect with a greater channel length (0.4232 μm); all the devices with LDD presents a smaller minimum channel length without SCE (0.1385μm), indicating that its addition really improve the performance of the devices.

Moreover, as Figure 7 shows, all these studied LDD lengths present the same minimum channel length without SCE (0.1385μm), indicating that there was no significant difference for the studied lengths when compared this parameter only for the LDD devices. So, it is possible to guarantee the lower effective potential in the channel and lower lateral diffusion using these LDD lengths. In these structures with LDD, only the channel length is the limiting dimension for the presence of the SCE.

According to the data in Figure 6, for channel length equal to 0.2μm, the value of the subthreshold slope were about 105mV/decade, a high value comparing with the ideal case. Figure 7, however, shows that the threshold voltage has not demonstrated the SCE yet, since that, as L=0.3μm structures, the L=0.2μm devices also presented a value of the threshold voltage of 0.41V. So, it is possible to conclude that the subthreshold slope method is better to analyze the short channel effect, since that this parameter suffered the SCE for a greater channel length than that demonstrated the threshold voltage method.

3.4. The series resistance

Aiming to minimize the series resistance (R_{SD}), it was necessary to obtain its value. So the method used was Hu et al [8], where, through the drain current and the drain voltage values, the total resistance as a function of the channel length was plotted for two gate voltages for each LDD length. So, the RSD for each LDD length, was extracted by the crossover point with the y-axis of these curves, and the result can be seen in the Figure 8.
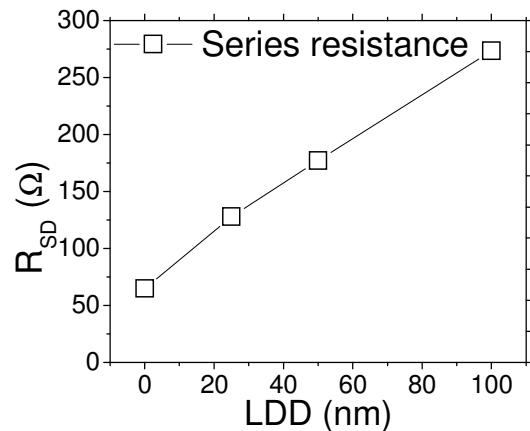
Figure 8: Series resistance as a function of LDD length.

According to the graphic presented in Figure 8, the series resistance increases with the increase of the LDD length, presenting the expecting behavior. The slope of this curve has a linear behavior, except when there is no

LDD, where the slope is a little greater. In this case, these devices do not have any LDD to increase the series resistance, however they also have a greater lateral diffusion that decreases the difference of the major series resistance due to the LDD addition.

3.5. The optimum LDD length range

Finally, to minimize the series resistance and the minimum channel length that a device may have without the SCE, it was necessary to multiply this parameter by L_{min} and plot it as a function of different LDD lengths to obtain a range for the optimum LDD length. Figure 9 and Table 2 show the obtained results.
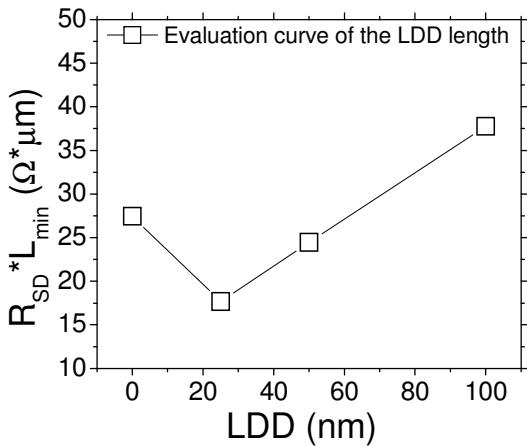
Figure 9: Curve to evaluate the optimum LDD length value (series resistance multiplied with the minimum channel length versus LDD length).

Table 2: Obtained results.

LDD (nm)	R_{SD} (Ω)	L_{min} (μm)	$R_{SD}*L_{min}$ ($\Omega *\mu$m)
0	64.83	0.4232	27.43606
25	127.95	0.1385	17.6571
50	177.08	0.1385	24.43704
100	273.52	0.1385	37.74576

For greater LDD length, the result of the product is higher due to the higher R_{SD} values. On the other hand, without LDD, the device is suffering of SCE, increasing the minimum channel length with the normal behavior and, consequently, the product yields higher. So, as indicated in figure 8, the optimum LDD length is given by the minimum value of the presented curve, resulting in a range from 0 up to 25nm for the studied devices.

4. CONCLUSIONS

A study of the influence of the LDD length on the series resistance and on the SCE was done through bidimensional numeric simulation. These parameters were quantified and evaluated and a range of the optimized LDD length was obtained.

The analysis demonstrated a linear increase of the series resistance with the LDD length, due to the lower carrier concentration. It was also confirmed the improvement of the SCE with the addition of the LDD region, due to the lower effective potential and lateral diffusion. But it did not indicate significantly influence when comparing only structures with LDD, because among the LDD length studied, these lengths are not low enough to observe any significant difference.

All of the studied parameter indicated a negligible variation of the insertion of LDD with different lengths for long channel devices since, for these structures, the channel resistance is much higher than the series resistance. As the channel length decreased, the series resistance becomes more evident than the channel's, resulting in a major sensibility of the parameters for different LDD length.

Comparing the subthreshold slope and the threshold voltage methods to determine the occurrence of the SCE, the former proved to be better than the last, showing that the first method is more sensitive than the last one.

Finally, to minimize the series resistance and the SCE, it was plotted the curve of the R_{SD} multiplied by L_{min} as a function of LDD length presenting a range of optimum LDD length from 0 to 25nm.

6. REFERENCES

[1] S. Nicolett, J. A. Martino, E. Simoen, C. Claeys, "Extraction of the lightly doped drain concentration of fully depleted SOI NMOSFETs using the back gate bias effect", Solid-State Electronics, p. 677-684, 2000.

[2] Kawamoto, S. Sato, Y. Omura, "Engineering S/D diffusion for sub-100-nm channel SOI MOSFETs", IEEE Transactions on Electron Devices, vol. 51, no. 6, June 2004.

[3] S. M. SZE, K. K. Ng, Physics of Semiconductor Devices, 3ª ed., New York, Wiley-Interscience – John Wiley and Sons, p.45, 2007.

[4] SILVACO International, ATLAS user's manual – Device Simulation Software, vol. 2, 2000.

[5] J. P. Colinge, Silicon-On-Insulator Technology: Materials to VLS, 3ª ed., Kluwer Academic Publishers, 2004.

[6] O. A. Conde et al., "A review of recent MOSFET threshold voltage extraction methods". Microelectronics Reliability, v. 42, p. 583-596, 2002.

[7] J. A. Martino, M. A. Pavanello, P. B. Verdonck, Caracterização Elétrica de Tecnologia MOS, 1ª ed., 2003.

[8] G. J. Hu, C. Chang, Y. T. Chia, "Gate-voltage-dependent effective channel length and series resistance of LDD MOSFET's", IEEE Transactions on Electron Devices, vol. ed. 34, no 12, December 1987.