A 920 MHZ CMOS PHASE-LOCKED LOOP DESIGN

Genival M. Araújo, Heider M. G. Madureira, José Camargo da Costa[1], Leonardo C. Neves[2], Rafael L. P. Martins, Rafael S.Ferreira , Reinaldo G. Pimenta

Department of Electrical Engineering, Universidade de Brasília
P.O BOX 4386, Brasília - DF, CEP 70904-970.
camargo@ene.unb.br leonardoneves@unb.br

ABSTRACT

This paper presents a 0.35µm CMOS Phase-Locked Loop (PLL) designed to synthesize the frequency of 920MHz. The PLL project includes the development of the Voltage Controlled Oscillator (VCO), the Charge Pump (CP), the Loop Filter (LF), the Phase-Frequency Detector (PFD) and the Divider.

1. INTRODUCTION

Typical receiver architectures usually have amplifiers, mixers and frequency synthesizers [3] [4]. One of the solutions for the circuit of the frequency synthesizer is a Phase-Locked Loop (PLL), which is a set of circuits in a feedback loop built to generate a signal with a certain frequency, using another signal frequency, usually lower than the output signal frequency, as a reference.

A 0.35µm CMOS Phase-Locked Loop (PLL) designed to operate at 920MHz as a part of a transceiver contained within a SoC CMOS for a wireless sensor network is developed in this paper. The complete transceiver architecture is shown in Figure 1. The PLL project includes the development of the Voltage Controlled Oscillator (VCO), the Charge Pump (CP), the Loop Filter (LF), the Phase-Frequency Detector (PFD) and the Divider.

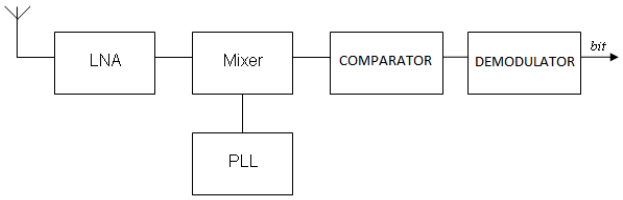

Figure 1 - Receiver Architecture.

This work is divided as follows. In section 2, all the circuits within the PLL are presented and their projects are explained. Section 3 shows the measurements results of the prototyped VCO and, in section 4, this work is concluded.

2. PLL DESIGN

The PLL is designed to synthesize the frequency of 920MHz and is composed of the Voltage Controlled Oscillator (VCO), the Charge Pump (CP), the Loop Filter (LF), the Phase-Frequency Detector (PFD) and the Divider. In the following subsections, the design of each one of these circuits will be explained in more details. The complete loop is presented in Figure 2.

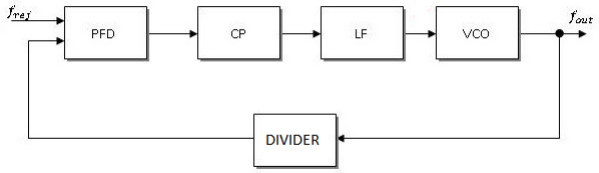

Figure 2 - PLL schematic.

2.1 Voltage Controlled Oscillator

The VCO is one of the most critical circuits to develop in a PLL. Due to the low quality factor of the inductors available in the technology, a ring oscillator topology was chosen. To avoid the need of many stages and at the same time achieve the specified frequency of 920MHz, the topology proposed on [1] was used. This topology increases in about 50% the synthesized frequency of the oscillator if compared with a conventional ring oscillator with the same number of stages. The simulated consumption of this circuit is 18 mW supplied by a 3.3V voltage source. The detailed schematic of the inverters connections is presented in Figure 3. The dimensions of the transistors, summarized on Table 1, were calculated through simulations and optimizations.

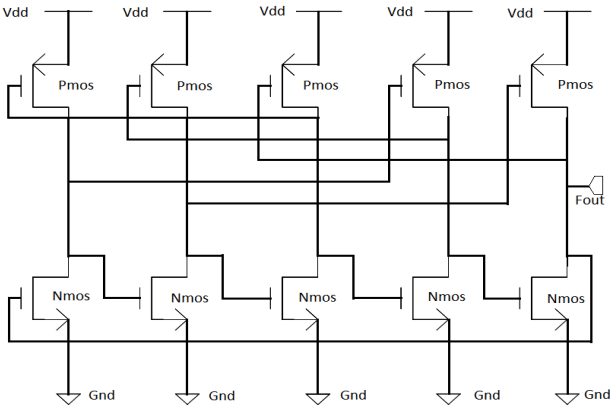

Figure 3 - VCO Schematic

Table 1- Dimensions of the transistors of the VCO

Dimension	Size (µm)
Width N type	17
Length N type	0.65
Width P type	20
Length P type	0.65

After extracting the parasitic capacitance of the layout of the VCO, a simulation was performed to verify the frequency versus control voltage characteristic. This curve is shown in Figure 4. It can be verified that this circuit is able to synthesize frequencies in the range of 880MHZ – 1GHz.

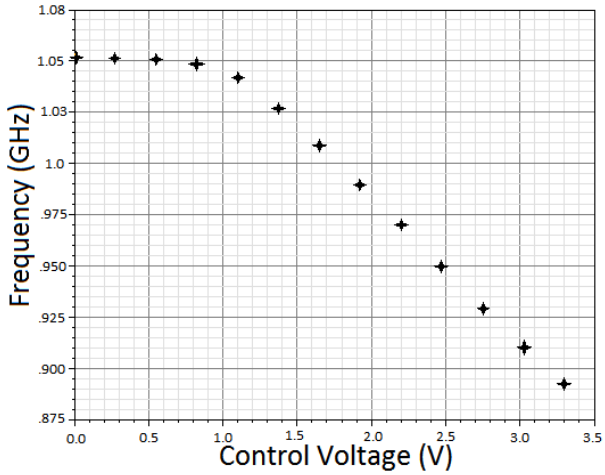

Figure 4 - VCO's Characteristic Curve Frequency versus Control Voltage

2.2 Divider and Phase-Frequency Detector

The Divider was developed to divide the frequency of the output of the VCO 42 times, so it can be compared with the 20MHz reference in the circuit of the PFD.

Due to the fact that both Divider and PFD circuits are purely digital, a digital flow of project was followed in the development of these blocks.

2.3 Charge Pump and Loop Filter

The CP is a circuit designed to function as a source or sink of current, supplying current to or retrieving current from the next stage, the LF. Its function as a source is controlled by the Down output of the PFD. Similarly, the sink function is controlled by the Up output. The current supply capacity of the CP is 20µA. Its topology, shown in Figure 5, was based on [2].

The blocks IDW and IUP in Figure 5 represent a Current Reference described in [7] that acts as a more stable current sink and current source respectively.

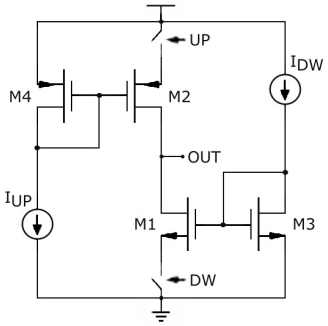

Figure 5 - Charge Pump Schematic

The LF circuit is shown in Figure 6. It is a typical circuit of a resistor followed by a capacitor and both in parallel with a second capacitor, which were placed to reduce the ripple at the output of the LF.

The behavior of the LF was simulated together with the other components of the PLL loop to verify its stabilization characteristics. Figure 7 presents the simulated results. One can see that the loop stabilizes and the required output frequency is achieved.

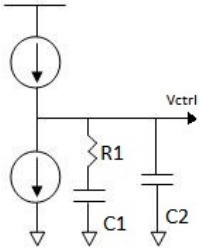

Figure 6 - Loop Filter Schematic

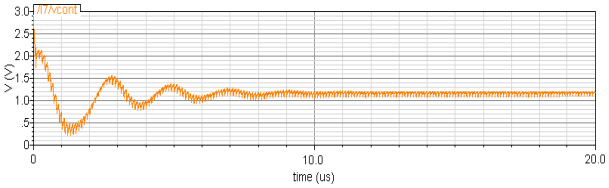

Figure 7 - LF`s Control Voltage versus Time.

3. PLL MEASUREMENTS

After prototype fabrication, the circuit of the VCO was then tested. The tests were performed using a Rohde & Schwarz 9KHz – 6GHz 50Ω function generator, a Rohde & Schwarz 9KHz – 3GHz 50Ω spectral analyzer and a Agilent E3647A 0 – 35V / 0.8A DC source. The VCO and PLL positions are highlighted in Figure 8 and Figure 9 respectively.

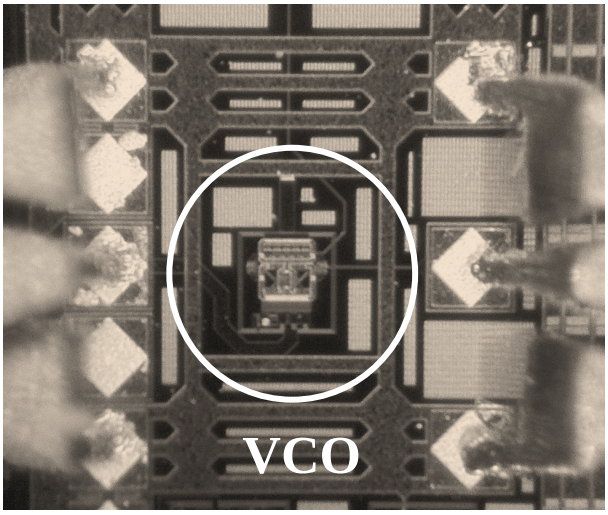

Figure 8 - VCO on chip.

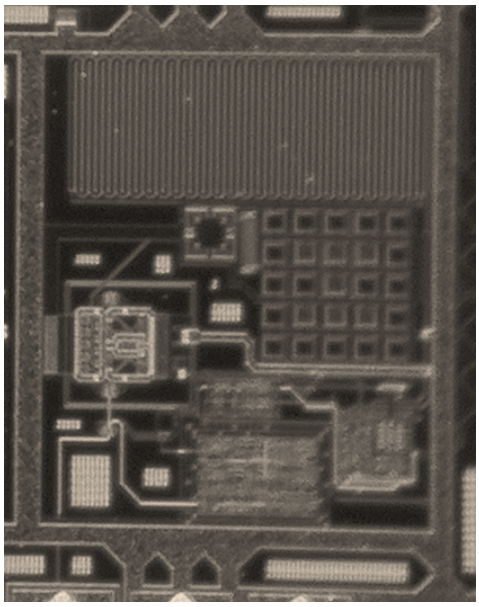

Figure 9 - PLL on chip.

The first test was the measurement of the frequency versus control voltage characteristic curve. The DC source was used to vary the control voltage from 0V up to 3.3V and, at each step, the frequency was taken from the spectral analyzer. The plot of the measured results is presented in Figure 10.

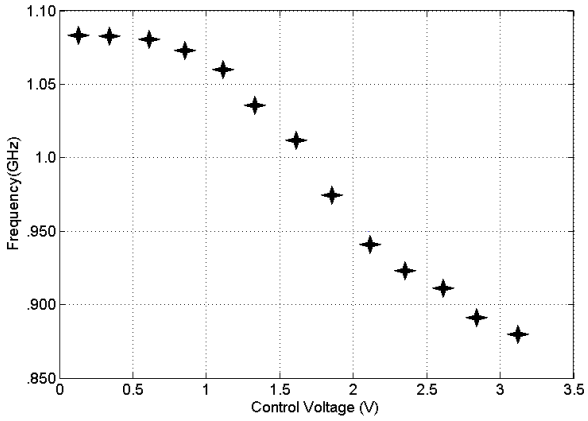

Figure 10 - Measured VCO's Characteristic Curve Frequency versus Control Voltage

It is possible to verify that the measured characteristic curve of the VCO is very close to the simulated characteristic curve of the same circuit. It validates the simulations of the circuit of the VCO and its project.

The second test performed is the VCO`s phase noise. A -79.13dBc/Hz @100KHz noise level was obtained. The result is presented in Figure 11.

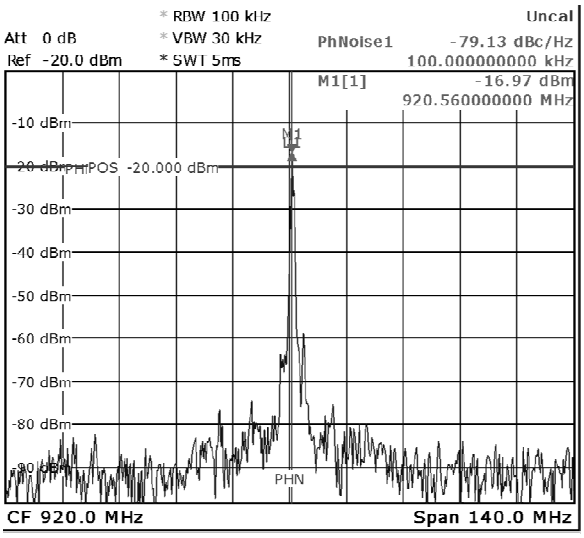

Figure 11 - VCO's measured phase noise @100KHz.

4. CONCLUSION

A 920MHz frequency synthesizer based on a PLL topology was developed in this work. An 880MHz-1GHz 18mW 3.3V VCO was designed following a non conventional topology. The circuit of the VCO was also characterized and its measured characteristic matches the one simulated. For future works, tests in the PLL circuit for its characterization are planned

5. REFERENCES

[1] LEE, Seog-Jun; KIM, Beomsup; LEE, Kwyro. *A Novel High-Speed Ring Oscillator for Multiphase Clock Generation Using Negative Skewed Delay Scheme*. IEEE Journal of Solid-State Circuit. Vol 32 NO 2, pp 289-291. 1997.

[2] RHEE, Woogeun. *Design of High Performance CMOS Charge Pumps In Phase-Locked .IEEE* International Symposium on Circuits and Systems: NewPort Beach-CA, pp. II-545-548, 1999.

[3] BEHZAD, Razavi. *RF Microeletronics*. Los Angeles, United States of America: Prentice Hall, 1998.

[4] LEE, Thomas *H.The Design of CMOS Radio-Frequency Integrated Circuits.*. United Kingdom: Cambridge University Press, 1998.

[5] MAK,Pui-In; U,Seng-Pan; MARTINS; Rui Paulo. *Analog-Baseband Architectures and Circuits for Multistandard and Low-Voltage Wireless Transceivers.*. The Netherlands: Springer, 2007.

[6] SHU,Keliu; SINENCIO,Edgar Sanchez. *CMOS PLL Sinthesizers: Analysis and Design*. The United States of America: Springer, 2005.

[7] SAINT,Christoper; SAINT,Judy. *IC Mask Design: Essential Layout & Techniques*. New York, United States of America: McGraw-Hill, 2002.