IMAGE RECOGNITION TASK BASED ON A SINGLE-ELECTRON CONTENT ADDRESSABLE MEMORY

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ABSTRACT

This paper presents a Content Addressable Memory structure, formed by memory cells, a comparative circuit and a WTA network, which compares two or more input values and gives the one with the higher voltage level. This type of memory is used to address an input parameter based on information contained in its structure. The objective of this work is to develop a circuit that can faithfully compare input with stored image data using single-electron transistors (SET). The proposed architecture was simulated several times under room temperature (300 Kelvin) for different input images sizing 35 bits each, and compared with 4 images of the same size, which were stored in the memory cells. The simulations were performed using the computational tools MATLAB and SIMON.

1. INTRODUCTION

The technological era we find ourselves in is progressively finding ways to overcome the barriers we had a few years ago. Engineering has proved to be very efficient when it comes to technological improvement, successfully responding to this new era demands. The role of electronic engineers and scientists can be resumed to developing devices that can achieve four main objectives: low physical size, good energy management, low error rate and high processing speed. In order to enhance these features on electronic devices, both architecture and material improvements are being studied. Nanoelectronic is a very promising step the world of electronics is taking. It is mathematically proved to be more efficient than the microelectronic mechanisms currently in use, mainly in terms of area and energy management.

A Single Electron Transistor (SET) differs from the traditional FET (Field Effect Transistor) and BJT (Bipolar Junction Transistor) on the fact that its structure is capable of confining electrons to sufficiently small dimensions, so that the quantization of both their charge and their energy are easily observable, making the SET's, in an essential way, quantum mechanical devices.

The functionality of this transistor can be evaluated using a computational tool called SIMON [1], which allow us to design, simulate and evaluate the performance of the proposed circuit. It makes use of capacitors and tunnel junctions to generate nanoelectronic devices. This tool however, is very inefficient when it comes to designing large circuits (such as the one presented on this paper). Therefore, the use of MATLAB becomes essential. This second computational tool has many useful gadgets that allow us to easily multiply small circuits designed on SIMON, then automatically run the simulations and plot the results.

2. PROPOSED ARCHITECTURE

The structure proposed in this paper is a Content Addressable Memory [2]. In resume, the circuit searches the data stored in memory cells, compares the input word with each of the stored words and tells us which one is closer to it. The comparison is made bit to bit, which gives us a more reliable result.

2.1 Memory Cells

This part of the circuit holds all the information to which we want to compare the input word. The architecture used in each memory cell is the one of a Flip-Flop. It has the objective of data storage and presents low output impedance, highly necessary to maintain the voltage levels for different load values. The proposed circuit for a memory cell implemented with SET's is shown in Figure 1:

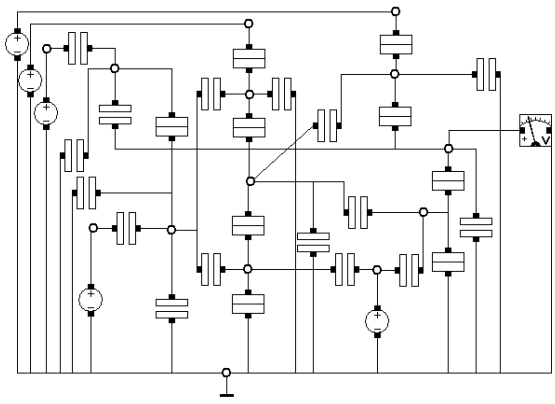

Figure 1 - Memory Cell

The voltage sources assume binary values 1 and 0 for voltage levels 1.6V and 0V. The optimal circuit was reached after several tests using SIMON.

2.2 Comparison Circuit

The second part of the circuit is the actual comparison structure, formed by logical operators that associate each input bit with the referred bit in the memory cells. This is performed using a NXOR gate, which gives us 1 for equal input values and 0 for different input values. A nanoelectronic circuit that can work well as a NXOR gate at the input voltage levels we are dealing with is shown in Figure 2:

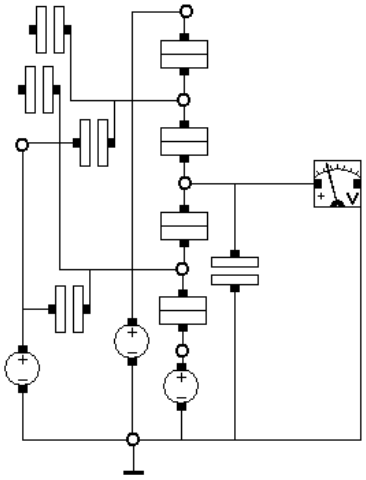

Figure 2 - NXOR Gate

The logical operator presents a good response for input voltages of 1.6V and 0V

2.3 WTA Network

Every output for these logical gates are linked together in a single node, inserted in a network called WTA (Winner Takes All) [3], which gives us the best match for the "word" (sequence of bits) we want to associate them with. The WTA network used has four input nodes, one for each stored word in the circuit. Figure 3 shows the proposed circuit for the network in question.

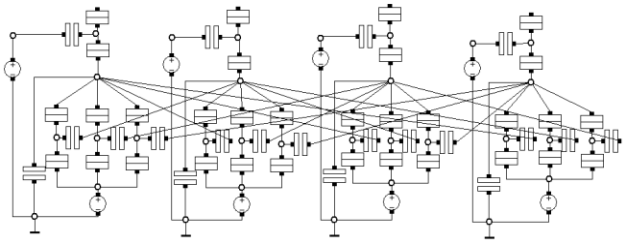

Figure 3 - WTA Network

2.4 Complete Circuit

Having presented all the partials of the Content Addressable Memory, MATLAB was programmed to put them together, multiplied in as many cells as wanted. The only variable missing is the number of bits (size) each word will have. It was estimated 35 to be a good size for an image (5x7 pixels), due to the facility of drawing letters and numbers of this particular size. Because of limitations on the computational tool, larger circuits were proved hard to simulate, taking almost 50 hours for SIMON to run a single simulation of a 64 bit word and four comparison words for a simulation period of 2 nanoseconds and time step of 2 picoseconds. On MATLAB, we used a circuit designing tool called SIMULINK, and with the help of a code previously programmed, we were able to associate each part of the circuit to a block at SIMULINK, and then easily multiply the blocks to reach the circuit size expected.

An important observation to make is the number of components used in the whole circuit. Each memory cell contains 9 junctions and 16 capacitors, each NXOR gate contains 4 junctions and 5 capacitors, and the WTA network has 32 junctions and 20 capacitors. As the whole circuit contains 140 memory cells, 140 NXOR gates and a WTA network, that leaves us with 1852 tunnel junctions and 2960 capacitors.

3. RESULTS AND DISCUSSION

To test the proposed circuit, 35 pixel images (letters and numbers) were drown, and then translated to a 35 bit binary word. The best match with the input figure should be given by the lowest Hamming Distance [4] (of all the four) from it. Hamming Distance how different a word is from another in bits, or how many different bits two words have between each other. Figure 5 shows an example of 9 images used for comparison, with their corresponding binary codes.

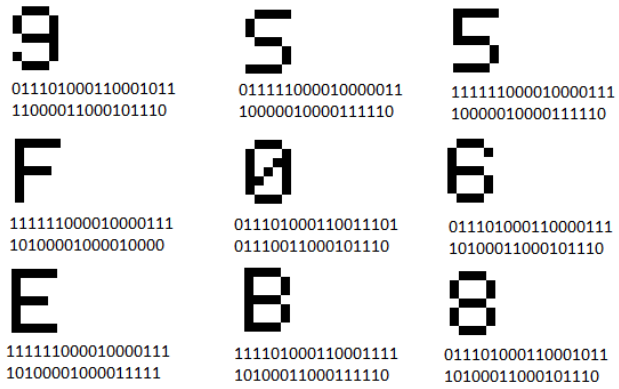

Figure 4 - 35 bit Symbols

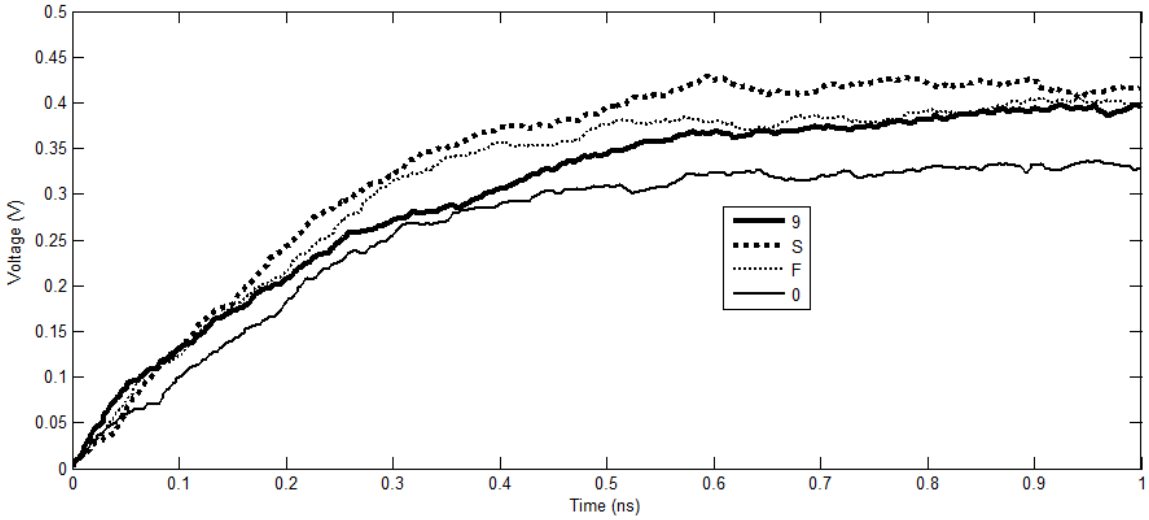

Figure 5 - Simulation Results

The first test was made with the input number "5", compared to "*9*", "*S*", "*F*" and "*0*". The expected match was, of course, the letter "S", with the lowest Hamming Distance from the number "5" (only 2 different bits). Several other tests were simulated in order to prove the circuit's functionality for every case, but we show (in Figure 5) only the results for one of them.

Table I shows the average voltage level at stability time (0.8 to 1 nanosecond) for each compared word, and helps us to better understand the results from the graph.

TABLE I: Numerical Results

Comparison Symbol	Hamming Distance	Voltage Level [V]
9	8	0.39
S	2	0.43
F	7	0.40
0	12	0.32

We can see that, at the stability time, the voltage level of each word follows a pattern according to the Hamming Distance of that word to the input (the level grows for smaller distance values). The relation between these two variables is, however, not linear, due to the complexity of the WTA Network and the way its outputs depend on each other.

Another important fact noticed during the studies is, as larger circuits were tested (up to 64 bits images), the voltage difference for words that have almost the same Hamming Distance was very low, making it almost impossible to tell which word is the winner. In order to make larger circuits work properly, it would be necessary to propose new architectures for the presented circuits or change the values of the material used (capacitors and junctions).

4. CONCLUSIONS

The results obtained from the simulations on the proposed circuit were satisfactory when it comes to identifying the winning word (best match) for the input parameter. Evaluating the voltage level at the output of the WTA network, we observe a very low difference between all four comparison words, which makes it harder to identify the highest level, requiring a precise mechanism to do so. It is important to notice that the results were obtained for a large-scale single-electron circuit, and the fact that these circuits were simulated at room temperature is essential for a future implementation of these systems, but to achieve such goal and to guarantee its utility, a larger circuit design is needed.

ACKNOWLEDGEMENTS

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5. REFERENCES

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