STUDY OF SOURCE AND DRAIN GEOMETRY IMPACT ON SERIES RESISTANCE OF TRIPLE GATE FINFETS

Arianne Soares do Nascimento Pereira, Paula Ghedini Der Agopian, Renato Giacomini

Centro Universitário da FEI

ABSTRACT

The focus of this work is a comparative study of silicide film thickness influence in the series resistance for two fin geometries: rectangular and trapezoidal. The series resistance dependence on the silicide thickness presented different behaviors for the two fin geometries. The trapezoidal fin presented series resistance values around 10% lower than rectangular fin, due to its larger area. The minimum values of the series resistance were obtained for different silicide depth depending on the source/drain shapes.

1. INTRODUCTION

The FinFET is a promising alternative to continue the evolution of semiconductor devices in nanometric scales. The multiple gates and the narrow fin width allow a better coupling, decreasing short channel effects (SCE) [1]. However, sources and drains made in thin fins have a high resistance. This resistance is a parasitic effect called Source/ Drain series resistance.

The contact resistance of source and drain regions dominates the S/D series resistance [2]. This resistance can be reduced with larger contact areas by using silicides in contacts: lower resistivity materials made of silicon and a metallic material in order to reduce the resistance between silicon and contact. A widely used silicide is NiSi that has resistivity of 10 μΩ.cm [3] while the Si resistivity at 300 K is 1000 μΩ.cm for a doping concentration of $1x10^{20}cm^{-3}$ [4]. Recent studies show substantial variation in S/D series resistance when different silicide film thickness and geometries are used [5].

In multiple-fin structures, several FinFETs are connected in parallel with the purpose of increasing the current drive of the array. The multiple connections create a raised source and drain contact areas. This change in contact area may also modify the S/D series resistance. Thus, it is worth to consider structures as closer as possible to a real one in the study. Figure 1 is an approach of a multiple-fin structure created from a trapezoidal shape, the same geometry described in Silvaco ATLAS Simulator for the present study.

This work presents a comparative study of S/D series resistance with the purpose of investigating the influence of silicide film thickness for two fin geometries: the rectangular fin and the enlarged fin.

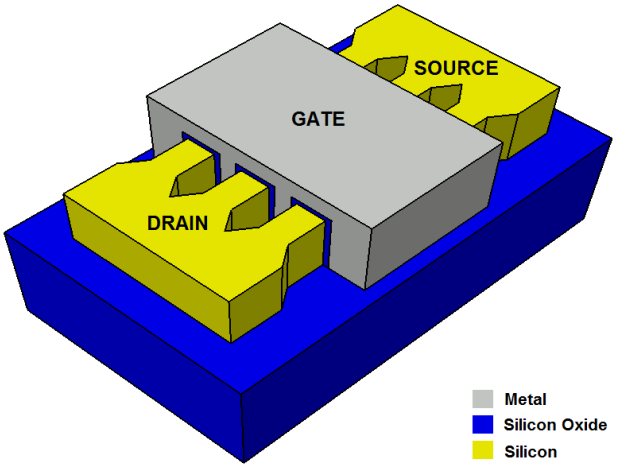

Figure 1: Multiple-fin structure described from a trapezoidal shape.

2. DEVICE STRUCTURE AND SIMULATIONS

The simulations were performed in Silvaco ATLAS Simulator. Two basic fin geometries – rectangular and trapezoidal – with the following characteristics were described (Figure 2): channel length (L) of 100 and 150 nm, source and drain extension length (L_{SP}) of 50 nm, source and drain silicide/ HDD length (L_S) of 100 nm, fin height (H_{FIN}) of 50 nm, silicide film thickness (H_S) varying from 10 to 45 nm, gate oxide thickness of 1.5 nm, buried oxide thickness of 150 nm, buried oxide width of 100 nm, p-type channel doping concentration of 10^{15} cm^{-3}, n-type extension source and drain doping concentration of 10^{19} cm^{-3}, n-type HDD source and drain doping concentration of 10^{20} cm^{-3}. For the rectangular fin, the fin width (W_{FIN}) is the same along the whole fin length, i.e. from source to drain (Figure 2A). For the trapezoidal fin, the silicide/ HDD source and drain areas have a trapezoidal shape, with 100 nm width (W_S) in two edges (Figure 2B), in order to have the approach of real situation showed in Figure 1.

The two structures were simulated considering a contact resistivity of 10^{-8} $\Omega.cm^2$ [5]. It was observed the total current density and compared the influence of silicide film thickness (H_S) in series resistance for each case: rectangular fin and trapezoidal fin. Besides, the drain current and transconductance curves for a low drain voltage bias (V_{DS} = 50 mV) were extracted and compared.

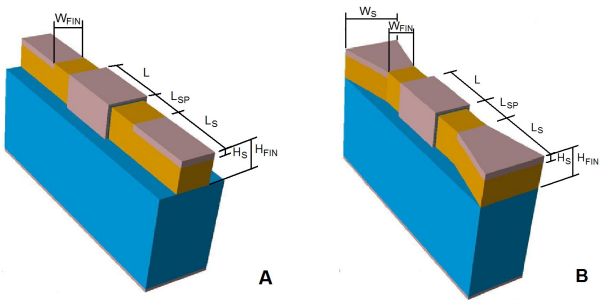

Figure 2 – The source /drain geometries of FinFETs studied by simulations. A: Rectangular fin; B: Trapezoidal fin.

3. RESULTS AND DISCUSSION

The series resistance can be observed in Figure 3. The Terada e Muta method [6] was applied to extract the series resistance values. For this reason two channel lengths (100 and 150 nm) were used in simulations. Notice that the trapezoidal fin geometry has lower resistance values than the rectangular fin, due to its larger area. Moreover, the lowest series resistance for each structure appears for different silicide film thickness values: 35 nm for rectangular fin and 10 to 30 nm for trapezoidal fin. This happens because in trapezoidal fin geometry, most of the current flows below the silicide film, due to the higher area of this region, while in the rectangular fin, most of the current flows through the lateral contact of the silicide. For thicker silicide films (above 40 nm) both series resistance increases, because the path below the silicide film becomes throttled, so the easier current path are the lateral contacts for both fin geometries. In such case, not always the larger contact area means the lower series resistance.

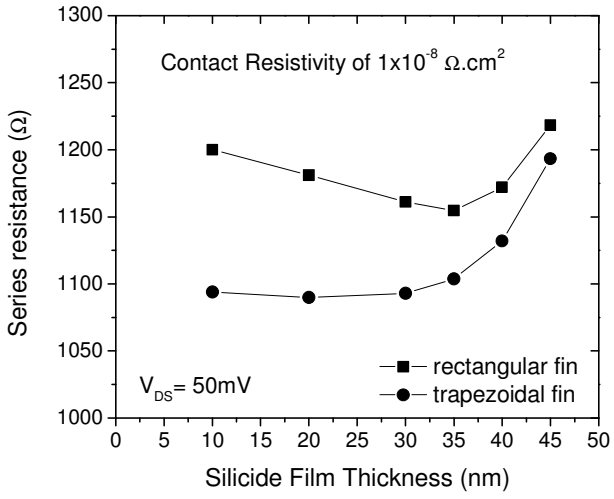

Figure 3 – The total series resistance with silicide film thickness variation (H_S).

The current behavior is showed in Figure 4, where the current densities are ploted in silicon fin of α plane (Figure 4A). It can be observed a higher current density below silicide film of 20 nm in the trapezoidal fin geometry. This phenomenon is called current crowding [7] and is more significant in larger contacts, where most of the current will flow only in a fraction of the contact, while in the rest of contact only a negligible current will flow. For silicide films of 40 nm, the behavior of current in two geometries is more similar, due to the strangulation of the area below silicide film, but the current crowding can still be observed in trapezoidal fin.

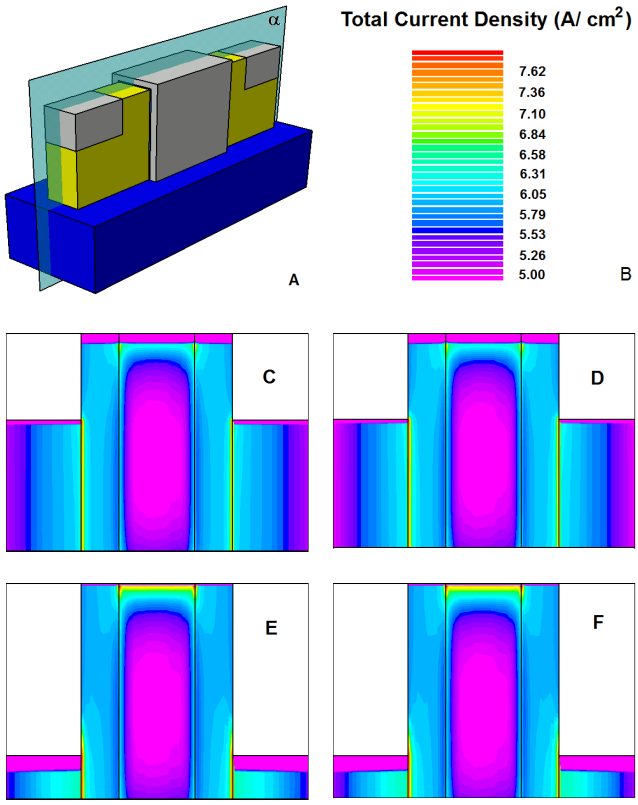

Figure 4 – Total current density – A: Rectangular fin described in simulator with the cut plane representation for current density view; B: Total current density scale; C: Current density in α plane for rectangular fin and H_S of 20 nm; D: Current density in α plane for trapezoidal fin and H_S of 20 nm; E: Current density in α plane for rectangular fin and H_S of 40 nm; F: Current density in αplane for trapezoidal fin and H_S of 40 nm.

In Figure 5 is showed the I_{DS} x V_{GS} curves, notice that the higher values of drain current appear in trapezoidal fin geometries, according to series resistance results.

Figure 6 shows the transconductance curves. This is an important parameter to demonstrate the drivability of MOS devices [8]. When the focus is the series resistance, the most important region in Figure 6 is the gm degradation at higher gate voltages. Although the gm degradation difference between the trapezoidal and

rectangular shape is not high, a smaller degradation can be observed for the trapezoidal shape, due to the lower series resistance.

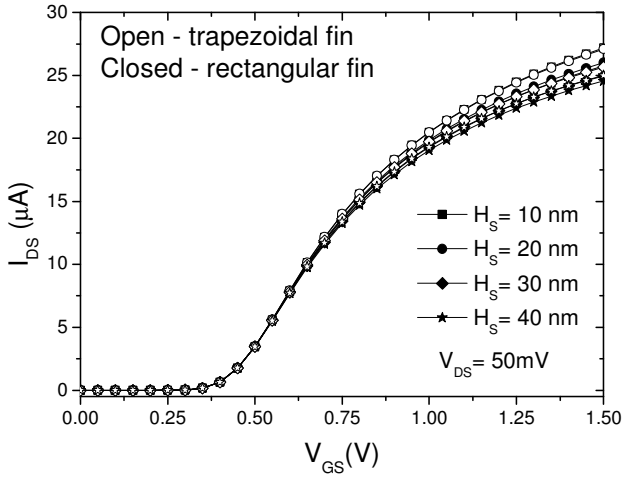

Figure 5 – Drain current versus the applied gate voltage curves for different silicide thicknesses for both trapezoidal and rectangular source/drain shapes.

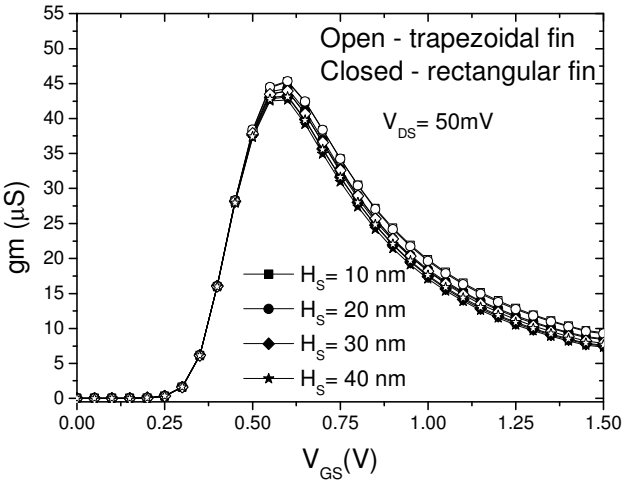

Figure 6 – Transconductance behavior as a function of gate voltage for trapezoidal and rectangular source/drain shapes for different silicide thicknesses.

4. CONCLUSION

The results evidence the importance of considering different source and drain geometries in series resistance studies, since the lowest value of series resistance to each geometry appears for different silicide films thickness. In addition, the trapezoidal fin geometry presented lower series resistance than the rectangular one, around 10% lower values, due to its area gain. Besides, it was presented a way to improve the simulation accuracy by approximating the simulation geometries to real structures.

5. ACKNOWLEDGEMENTS

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6. REFERENCES

[1] Colinge, J.P., *FinFETs and Other Multi-Gate Transistors*, Springer, New York, 2008.

[2] A. Dixit, N. Collaert, M. Goodwin, M. Jurczak, and K.D. Meyer, "Analysis of the Parasitic S/D Resistance in Multiple-Gate FETs," *IEEE Transactions on Electron Devices*, Volume 52, No. 6, pp. 1132-1140, 2005.

[3] B. Meyer, U. Gottlieb, O. Laborde, H. Yang, J.C. Lasjaunias, A. Sulpice, and R. Madar, "Intrinsic Properties of NiSi," *Journal of Alloys and Compounds*, Volumes 262-263,pp. 235-237, 1997.

[4] Colinge, J.P., and C.A. Colinge, *Physics of Semiconductor Devices*, Springer Science, New York, 2002.

[5] Y. Omura, K. Yoshimoto, O. Hayashi, H. Wakabayashi, and S. Yamakawa, "Impact of Metal Silicide Layout Covering Source/ Drain Diffusion Region on Minimization of Parasitic Resistance of Triple-Gate SOI MOSFET and Proposal of Practical Design Guideline," *Solid State Electronics*, Volume 53, pp. 959-971, 2009.

[6] K. Terada, and H.Muta, "A New Method to Determine Effective MOSFET Channel Length," *Japanese Journal of Applied Physics*, Volume 18, No. 5, pp. 953-959, 1979.

[7] Martino, J. A., Pavanello, M. A., and Verdonck, P. B., *Caracterização Elétrica de Tecnologia e Dispositivos MOS*, Thomson, São Paulo, 2003.

[8] Gentine, B., *A Study of the Potential of SOI Technology for Analog Applications*, Catholic University of Louvain, Louvain, 1996.