# STUDY OF DIFFERENT TRIPLE-GATE STRUCTURES THROUGH 3D DEVICE SIMULATION

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## ABSTRACT

The purpose of this work is to compare five different Triple-Gate devices performance: Bulk, SOI (Silicon-On-Insulator), Pi-Gate SOI, DSOI (Drain Source On Insulator) and M-DSOI (Modified Drain Source On Insulator) through the basic parameters (subthreshold slope, maximum transconductance and drain current) and internal electrical variables (current density and electric field distribution). Although all structures presented almost the same subthreshold slope when the drain current and maximum transconductance are evaluated the DSOI structure presented best behavior (higher values) due to this structure combine the benefits of the bulk FinFET (smaller self-heating effect) and the benefits of SOI (better coupling).

## 1. INTRODUCTION

Academic researches, industry investments and innovations in semiconductor area show increasingly that multiple gate devices will replace the conventional planar MOS devices. The adoption of scaling down forces the channel control improvement by gate, to avoid short channel effects (SCE). A possible solution is the migration for multigate structures as Intel announced in [1].

The FinFET is a promising candidate to substitute the conventional planar devices and to continue the evolution in nanometric scales. It has characteristics as a better coupling, the current paths in both side of the fin and the parasitic effects lowering that contribute to superior scalability [2].

Normally, FinFETs may have one of two substrate implementations: the Bulk FinFET in Fig. 1(a), and the SOI FinFET in Fig. 1(b).

The Bulk FinFET has some advantages such as low cost patterning, high heat transfer rate and the optimization of device level dc characteristics. On the other hand, this type of structure has also some disadvantages as the subthreshold slope and the lower gate control of the channel charges. In subthreshold regime it is possible to observe that leakage current appear naturally under the channel region, with consequences for the device performance.

The SOI FinFET has great advantages as low junction capacitances compared to Bulk, lower short channel effects, notorious protection against radiation and excellent subthreshold characteristics. It has two notable disadvantages: a thermal transfer problem and the floating body effect [3].

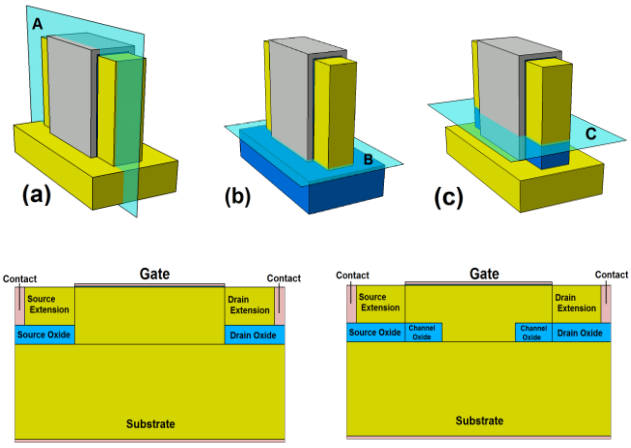


**Fig. 1. Simulated structures and peculiarities. (a) Bulk FinFET; (b) SOI FinFET/ Pi Gate FinFET; (c) DSOI/ M-DSOI FinFET; (d) DSOI vertical plane A; (e) M-DSOI vertical plane A.**

The thermal transfer or self-heating problem affects the carrier mobility. The buried oxide has a much higher thermal resistivity than the bulk silicon [4].

The Pi Gate SOI FinFET is similar the SOI FinFET, [5], but the gate electrode is extended down, inside the buried oxide preventing the drain electric field lines to reach the channel region.

The DSOI FinFET [6] as shown in Fig. 1(d) has a silicon oxide under the extension regions and above substrate region. The M-DSOI FinFET [7] as shown in Fig. 1(e), equally to DSOI, has the buried oxide under the extensions but also under part of the active region. Both have excellent properties (low leakage current and low junction capacitances), similar subthreshold slope compared to SOI structures preserving the good thermal conduction of the Bulk structure.

Moreover, the M-DSOI and the DSOI devices suffer the gate influence in window under the channel until the substrate. With the gate aligned to the oxide extension is guaranteed to carriers a strong control for the leakage current flows over the depth channel region, being the devices immune to self-heating, preserving some parameters as drain current level and increasing the device speed.

## 2. DEVICE SIMULATION

The simulations were performed using the 3D numerical simulator – Atlas, Silvaco [8]. The FinFET structures were simulated in simulator with the following

characteristics: drain/ source concentration of $8x10^{19}cm^{-3}$, channel doping concentration of $1x10^{15}cm^{-3}$, buried oxide thickness of 150nm, channel length (L) of 150nm, fin width of 50nm and fin height of 60nm. For DSOI FinFET and M-DSOI FinFET a higher fin height were necessary in order to introduce 30nm of $SiO_2$ under the source and drain extensions keeping the same transistor active area. For M-DSOI, the extension of the buried oxidation length under the transistor active area is equal to a quarter of channel length. Finally, the Pi Gate SOI FinFET has the same characteristics of SOI FinFET, except that the gate penetrates 30nm into the buried oxide.

In terms of polarization, the gate voltage was ranged from 0V to 1.5V in triode mode ($V_{DS}$=50mV).

Two planes (A and B), were obtained for all structures owing to evaluate in order the current density and the electric field distribution. Moreover, for D-SOI and M-DSOI structures was also adopted the plane C to evaluate the electric field distribution before the window under the channel. These plans are represented in Fig. 1 and distributed in each structure for a better visualization. For all structures, the plane A is vertical and parallel to the lateral channel and the plane B is horizontal next to substrate region. The plane C presents only in the DSOI and the M-DSOI structures is horizontal and 30nm above the substrate.

## 3. RESULTS AND COMPARISONS

In the next topics, was made a comparison among the different presented structures regarding some basic parameters (drain current, subthreshold slope and transconductance), and some internal variables (current densities and electric field distribution along some selected planes in devices).

### A. BASIC PARAMETERS

Figure 2 shows the drain current as a function of the gate voltage ($I_D$x$V_G$) five simulated structures. It is easy to see that the higher current level is obtained for DSOI FinFET structure. It occurs due to the better charges control by the gate since the buried oxide under the source and drain regions reduces the lateral field influence on the channel. In addition the absence of oxide under the channel region results in a better heating dissipation and consequently a better self heat effect.

The M-DSOI had the second higher current level because looks like DSOI except for it has smaller window under the channel. The Bulk device has the worst current level because it is low coupled and it starts the current curve with difference from the others [9].

The Pi-Gate and the SOI FinFET had the similar results compared with M-DSOI due to the silicon oxide presents in substrate has more resistivity than silicon substrate.

The subthreshold slope (SS) was showed in Figure 3. From figure 3 it is easy to see that unlike the Bulk FinFET, the DSOI and M-DSOI had the similar slope compared with SOI and Pi Gate SOI because it suppressed leakage current at the subthreshold region.

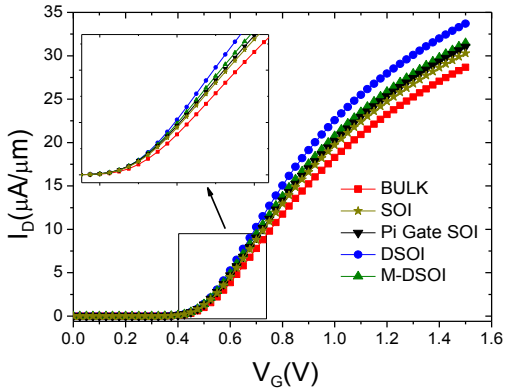


**Fig. 2. $I_D$ x $V_G$ curve for Bulk, SOI, DSOI, Pi Gate SOI, and M-DSOI FinFET devices.**

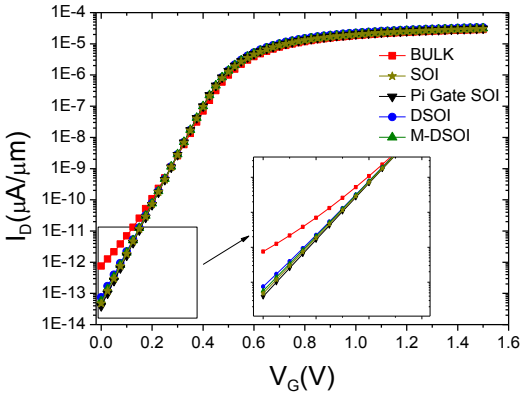


**Fig. 3. Subthreshold Slope (SS) for Bulk, SOI, Pi Gate SOI, DSOI and M-DSOI FinFET devices.**

Other basic parameter studied in this work was the transconductance. This parameter was obtained through first derivate of the drain current as expressed in eq. 1.

$$g_m = \frac{\partial I_D}{\partial V_{GS}} \qquad \text{eq. 1}$$

Figure 4 shows that the maximum transconductance was observed in the DSOI and the M-DSOI devices, demonstrating the best driving capability for these structures [10].

Another important analysis is the gm degradation. After the maximum value of gm the curve showed higher degradation in DSOI and lower degradation in Bulk FinFET exclusively the construction features.

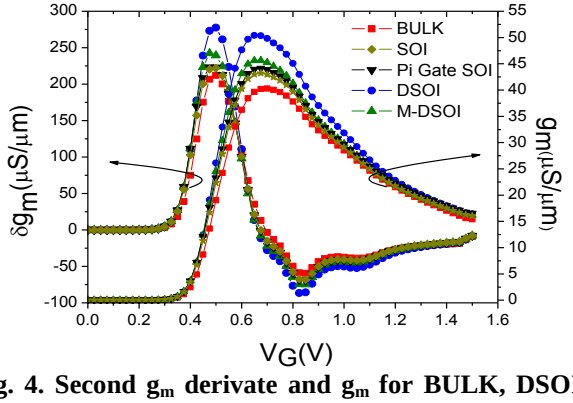


**Fig. 4. Second $g_m$ derivate and $g_m$ for BULK, DSOI, M-DSOI, Pi Gate SOI and SOI FinFET devices.**

The threshold voltage was extracted using the second derivative method [11]. The analyzed threshold voltage values are constant for all devices as can be seem in Figure 4.

Comparing the basic values parameters in Table 1, it can be noticed that DSOI presented the best values for drain current in triode mode ($V_G$ =1V) and best $gm_{max}$ because it combines some good characteristics of SOI FinFET and Bulk FinFET. The SS was similar to all structures except the Bulk FinFET with 80mV/dec.

**TABLE 1. Basic parameters results.**

| Type of transistor | Id (A/m) Vg=1V | S (mV/dec) | $gm_{máx}$ (µS) |
|---|---|---|---|
| Bulk | 0.1827 | 80 | 40.2818 |
| SOI | 0.1970 | 63 | 43.2066 |
| Pi Gate SOI | 0.2019 | 62 | 44.1466 |
| DSOI | 0.2257 | 65 | 50.3944 |
| M-DSOI | 0.2076 | 64 | 45.6342 |

## B. INTERNAL ELECTRIC VARIABLES

For each structure, the current density and the electric field distribution were analyzed in specific plans. Figure 5 shows for five devices that the current density was obtained in plane A as shown in Fig. 1.

Figure 5(a) shows the current density in Bulk FinFET. It is possible to observe that the higher leakage current under the fin and through the silicon substrate, which causes the worst S. The leakage current is also observed in Figures 5(d) and 5(e) proportionately to the window under the channel until the substrate. This behavior corresponds to consider that the D-SOI and the M-DSOI devices present lower leakage current compared with the Bulk because they suffer the strong control influence aligned to the gate extension. On the other hand, the five structures showed similar current density due to almost did not have difference among the color diagram that represents the current density values from drain to source regions.

Figure 6 shows for all devices the electric field distribution that was obtained in plane B as shown in Fig.1. For DSOI and M-DSOI were also used the plane C representing the electric field distribution above 30nm of the substrate. In terms of polarization, was considered gate voltage ($V_{GS}$) equal to 1.5V. It is possible to observe the volume inversion or maximum electric field close to corner gate due to be close to maximum potential applied.

The electric field is responsible to carriers control. It is dependent of coupling, geometry, impurity distribution and potential applied (drain and gate voltage).

Figure 6 (a), 6(b) and 6(c) show the similar electric field distributions along the device due to bias conditions. In this situation, the carriers are inverted and the channel is formed. On the other hand, Figures 6(d) and 6(e), shows that electric field along the depth is decreased presenting some differences compared with the top interface represented in plane C, as see in Figures 6(f) and 6(g).

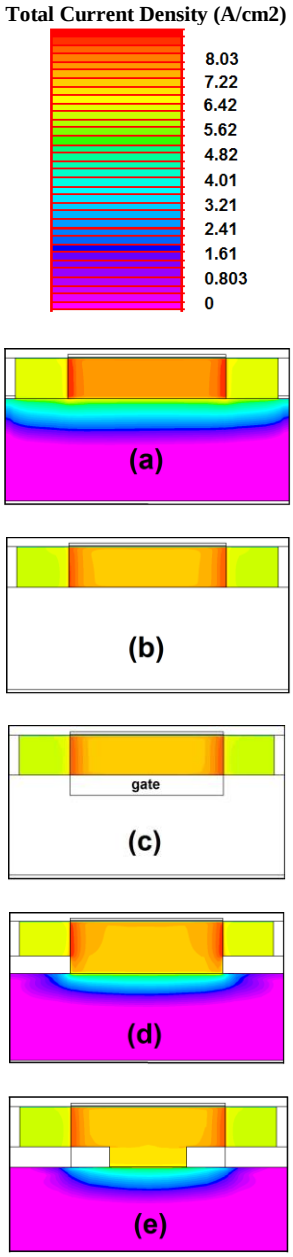


**Fig. 5. Current density for five transistors using plane A. (a) Bulk FinFET; (b) SOI FinFET; (c) Pi Gate SOI FinFET; (d) DSOI FinFET; (e) M-DSOI FinFET.**

In general, the transistors showed similar electric field distribution close to double gate due to volume inversion and channel formation, depletion regions and potential. In these five structures the field lines along the depth presented lower values because in this situation, it depends to the geometric distributions determined by features construction and bias conditions.

Finally, considering the electric field distribution expressed in plane B the structures did not have considerable differences. Through the color diagram values in all transistors was noticed smaller variations, proving that five transistor have the similar electric field distribution or the same linear distribution independently their construction features.

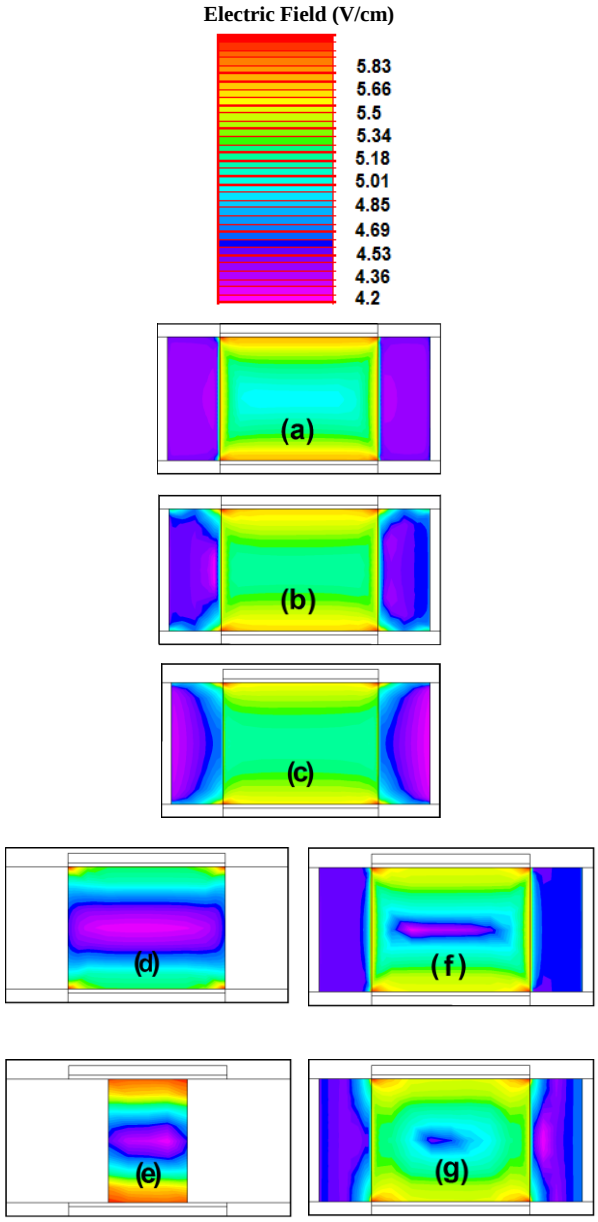


**Fig. 6. Electric field distribution for five transistors using plane B: (a) Bulk FinFET; SOI FinFET (b); Pi Gate SOI (c); (d) DSOI FinFET; (e) M-DSOI FinFET. Electric field distribution for five transistors using plane C: (f) DSOI FinFET; (g) M-DSOI FinFET.**

## 4. CONCLUSIONS

This study showed a comparison involving five transistor implementations, some being improvements of Bulk FinFET and another of SOI FinFET.

The transistor DSOI had a better performance expressed by drain current, maximum transconductance, and low leakage current. It is unlike Bulk due to coupling gate and window under channel to dissipate heat.

The five devices also had the same electric field distribution and almost at the same threshold voltage. In terms of SS all transistors, except the Bulk FinFET had the worst subthreshold slope due to higher leakage current around the device. The simulation results showed that the best values will be obtained in different structures combining the benefits for reduction of the parasitic effects with bias conditions, not assuming that the same device is necessarily the best for all comparison criteria.

## 5. ACKNOWLEDGEMENTS

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## 6. REFERENCES

[1] Courtland, Rachel, "Intel Transistors Enter the Third Dimension", *Tech Talk- IEEE Spectrum Inside Technology*, May 2011.

[2] Manoj C.R., M. Nagpal, D. Varghese, V. R. Rao, "Device Design and Optimization Considerations for Bulk FinFETs", *IEEE Transactions on Electron Devices*, vol. 55, no.2, pp. 609-615, February 2008.

[3] C. Wensong, T. Lilin, L. Zhijian, "A Novel Drain/ Source on Insulator (DSOI) Structure to Fully Suppress the Floating-Body and Self-Heating Effects ", *5th IEEE International Conference on Solid- State and Integrated Circuit Technology (ICSICT)*, IEEE Press, Beijing (China), pp. 575-578, 1998.

[4] P. He, X. Lin, B. Jiang, L. Liu, L. Tian, Z. Li, Y. Dong, M. Chen, X. Wang, "Measurement and Simulation of Electrical and Thermal Property of Drain and Source on Insulator MOSFETs (DSOI)", *2002 IEEE International SOI Conference*, Virginia (USA), p. 55-57, October 2002.

[5] Park J.-T., Colinge J.-P., Diaz C.H., "Pi Gate SOI MOSFETs", *IEEE Electron Device Letters*, vol.22, no.8, pp. 11-17, October 2007.

[6] J. Liu, Z. Luo, H. Yin, H. Zhu, H. Wang, F. Yuan, "Low Leakage Bulk Silicon Substrate Based SDOI FinFETs", *10th IEEE International Conference on Solid- State and Integrated Circuit Technology (ICSICT)*, IEEE Press, Shanghai (China), pp. 1820-1822, November 2010.

[7] J. Bo, H. Ping, T. Lilin, L. Xi, "A Modified DSOI (Drain/ Source on Insulator) Device Structure with Better Electrical Performance", *23rd International Conference on Microelectronics – MIEL 2002)*, IEEE SSCS, Nis (Yugoslavia), vol. 2, pp. 487-490, 2002.

[8] *ATLAS User´s Manual*, version 5.14.0.R, Silvaco, California (USA), October 2008.

[9] Colinge J.-P.,"From Gate-All-Around to Nanowire MOSFETs", *International Semiconductor Conference, 2007 – CAS 2007)*, Sinaia (Romania), vol.1, pp. 11-17, October 2007.

[10] Martino, J. A.; Pavanello, M. A.; Verdonck, P. B., Caracterização Elétrica de Tecnologia e Dispositivos MOS, Thomson, São Paulo, pp. 91-99, 2003.

[11] Gentine, B., *A Study of the Potential of SOI Technology for Analog Applications*, Catholic University of Louvain, Louvain, 1996.