A 2.45 GHz CMOS Differential RF Driver Amplifier

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***Abstract* – In this paper is presented a 2.45GHz CMOS fully integrated RF Driver Amplifier. This amplifier has two switchable power gain modes: high gain mode (HG) and low gain one (LG), whose control is established by a single digital input. It also has a power down control to save power. According to simulation results, this RF pre-amplifier has the following characteristics: 33.3% power added efficiency; 10.12dB gain and 11.35 dBm output 1dB compression point.**

I. Introduction

Power amplification is a key function for radio front-ends. Its performance directly impacts on many system parameters such as communication range, Quality of Service (QoS) and power consumption [1]. Since there is an inherent trade-off between linearity and power gain [1], it is a well-known design practice dividing the power amplifier (PA) into two stages in order to achieve optimal linearity and power gain performance: the first stage of this block is then a pre-power amplifier (PPA), a circuit intended to provide a high gain for subsequent high power stage. This paper objective is to present the design, simulation and layout of a PPA for a Wifi IEEE 802.11b front end.

The designed amplifier features a digital gain control input for increased dynamic range and a digital power down input for decreasing power consumption during non-transmitting periods. The circuit operates in class AB in a fully differential topology which was chosen for better linearity purpose.

The organization of this paper is as follows. Section II describes the design approach of the PPA. Sections III and IV exhibit simulation results and layout of the proposed pre-amplifier. Finally, the conclusion summarizes in section V.

II. Design principle

In order to conceive the pre-power amplifier, a differential pair topology has been used: which improves linearity and common mode rejection [2]. Since the common mode noise has not a significant impact on the differential signal in a PPA [3]; the differential pair is implemented without any tail current source in order to easy the current increasing.

The transistor is biased to operate in the class AB, which means that the conduction angle ranges between $180°$ and $360°$. In this class, decreasing the conduction angle implies an efficiency increasing. However, one reduces the amplitude of the fundamental component of the output current [4]. Therefore, the choice of the conduction angle is a compromise between efficiency and linearity.

The bias voltage is determined taking into account the desired conduction angle: the transistor gate voltage lies between threshold voltage V_{TH} and $V_{GS_{max}}$; if the conduction angle is $360°$ (class A), there would be a sinusoidal voltage V_{GS} with the bias voltage as an offset (1).

$$V_{GS} = V_{GS_{DC}} + (V_{GS_{max}} - V_{GS_{DC}}) \times \sin(\Theta) \quad (1)$$

In class AB operation, the V_{GS} voltage enters into a non-conduction zone for an angle Θ_x depending on the conduction angle α, ranged between $180°$ et $360°$ (2). The following equation (3) determines the bias voltage as function of conduction angle.

$$\Theta_x = 180 + \frac{\alpha - 180}{2} \quad (2)$$

$$V_{GS_{DC}} = \frac{V_{th} - V_{GS_{max}} \times \sin(\Theta_x)}{1 - \sin(\Theta_x)} \quad (3)$$

The pre-power amplifier has two power gain modes (Low-gain and High-gain), both depending on the conduction angle. It is optimized to obtain good linearity for maximum gain mode. Thus, the conduction angle is the best compromise between fundamental current and distortion for high-gain mode, then it is chosen an angle of $240°$. In order to obtain low-gain mode, just one changes the biasing and, as a result, the conduction angle.

The two bias voltages for the operation modes are generated by a voltage source that delivers a DC signal V_{BIAS} taking two different values, by means of a digital command signal ($0V$ or V_{CC}). A power-down mode is also available, it reduces the power consumption. The idea is to drop the biasing voltage down: for that, we use a parallel transistor switch in the output of the biasing voltage source.

The circuit diagram of the pre-power amplifier is available in figure 1. It is constituted by two symmetrical common-emitter

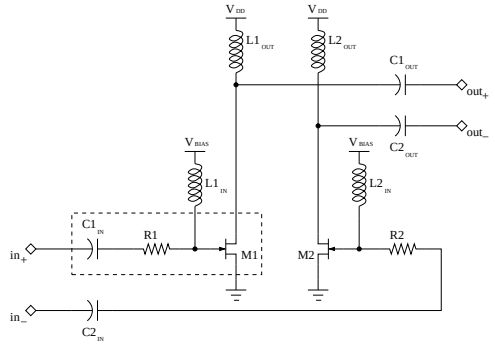

Fig. 1. Schematic of the pre-power amplifier

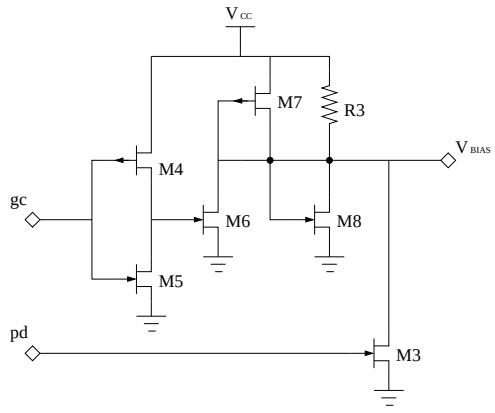

Fig. 2. Schematic of the biasing voltage generator

amplifier that form the differential pair. Transistors M1 and M2 are sized $40\mu m \times 0.2\mu m$* to provide power amplification and 11 dBm output 1dB compression point; the resistors R1 and R2 ensure stability and matching network is provided by inductors L1, L2 and capacitors C1, C2. The DC signal V_{BIAS} is generated by a voltage source with schematic available in figure 2.

The V_{BIAS} voltage is generated by transistors M6, M7, M8 and a resistor R3, controlled by a digital command signal. A digital inverter made with both transistors M4 and M5 are used to establish a convention: the High-Gain mode is selected through a high level bias (gc) and the Low-Gain mode with a low level. Although, the transistor M3 is used as a switch and controlled by the power down (pd) input, it reduces the bias voltage and the DC current consumption. The output bias voltage V_{BIAS} obtained defines the transistors M1 and M2 conduction angle as shown in figure 1.

III. Simulation results

The pre-power amplifier is designed to have a 10dB power gain in high-gain mode and a $+4,5dBm$ output power. The polarization has been chosen to obtain a conduction angle of $240°$, *i.e.* using a bias voltage of $1.66V$. The values of the inductances and the capacitances of the matching network are chosen to satisfy the power gain S_{21} value at frequency 2.45GHz. In order to obtain a $7dB$ power gain in low-gain mode, the bias voltage must be tuned to $921mV$. Both figures 3 and 4 show respectively the forward transmission and input reflexion coefficient in high gain mode.

*M1 and M2 are composed of four $10\mu m$ MOS transistors in parallel.

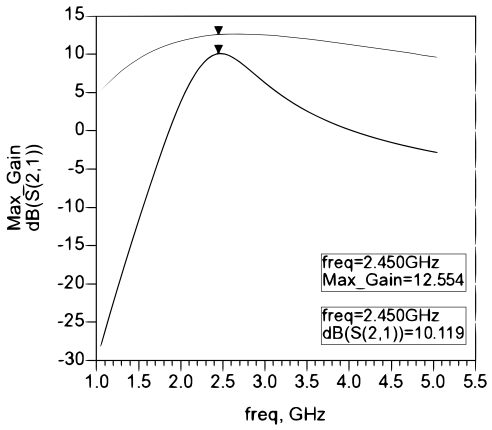

Fig. 3. Forward transmission gain S_{21} in high gain mode

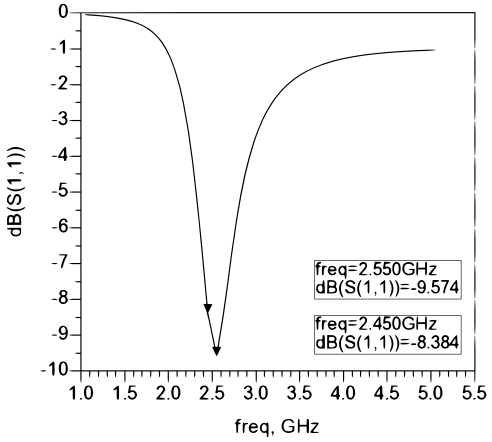

Fig. 4. Input reflexion coefficient S_{11}

The input resistors ensure the stability of the power amplifier for high gain mode.

In figure 5, one can see the amplifier compression characteristics, indicating an output $1dB$ compression point equals to $11.38dBm$. This implies that for acceptable linear operation, the maximum input power is $-5.5dBm$ for a $10dB$ power gain. The maximum power added efficiency is 33.35%, while delivering an output power of $13.16dBm$ with an input power of $7dBm$.

When the gain mode control is tuned low, the voltage source generates a bias voltage V_{BIAS} lower and the forward transmission gain S_{21} falls from $10.12dB$ to $7.02dB$ as shown in figure 6.

The power down input control allows a total power reduction in order to reduce the power driven from the supply. The table I summarizes the power down control

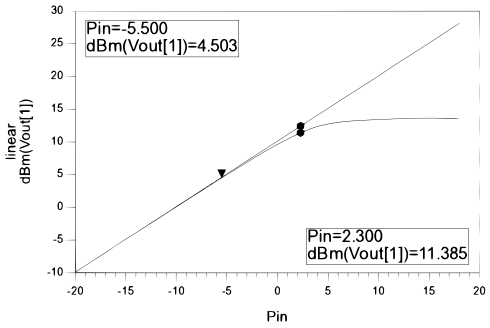

Fig. 5. Power gain versus input power in high gain mode

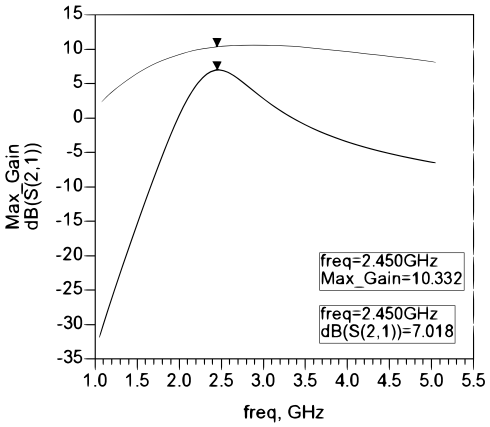

Fig. 6. Forward transmission gain S_{21} in low gain mode

impact on DC power at high-gain mode, and shows also the output power when the input power is $-5.5dBm$. As a summary, all characteristics of the amplifier at 2.45GHz are available in table II.

TABLE I
POWER DOWN CONTROL IMPACT ON DC POWER

Power down	P_{DC}	Output power
0	$55mW$	$4.5dBm$
1	$20mW$	$-10.5dBm$

IV. LAYOUT

The proposed pre-power amplifier has been designed in XFAB $0.18\mu m$ CMOS technology [10], the layout of the pre-power amplifier is shown in figure 7. Four on-chip inductors are used for biasing and impedance matching. They are disposed in the four corners of the layout, surrounding the circuit. Seven pads are used as interface for the circuit. Each connection in the circuit will be assured by wire bonding on those pads.

The entire circuit occupies an area of $1.024mm \times 0.914mm = 0.93mm^2$. The amplification is made on each part by four $10\mu m$ MOS transistors in parallel, as shown in figure 8†.

†Figure 8 represents the dashed part in figure 1, composed by capacitance $C1_{IN}$, resistance R1 and transistor M1.

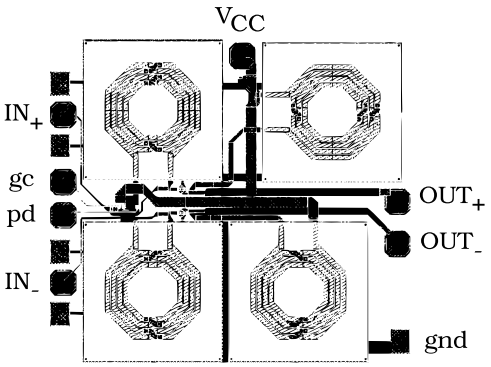

Fig. 7. Layout PPA

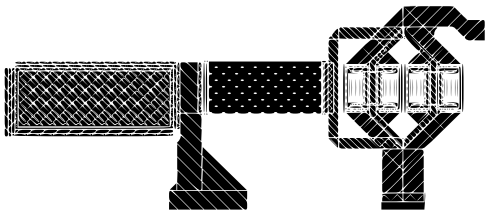

Fig. 8. Detailed transistor layout

TABLE II
SIMULATION RESULTS, SUMMARY

	Value	Unit
Power gain (HG mode)	10.12	dB
Power gain (LG mode)	7.02	dB
Output power	4.5	dBm
Output 1dB compression point	11.38	dBm
PAE_{max}	33.35	%
Stability factor	2.52	

V. CONCLUSION

A 2.45 GHz class AB single-stage differential $0.18\mu m$ pre-power amplifier has been presented in this paper. The simulation results show that under a DC voltage supply of 1.8V, the proposed PPA achieves 33.35 % power added efficiency, an output power of $11.385dBm$ at 1dB compression point, and a DC dissipation power of $55mW$. The layout size is $0.93mm^2$. Four on-chip spiral inductors are used for fully integrated biasing and impedance matching.

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