Full Adder Cells Evaluation for Subthreshold Operation on 32nm CMOS Technology

Augusto Neutzling

PPGC – Universidade Federal do Rio Grande do Sul – UFRGS

ansilva@inf.ufrgs.br

Cristina Meinhardt, Paulo F. Butzen

Centro de Ciências Computacionais – Universidade Federal do Rio Grande – FURG

{cristinameinhardt, paulobutzen}@furg.br

ABSTRACT

The migration towards deep submicron technologies has drastically changed the face of low-power design. Leakage currents turn the static power an important part in the total system power consumption. Subthreshold operation is proposed to reduce static and dynamic power consumption. This paper focus on performance and power consumption characteristics of different full adders (FA) cells designed to work at subthreshold voltages. The selected cells are the most widespread according to literature: CMOS, CPL, Hybrid, TFA, TGA and 14T. A 32nm predictive CMOS technology was used to describe the circuits. Electrical simulations were performed and the delay, dynamic and static power were measured. Results show that the TFA and TGA have better values for dynamic power consumption and delay, following for CMOS. It also show a trade-off among power and delay, when the circuits work on a subthreshold voltage operation. When the circuit will be a long time in standby mode, i.e., a long time of static consumption, the CMOS cell presents better results in subthreshold operation, and the TFA at nominal voltage.

Categories and Subject Descriptors

B.2.1 [**Arithmetic and Logic Structures**]: Design Styles - *Calculator*

General Terms

Measurement, Performance, Design

Keywords

Full Adders, Architectures, Power, Delay, 32nm, Low Power, Subthreshold

1. INTRODUCTION

As Moore Law predict, technology scaling make possible to integrate a higher number of devices in the same chip area. The scaling also improves the performance of the devices. The system frequency has become so high that it is enough for most applications. The high frequency and the large number of transistors, turn the power consumption an important design constraint, mainly in portable devices. For this kind of applications, technology scaling has directly impacted the power and energy constrains. For example, batteries capacity has not evolved in the same velocity, compromising the autonomy of new products that make use of them. Either the decrease of the power consumption has not evolved in the same way, making this restriction one of major challenges of the new technologies. By the growing number of portable devices, this challenge becomes even more important [1][2][3].

One of the more efficient approaches to reduce the power consumption is design the digital circuits with transistors operated in subthreshold region (supply voltage V_{dd} less than the threshold voltage V_{th} of the transistor) or near-threshold (V_{dd} close to V_{th}) [18]. In subthreshold designs, the subthreshold current is used for necessary computation, providing a near ideal voltage transfer characteristics of the logic gates. Its impact on system design is an exponential reduction of power at the cost of performance degradation [18].

One of the most important parts of any electronic system is the arithmetic logic unit (ALU). ALUs are responsible for performing arithmetic operations on data and addresses, making logical decisions, such as deflects and procedures calls [4]. Adders are the basic block in arithmetic units [5]. Adders cells also are the base of many others operations like as subtraction, multiplication and division. When considered how many times a system executes the sum operation, it highlights that optimization of their speed and power consumption can have considerable impact on power efficiency and speed of the overall system.

Several transistors topologies were proposed to implement adder cell. Some of the classical designs of full adder circuits use standard static CMOS and complementary pass-transistor logic (CPL) circuits [14]. There are some new designs and optimizations on full adder cells for nanometer technologies [2-7], as well as numerous works evaluating these adders [8-13]. Although the migration towards nanometer technologies has drastically changed the face of low-power design, turning static power an important part in the total power consumption, almost all the previous works brings only an evaluation of dynamic power and delay.

Hence, this paper focus on evaluating the performance, static and dynamic power consumption of different adders cells designed to work at subthreshold voltages. The circuits evaluated in this work are CMOS, CPL, Hybrid, TFA, TGA and 14T. They appear in the majority of articles reported in the literature and are illustrated in Fig. 1. The main objective of this work is to establish a comparison between those six adders circuits designed in a nanometer technology.

Next Section introduces the main concepts about power consumption in digital CMOS. Section 3 presents a general summary about the six evaluated full adder cells. Section 4 describes the used methodology. Section 5 shows the results and analysis. Finally, conclusions are discussed on Section 6.

2. POWER CONSUMPTION IN DIGITAL CMOS

The power dissipation in digital CMOS circuits can be decomposed in two parts, which are summarized in the following equation:

$$P_{total} = P_{dynamic} + P_{static} \quad (1)$$

The first term represents the dynamic component of total power. This portion is also composed by two parts as presented in equation (2).

$$P_{dynamic} = P_{switching} + P_{short\text{-}circuit} \quad (2)$$

The switching power $P_{switching}$ is due to the charge and discharge of the capacitors driven by the circuit. It is modeled by the following equation

$$P_{switching} = ½.C_L.V_{DD}^2.f.\alpha \quad (3)$$

where C_L is the output load of the gate, V_{DD} is the supply voltage, f is the clock frequency and α is the switching activity of the gate, defined as the probability of the gate output to make a logic transition during one clock cycle.

The short-circuit power $P_{short\text{-}circuit}$ is caused by the short circuit currents that arise when pairs of PMOS/NMOS transistors are conducting simultaneously in a CMOS gate [15].

The second term in equation (1) represents the static power component of total power. It is also called leakage power. It is due to the leakage current that flows in the circuit such as subthreshold, gate tunneling or reverse-biased PN junction leakages [16].

For older technologies (0.25µm and above), $P_{switching}$ was predominant and the static current could be ignored. For nanometer processes, P_{static} becomes more important and should be considered in the total power dissipation analysis [17].

3. FULL ADDER TOPOLOGIES

There are many ways to implement the sum function. It can be generated by the simplification of the function itself or by different ways to implement each logic gate. After a review of several articles that evaluate adders cells [2-13], six circuits were chosen to be explored in this work, which are shown in Fig. 1: C-CMOS (a), CPL (b), Hybrid (c), TFA (d), TGA (e) and 14T (f). This chapter presents a brief description of these adders.

The CMOS full adder cell is the standard adder circuit. It is based in the CMOS logic family which has complementary pull-up and pull-down transistor networks. It main characteristic is a high driven capacity [6][11][13]. The Complementary Pass-transistor Logic adder, CPL, is another well known circuit. It uses the concept of pass transistors. It provides the output and its complement, high performance, strong output signals and a good driven capacity [4][5][14]. Hybrid cell is known as a mix of previous two cells. Its original purpose claims to optimize performance and power consumption. The circuit works well in low voltages, because it has a strong output signal [7][9].

Transmission Gate Full Adder, TGA, is based on the transmission gates theory, which consists of a PMOS and a NMOS transistors connected in parallel, being a special type of pass transistor. Considering low power consumption, TGA presents good response at low voltage [7][10]. The Transistor Function Full Adder, TFA, is also based in the transmission function theory. It uses pull-up and pull-down paths to make the inverters, and utilizes transmission gates for the rest of the logic obtaining efficient implementations for the XORs and NORs [6][7][20]. The main disadvantage of the TFA and the TGA is the lack of the driven capacity, suffering more signal degradation when cascaded [7][10].

The 14T adder has the advantage of use a small area. 14T circuit uses the function XOR combined with the transmission gate function and, as the TFA, implements a complementary pass transistor logic to load the output [7][21].

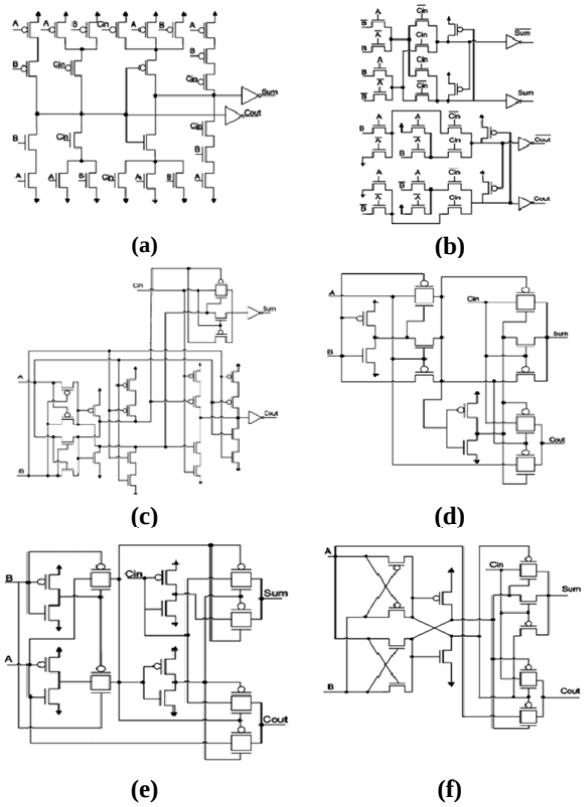

Figure 1 – Full-adder cells of different topologies [11]

(a) CMOS, (b) CPL, (c) Hybrid, (d) TFA, (e)TGA, (f)14T.

4. METHODOLOGY OF EVALUATION

To allow a complete comparison between the different adder circuits, the delay, dynamic and static power of all six cells were simulated. A low power 32nm CMOS predictive technology model was used to describe the circuits and the electrical simulations were performed in NGSPICE [22]. This technology has nominal voltage of 1 V. The transistor threshold voltage has been measure as 615 mV. The transistor sizing used was the same suggested in [9] which is also utilized in [6-8], and the frequency of operation was defined as 10 Mhz. It is the limit frequency when the circuits are operation at subthreshold voltage of 0.5V. Two different supply voltages were selected to evaluate the full adders: the nominal voltage (1V) and a subthreshold voltage of 0.5V. Buffers were used in the input and the output, to simulate real operation conditions.

The power of each transition was obtained by the equation (4), and the dynamic power was calculated from the average between the values from 24 possible arches. The delay is also an average between the 24 propagation delays. Between the sum bit delay and the carry bit delay, prevailed always the biggest (worst delay). The PDP is the product of the dynamic power by the delay, and was calculated from the results of these two parameters.

$$P_{avg} = \frac{1}{t}\int_0^t I(t)\cdot V\cdot dt \quad (4)$$

The evaluation the static power in nominal and subthreshold operation is a main contribution of this work. To calculate the static power, the 8 logical possible combinations were simulated in each adder circuit. The presented static power is the average result of all 8 simulations.

5. RESULTS OF EXPERIMENTS

Table 1 presents the delay, dynamic and static power values obtained through simulations of the six full adders in nominal and subthreshold operation. Firstly, it is important to observe that 14T adder was simulated at different subthreshold voltages and does not work correctly on any of them. The graphs of Figures 2-5 show the normalized results of the dynamic power, delay, PDP and static power, respectively.

From the dynamic power results is observed that the CPL adder has the highest power consumption. The main reason for this behavior is the fact that CPL switching has to generate transitions for the direct and complementary outputs. Following, the 14T and the Hybrid cells consume more power than the CMOS. TFA and TGA adders present low power consumption for the nominal voltage. It is important to note that at the subthreshold voltage (50% of nominal voltage), all circuits consume up to 25% of the power consumption at nominal voltages. This behavior reflects the dynamic power consumption quadratic voltage dependence.

In relation to the delay, the 14T present the worst results. Among the others, the CPL presented the higher values, followed by the Hybrid. The CMOS has an intermediate delay and the TFA and the TGA have the lowest delay. The results show that at subthreshold voltage, the absolute delay suffers huge penalties but the behavior described to nominal supply is maintained.

The degradation on delay at subthreshold is observed in the results. This also impacts PDP, lead to worse values than at nominal voltage. Analyzing the architectures was observed that the CPL presents the worst PDP value, followed by the Hybrid. CMOS presented a better result, which represents a better tradeoff between dynamic power and delay. The TFA and the TGA presented the best PDP values.

The analysis of the static power consumption shows that, as expected, at the subthreshold voltage the results are always lower than at the nominal voltage. But the ratio between the two different supply voltages varies for each approach. At nominal voltage, the 14T shows high static power consumption. The main reason for it is the fact that, for the input Cin=1, A=0 and B=0, the static consumption is a hundred times greater than in the other cases, which leads the average up.The CPL also consumes more than the others. TFA has the lowest values. At subthreshold operation, CMOS reduces static power more than the others, and presents the lowest consumption, followed by the TFA. The CPL consumes more than the TGA and less than the Hybrid.

The data analyses allow identifying which adders are more suitable for a particular purpose, when designing an integrated circuit in 32nm technology, and observe how each of those adder cells works on a subthreshold supply voltage.

At nominal voltage, if the main design objective is to reduce power consumption in a circuit that uses adders several times, the main constrain is the dynamic power, and the TFA, TGA and CMOS are the most suitable. If delay is a critical design constrain, TFA and TGA are also the good choices. And if the adder circuit will be a long time on standby, the static power becomes a serious restriction in nanometer technologies, the TFA are the most suitable. The Hybrid is the intermediate choice for this technology, for any objective.

On subthreshold the dynamic power can be economized about 80% with a 50% voltage reduction. At this voltage, the delay increases about 160 times. In this case the static power consumption reduces between 14% and 38% depending of the adder cell. On subthreshold,operation, CPL has the highest proportional savings and the CMOS has the lowest absolute value of static power consumption.

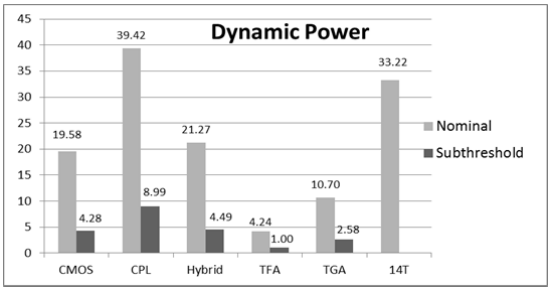

Figure 2 – Normalized Dynamic Power Results.

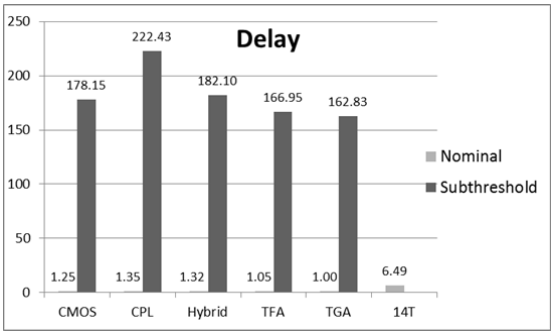

Figure 3 – Normalized Delay Results.

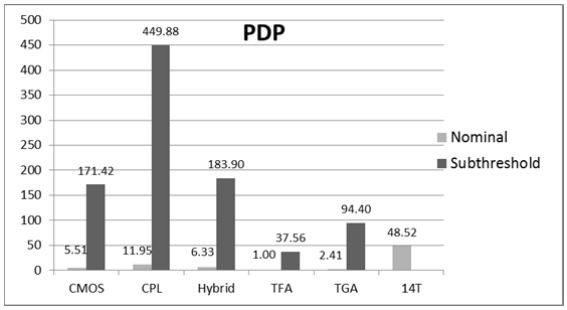

Figure 4 - Normalized PDP Results.

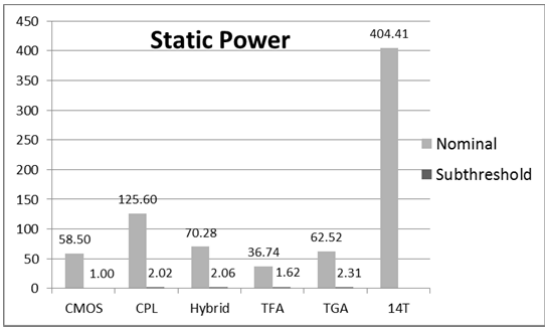

Figure 5 - Normalized Static Power Results.

Table 1 - Simulation results of dynamic and static power, delay and PDP, for each cell.

	CMOS		CPL		Hybrid		TFA		TGA		14T	
	nominal	subthreshold	nominal	subthreshold	nominal	subthreshold	nominal	subthreshold	nominal	subthreshold	nominal	subthreshold
Dinamic Power (μW)	1.80	0.39	3.62	0.83	1.95	0.41	0.39	0.09	0.98	0.23	3.05	-
Delay (nS)	0.11	16.10	0.12	20.11	0.12	16.46	0.09	15.09	0.09	14.72	0.59	-
PDP (fJ)	0.20	6.32	0.44	16.59	0.23	6.78	0.04	1.39	0.09	3.48	1.80	-
Static Power(pW)	233	3.98	500	8.05	280	8.22	146	6.46	249	9.21	1611	-

6. CONCLUSIONS

An evaluating of different full adder topologies was performed to allow identifying which adders are more suitable for a particular purpose. The goals were compare the cells analyzing dynamic power, delay and highlight the static power consumption, which the importance has increased at submicron technologies. It was used a 32nm technology designing an integrated circuit, and observed how each of those adder cells works in nominal voltage and with transistors operated in subthreshold region. The results showed that the TFA and TGA is most suitable choices, and CMOS is a good option, if the adder circuit will use subthreshold voltage and will be a long time on standby. For all topologies, adopting subthreshold operation as low power technique can represent a high economy of dynamic and static power consumption, with a quite significant degradation on delay.

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