Project of DMT modulator in Multicore DSP with FFT Coprocessor

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ABSTRACT
This work discusses the characteristics of a multicore processor to perform DMT/OFDM modulation, while eventually executing other concurrent tasks. The DMT modulation is of special interest because it has been adopted in several communication systems. As a case study, the TMS320C6670 is adopted, which has a (I)FFT coprocessor. The use of these coprocessors can be essential to make a DMT/OFDM feasible given that the majority of the computation cost for transmission/reception corresponds to the (I)DFT algorithm. The obtained results indicate that DSP chips with (I)FFT coprocessor are competitive with alternatives such as FPGA, with respect to cost and performance.

General Terms
DMT / OFDM Modulation, DSP Multicore

Keywords
FFT, FPGA, Modulation, Telecommunications

1. INTRODUCTION
The increase in computing power and benefits of this development is noted over the years. One important area that has been evolving in this direction are Multicores DSP (Digital Signal Processor). With a constantly growing demand for computing performance, these chips have applicability in many areas that rely on real-time processors for high performance - highlighting the signal processing in the area of telecommunications.

As shown in [9] the content of the communications network has great influence on the development of the architecture of DSP chips. With the introduction of high definition video, voice processing, among other uses networks have led to demands for data traffic have been growing and using more than one DSP core becomes a viable solution within this context.

Professinonals from academia and industry have interest in platforms for implementation of algorithms for telecommunications and digital signal processing in general. To do this, apart from DSPs, the FPGAs (field-programmable gate array) is other option. Thus the comparative results between these platforms in each area of use have great value as see in [8].

Within the field of telecommunications, the transmission of modulated signals and the ability to process the demodulated received signal has a great influence on the efficiency of a communication system. A type of modulation commonly used is the DMT (Discrete Multi-Tone), which has gained much attention in fields such as communication in wireless networks, because of the efficiency of this technique in the use of available bandwidth. [6]

In [5] the use of GPUs (graphics processing units) applied to accelerate simulations of OFDM (Orthogonal frequency-division multiplexing) in PLC (Power Line Communication). DMT and OFDM are similar, the basic difference is the band where each one operates.

In [2] is discussed aspects of the implementation of a prototype modem based on OFDM physical layer of IEEE 802.11 in a Xilinx FPGA. The use of OFDM in wireless networks is vast, as shown in [2], the 802.11 family of standards use this modulation technique based on.

In this context, this paper presents the design and the intial implementation results of a DMT modulator in a multicore DSP using FFT (Fast Fourier Transform) coprocessors, and a comparison between FFT implementations in FPGAs and DSPs . This becomes possible to build a high performance modulator, capable of communication with higher rates, taking advantage of the processing power that multicore DSP chip offers and especially the ability of the FFT coprocessors.

This paper is structured as follows: Section 2 presents the main features of a multicore DSP, Section 3 presents the DMT modulation technique, Section 4 highlights the design

features of a DMT modulator in a multicore DSP; Section 5 presents the overall result obtained; Section 6 presents the conclusions and future work.

2. PLATAFORMS MULTICORE DSP

The multicore DSPs are classified according to some relevant features as: architecture, type of interconnection and organization of memory.

As shown in [4], the state of the art, multicore DSPs are defined by the type of their cores as homogeneous or heterogeneous. In the first case a multicore DSP chip has identical cores. On the other hand, in the second case, the chip has cores of different types, for example, an arrangement of GPP (general - puporse processors) GPUs or MCUs (microcontroller units) cores.

Furthermore, multi-core DSPs are classified according to their type of interconnection. This type of classification is defined topologies into two types: hierarchical or mesh.

Multicore hierarchical topology has its data transferred between your kernels through at least one unit of exchange. Already those with mesh topology have connections with all its neighbors, facilitating the scalability in this type of interconnection. More information about interconnection topology can be seen in [4].

This work will be treated in the TMS320C6670 chip developed by Texas Instruments. This chip has four cores, characterized by the homogeneous architecture and has hierarchical interconnection. [3]

3. DMT MODULATION

The DMT modulation is often used in data transmission because the modulator may be configured such that the transmission is optimized according to the channel information.

The DMT modulation discretized signal in the frequency band and divides into several smaller, through DFT (Discrete Fourier Transform) and IDFT (Inverse Fourier Transform Dicrete Time), so that several different bands can transmit data at different rates.

The idea of multitone modulation is focused on a principle commonly used in engineering: divide and conquer. According to this principle, a problem is solved by dividing the same into various problems simpler and thus combining the solutions obtained. In our context, the problem is the transmission of data over a broadband channel. Broadband is partitioned into several smaller bands, where in each of one the QAM modulation is used, and the number of QAM constellation points depends on the noise in that band.

The Figure 1 shows the DMT technology. The *FEQ* block is the equalization in frequency (Frequency Domain Equalizer) that for each carrier, offsetting the effect of the channel *H[k]*. One of the FEQ algorithms has the function of estimate H[k] and multiply each symbol Y_k for $Z[k] = \frac{1}{H[k]}$.

The fundamental equation of DMT modulation is:

$$Y[k] = H[k]X[k] + N[k], \quad (1)$$

where H_k and N_k, are the channel frequency response and the noise in Kth-carrier, respectively. This equation is valid only when the channel is partitioned, for more details see [7].

The TEQ block is used when the impulse response of channel is very long. The TEQ allows to the system use a cyclic prefix lower.

The signal *x(n)* can be obtained using the inverse DFT, as shown in Figure1. Before the samples in the time domain are sent to the channel h(n), the DMT modulation copies *L* sampels of the end of signal *x(n)* to the top of the same signal. The samples so-called cyclic prefix (CP), as shown in Figure 2 where L equals 20. This redundancy is utilized to minimize the intersymbol interference produced by the channel.

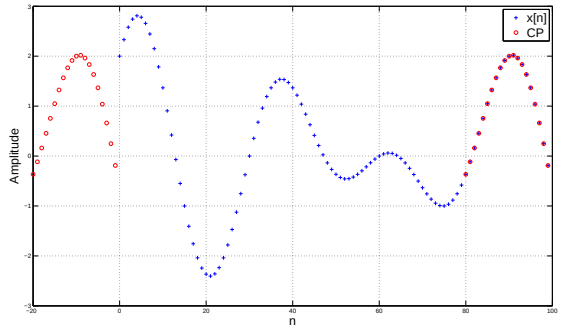

Figure 2: Representation of cyclic prefix.

In the Demodulation, the cyclic prefix is removed and the remaining samples are little affected by the intersymbol interference.

4. DMT IN MULTICORE DSP

In this section we discuss the details of a design of DMT modulation in a multicore DSP.

4.1 Design

The design of a DMT modulator in a multicore DSP has as its main task the best use of resources of parallelism that this environment offers, in addition to the hardware implementation of the FFT processing. Therefore, the Figure 3 shows the flowchart of the implementation of this modulator in TMS320C6670 DSP chip that has four cores.

As shown in the flowchart, this project consists of building blocks of the modulator and implementation of DMT each. As the blocks conversion of the serial input to parallel, QAM mapping and passing data to FFT coprocessor are less costly in terms of processing. The project has been determined that they will run on a single core. Thus leaves to others the task of input and output data, since in a communication system for high performance flow rate of the data tends to be high in need of a good computational resource.

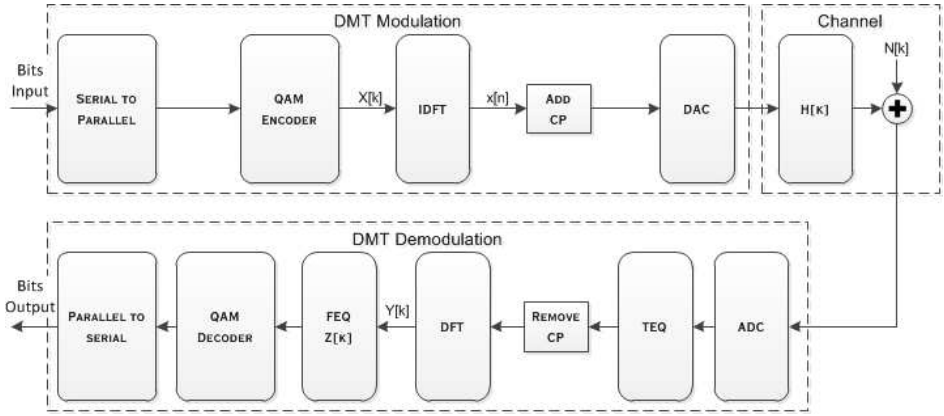

Figure 1: Representation of blocks of a system for DMT Modulation and Demodulation.

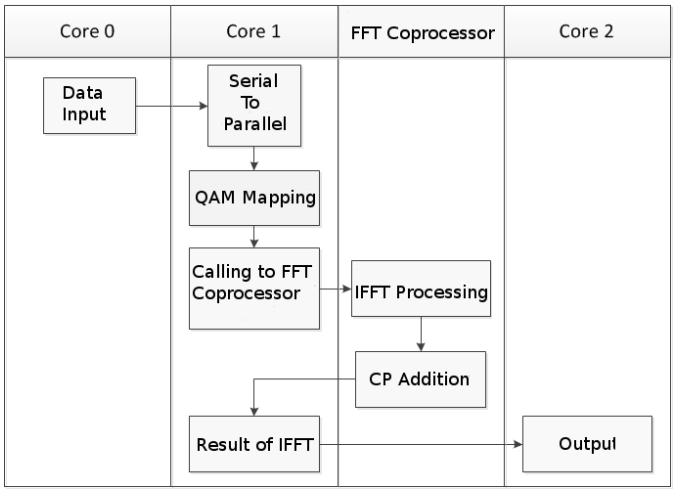

Figure 3: Flowchart of DMT modulation in multi-core DSP environment.

It is worth noting that the IFFT processing is not executed by the DSP cores, but by an FFT coprocessor present in the chip. Thus the block IFFT processing is executed in the coprocessor, increasing system performance DMT since this tends to be most of the processing.

This coprocessor IFFT also is capable of adding the cyclic prefix. So this task will be executed within this coprocessor, which passes as a result the output of the IFFT with the prefix cíclio added.

5. RESULTS

Since the FFT coprocessors perform the most expensive computational part of this project, this Section presents the results of these coprocessors compared with other implementation of FFT. The results of the implementation of DMT modulator in DSP are presented in this Section too. Lastly, it is analyzed the results of TMS320C6670 chip in comparison with results of FFT Mega Core Function, which is an IP Core for FPGA from Altera

So is analised the results of TMS320C6670 chip in comparation of results of *FFT Mega Core Function*, what is an IP Core for FPGA belonging to Altera.

The table shows the comparison between FFT implementations in FPGA and DSP. To compare the implementation of this FFT chip TMS320C6670 with the implementation of the FFT Mega Core Function in two possible families of FPGA, the Stratix IV (the family that has more computing power able to implement this IP Core) and Cyclone III (the family that has less computing power to implement the same IP Core). For mor details see in [1].

As shown in table 1, the FFT coprocessor of TMS320C6670 has an efficiency similar to the FPGA implementation of the FFT Stratix family IV with two clear advantages in relation to this FPGA:

- It is possible to process FFT blocks of 8192 points.
- It is cheaper than the FPGA.

It has also been implemented in DSP the QAM mapping blocks and serial to parallel allowing the implementation of a modulator DMT simple. Table 2 shows the number of clock cycles required for the execution of each block in a DMT modulation with the number of points in the FFT.

Table 2: Number of clocks cycles for each block implemented

	32 points	64 points	128 points
serial to parallel	2.664	5.528	10.937
QAM mappping	2.647	5.329	10.636
Total	5.311	10.857	21.576

6. CONCLUSIONS AND FUTURE WORKS

When analyzing the results developed in this work, it is possible to notice the feasibility of implementing a DMT systems of high rates in chip TMS320C6670 from Texas Instruments, mainly taking advantage of the computing power of the FFT coprocessor present this chip. As shown in table I, it has a capacity similar to the FFT implementation in Stratix IV FPGA family from Altera with much lower cost and processing blocks larger than the chips of this family.

Table 1: Comparative table of FFT implementation in FPGA and DSP

	TMS320C6670	Stratix IV	Cyclone III
lenght of FFT (points)	8192	4096	4096
Time for FFT of 2048 points (μs)	4,8	4,68	8,36
Number of cores FFT in parallel	3	4	4
Price (U$$)	330	1400	50

This work also get as important result, the discussion about aspects the implementation of digital signal processing in modern multi-core DSP platforms, with emphasis on the use of FFT coprocessor. The tendency to use such chips is promoted by increasing the sampling rate in applications such as wireless telephony, which require the calculation of FFTs with large numbers of points in a short time.

As future work, we intend to develop a complete DMT system involving Modulators and Demodulators. In addition, this can be used in Texas Instruments multicore chip to get results for this implementation, enabling the system to check potential bottlenecks.

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