A Systematic Methodology for Analog Design of Operational Amplifiers Composed by Nanodevices

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ABSTRACT

A systematic analog design methodology for integrated operational amplifiers composed by nano-devices such as FinFETs and CNTFETs is presented in this paper. The methodology includes the sizing of gate width and length of transistors and is based on the gm/I_D x I_N and Early voltage x L characteristic curves. The main advantage over the traditional analog design methodology is the independence on device equations. It is fundamental for nano-devices design, since the very complex electrical models do not provide intuitive relations between design specifications and device electrical parameters. As an example, the proposed methodology is applied for the design of a differential amplifier in 32nm technology node.

1. INTRODUCTION

With the evolution of the integrated circuits (ICs), there is a need to reduce the dimensions of the transistors to accommodate the growing demand for devices with higher speed and lower power consumption. Nowadays, silicon planar technology is dominant in the market, but some of its parameters, such as the typical thickness of gate oxide layer (T_{ox}), are in the order of magnitude of a few nanometers, near the physical limit [8]. Therefore, there is a need to explore new materials and fabrication methodologies for the development of new devices and keeping the evolution of ICs according to the Moore's Law. Two candidates are the fin field-effect transistors (FinFETs) and the carbon nanotube field-effect transistors (CNTFETs), which present similar electrical characteristics than the silicon metal-oxide-semiconductor field-effect transistors (MOSFETs).

Design methodologies must evolute in compass with the fabrication process technology. Typically, the analog integrated circuit design is basically manual, based on the experience of the human designer. The verification depends on the electrical simulator. In a general way, the initial values of a design are estimated using simplified equations of the device, which are simple to work. These equations give a direct but imprecise relationship between drain current, terminal voltages, and small signal characteristics. The refinement of the design is based on interactive electrical simulations and empirical perturbation of design parameters.

Electrical models for the new technologies do not provide a simple relationship between current and voltage, making traditional methods used for planar technology inadequate for the design using these devices. Therefore, this work proposes a design methodology suitable for the sizing of analog blocks using FinFETs and CNTFETs. The design methodology is based on the rearranging of design equations in function of gate transconductance over drain current (gm/I_D) and Early voltage (VA). There are two positive aspects of the methodology: it takes into consideration all regions of operation of the device and it provides a systematic way to size the circuit without handling complex device model equations.

2. ELECTRICAL MODELS

Some electric models for the MOS transistor in planar technology are very simplified, allowing the relation between drain current and terminal voltages to be explicit in a single equation. As an example, Spice Level 1 is based on a simplified equation for the transistor drain current, as the following for linear region [1]:

$$I_D = \frac{\mu_0 C_{ox} W}{L}\left[(V_{GS} - V_T) - \frac{V_{DS}}{2}\right] V_{DS} \qquad (1)$$

However, it is not accurate and can not be applied for submicrometer devices due to the growing relevance of second order effects. A more accurate electrical model is BSIM3, which was introduced in 1994. It is widely adopted by the industry today and provides good performance when applied to analog circuit simulation [2]. For modeling new devices, macro blocks can be formulated using basic MOS models. An electrical model used for modeling the FinFET technology is the BSIMSOI model, an international standard model for SOI (Silicon-On-Insulator) circuit design [9]. This model is formulated on top of the BSIM3v3 framework. It shares the same basic equations with the bulk model so that the physical nature and smoothness of BSIM3v3 are retained.

BSIMPD [11] is the Partial-Depletion (PD) mode of BSIMSOI and includes many enhanced features. The body potential is determined by the balance of all the body current components. It provides an improved impact-ionization current model, gate-to-body tunneling current model and en-

hancements in the threshold voltage and bulk charge formulation of the high positive body bias regime [5]. Instance parameters (*Pdbcp*, *Psbcp*, *Agbcp*, *Aebcp*, *Nbc*) are provided to model the parasitics of devices with various body-contact and isolation structures [10]. An external body node (the 6th node) and other improvements are introduced to facilitate the modeling of distributed body-resistance.

The electrical model that models the CNTFET technology is the model created by the Department of Electrical Engineering at Stanford University [4]. The model includes quantum confinement on both the circumferential and the axial directions, the acoustical/optical phonon scattering in the channel region and the screening effect by the parallel CNTs for CNTFET with multiple CNTs. In this model, the nanotubes are placed in two groups: the two CNTs at two ends (with only one neighboring nanotube) and the other $n-2$ CNTs in between (each with two neighbors to the sides). This model accounts for charge screening effects on drive current and device performance. The model was designed to be used in unipolar devices. The screening effect by the parallel channels is also incorporated in to the device model [6].

The three technologies discussed in this paper have electrical characteristics in common, but with different behaviors. This fact can be analyzed through the curves that represent the characteristics of the parameters gm/I_D and VA of the technologies. Fig. 1 shows gm/I_D x I_N (normalized drain current), VA x L, VA x V_{GS} and VA x V_{DS} for planar, FinFET and CNTFET technologies. These curves were obtained by electrical simulation of an n-type transistor using Spice for 32nm predictive parameters.

For design purposes, free design parameters of a CMOS transistor are the channel width (W) and length (L). For the design of analog circuits with FinFET technology, the designer has the freedom to vary the dimensions L and the number of *fins* in parallel for emulating a larger W. For the CNTFET technology the free design parameter is the length of the channel. The transistor width is fixed, given by the diameter of the nanotube. For larger widths, it is necessary to use a parallel association.

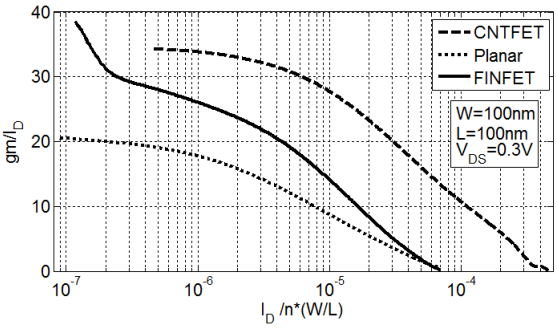
3. PROPOSED METHODOLOGY

The methodology proposed in this paper is based basically on the gm/I_D methodology [7], which is a design technique that considers the relationship between the ratio of the transconductance gm over DC drain current I_D and the normalized drain current $I_N = \frac{I_D}{(W/L)}$ as a fundamental design tool. Some adjustments were made in the gm/I_D methodology for the design flow, including steps that enable the design of gate width and length.

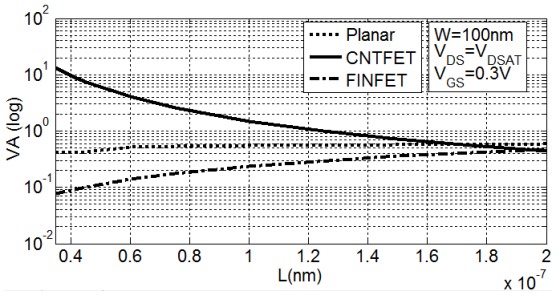
The gm/I_D curve can be observed as the derivative of the logarithmic of I_D with respect to V_{GS}, as shown below:

$$\frac{gm}{I_D} = \frac{1}{I_D} \cdot \frac{\partial I_D}{\partial V_{GS}} = \frac{\partial (ln(I_D))}{\partial V_{GS}} \qquad (2)$$

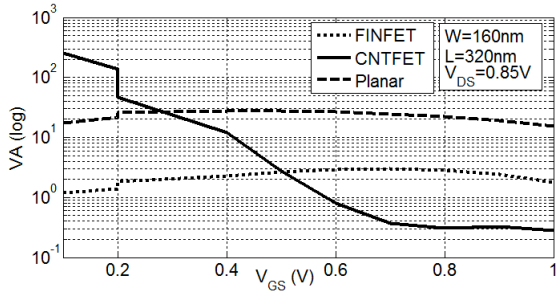
The strategy used in this work is to complement the gm/I_D methodology including the design stage of the channel length by means of the Early voltage and L relationship. Early voltage is a parameter directly dependent on the channel



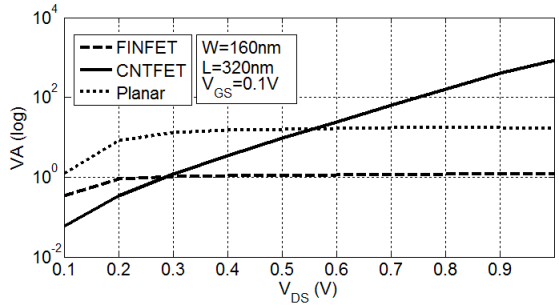
(a) gm/I_D x I_N



(b) VA x L



(c) VA x V_{GS}



(d) VA x V_{DS}

Figure 1: Simulated characteristic curves for planar, FinFET and CNTFET technologies.

length of the transistor and represents the ratio between the drain current and the output conductance (gds) of the devices, as shown [3]:

$$VA = \frac{I_D}{gds} \qquad (3)$$

The complete design flow is shown in Figure 2. In general, an amplifier can be designed following up systematically the steps in this design flow. The first step is to define specifications of the circuit that are directly related to the pa-

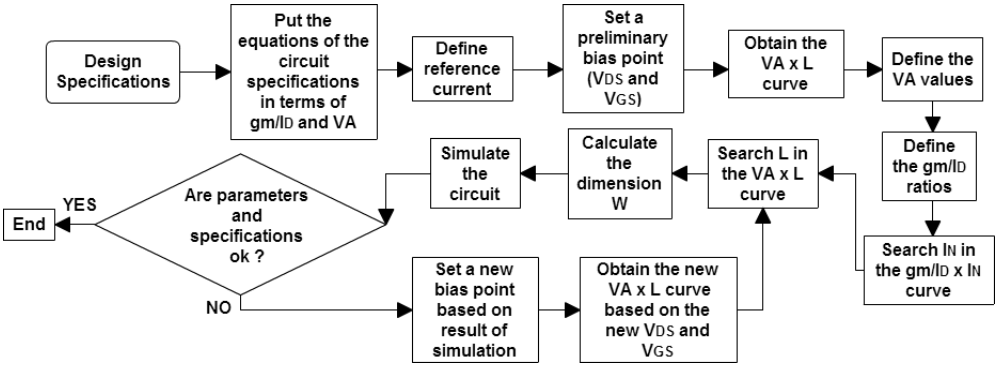


Figure 2: Design flow of the proposed methodology.

rameters gm/I_D and VA. The bias current of the circuit is scaled in order to comply with the specifications of the circuit. The estimation of a preliminary bias point of the circuit is necessary in order to provide an initial guess for the design parameters. With the preliminary values of V_{DS} and V_{GS} for each transistor it is possible to obtain the VA x L curve of each device and then choose the values of Early voltages and the values of the corresponding gate lengths that comply with the circuit specifications. The values of the gm/I_D ratios for each devices are also defined based on desired specifications. After defined the gm/I_D, ratio it is possible to find the normalized current I_N value of transistors. With this, the gate width can be calculated.

An electrical simulation of the circuit is necessary to check if the specifications and parameters are in agreement with the expected. If the specifications and circuit parameters are not in conformity with what was requested, then the procedure is repeated with a new bias point based on the result of the previous simulation. New VA x L curve based on the new V_{DS} and V_{GS} must be generated. The process of defining a new bias point, generating new curves, scaling the length and width of the transistor gate, simulating and checking is repeated until the specifications and circuit parameters are in accordance with the expected. The iteration is necessary because the Early voltage depends not only on the length of the gate device. As seen in Fig. 1, Early voltage is also directly dependent on the bias voltages V_{DS} and V_{GS} of transistor.

4. DESIGN EXAMPLE: DIFFERENTIAL AMPLIFIER

As a design example, the proposed methodology was applied to the design of a differential amplifier in order to illustrate the design on an analog block composed by nanodevices, specifically planar, FinFET and CNTFET technologies in 32nm node. The electrical schematic of a differential amplifier is shown in Figure 3. This amplifier is composed by a differential pair (M1 and M2) and a current mirror as active load (M3 and M4). For matching constraints, M1=M2 and M3=M4.

The application of the methodology for the design of the differential amplifier consists in determining the dimensions of the transistor M1 and M3. Design specifications are the following: minimum slew-rate (SR=10V/μs), maximum dissipated power (P_{max} = 1mW), minimum voltage gain (A_{V0} = 20dB) and minimum cutoff frequency (f_{-3dB}=100kHz). Environmental constraints are C_L=10pF, V_{DD}=0.45V and V_{SS}=-0.45V. Following the methodology in a systematic way, as the specifications are already defined, then the next step is to put the specifications of the circuit in terms of gm/I_D and VA. As $gds = \frac{I_D}{VA}$, so the voltage gain of a differential amplifier in terms of gm/I_D and VA is given by

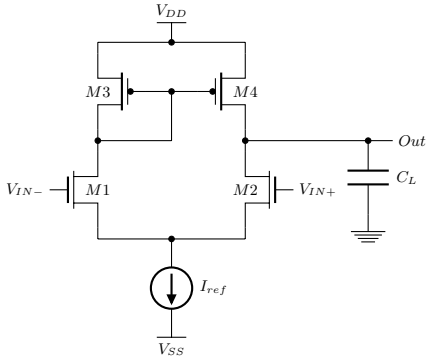


Figure 3: Schematics of a differential amplifier.

$$A_{V0} = (\frac{gm}{I_D})_1 \frac{VA_2 VA_4}{VA_2 + VA_4} \quad (4)$$

The cutoff frequency of a differential amplifier in terms of VA is given by

$$f_{-3dB} = \frac{I_D(VA_2 + VA_4)}{2\pi C_L VA_2 VA_4} \quad (5)$$

The other specifications cited are not directly related to gm/I_D and VA, but can be easily estimated. With the maximum dissipated power, the maximum current of the circuit is defined according to:

$$I_{refmax} = \frac{P_{max}}{V_{DD} - V_{SS}} \quad (6)$$

It gives a maximum reference current of $1.11mA$. The slew-rate specification determines the minimum current of the circuit:

$$I_{refmin} = SR \cdot C_L \quad (7)$$

So, the minimum current of the circuit is 100μA, which will be used for reference current of the current mirror. Now it

Table 1: Gate width and gate length for the designed transistors of the differential amplifier.

Technology	Transistor	W	L
Planar	M1, M2	6.6634μm	54nm
	M3, M4	74.183μm	90nm
FinFET	M1, M2	8·160nm=1.28μm	270nm
	M3, M4	32·160nm=5.12μm	400nm
CNTFET	M1, M2	18·3.01nm=54.18nm	180nm
	M3, M4	7·3.01nm=21.07nm	70nm

Table 2: Values of the specifications and parameters obtained after applying the proposed methodology.

Tech	A_{V0}	f_{-3dB}	VA_2	VA_4	$(\frac{gm}{I_D})_1$	P_{diss}	SR
Planar	20.42dB	1.38MHz	1.450	0.918	19.8	90μW	22.33V/μs
FinFET	23.43dB	0.84MHz	1.380	2.350	16.29	90μW	10.25V/μs
CNTFET	22.87dB	0.60MHz	2.548	2.565	11.06	90μW	9.99V/μs

is possible to estimate the drain current passing through the transistors, which is half I_{ref}.

The preliminary bias point was estimated as $V_{DS} = V_{DSAT}$ for planar technology and V_{DS}=0.25V for FinFET and CNTFET technologies. For the three technologies the V_{GS} voltage was estimated in 0.3V. With the VA x L curves generated for each technology it is possible to set the values of the parameters for VA_2, VA_4 and the gm_1/I_D ratio with its corresponding value of I_N.

After some iterations, a convergence was obtained for all technologies. The final transistors sizes for planar, FinFET and CNTFET technologies are shown in Table 1. For the CNTFET version, the width is determined by the number of unit nanotubes in parallel (n) multiplied by the nanotube diameter (which is equal to 3.012nm). The same occurs for the FinFET version, in which the unit channel width is 160nm. The final results of the specifications and circuit parameters obtained after applying the proposed methodology for the three versions are shown in Table 2.

It can be noticed that the voltage gain of planar technology achieved the smallest value between the three technologies. However, the cutoff frequency was higher. The values obtained for the Early voltages were very close to the specified values. The FinFET technology achieved the highest voltage gain and the cutoff frequency was higher than the CNTFET technology, but smaller than the planar technology. The CNTFET version presented a voltage gain higher than the planar but smaller than FinFET. The cutoff frequency was the largest among the three technologies. With respect to energy consumption of the circuit, the three technologies presented the same power dissipation, since the reference current was the same for the three designs.

5. CONCLUSION

The proposed methodology, based on gm/I_D x I_N and VA x L curves, provides a systematic design procedure for analog integrated blocks. The technique demonstrate robustness and is valid for the design of analog blocks composed by nanometer-scale devices. The design of a differential amplifier in planar, FinFET and CNTFET technologies presented adequate results, according to design specifications. The voltage gain of the differential amplifier was very close to the value specified for the three technologies, while maintaining the same dissipated power. The methodology showed to be very simple for designing analog block, since it does not take into account the hand calculations with complex equations that model the devices. For future work we intend to automate the methodology and apply it for other operational amplifiers.

6. ACKNOWLEDGMENTS

The grant provided by Fapergs, CNPq and CAPES Brazilian research agencies are gratefully acknowledged.

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