Correction of the errors due to the non zero drain-to-source voltage in the g_m/I_D based V_{th} extraction methods

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***Abstract*—In this paper we study the drain voltage effect on the threshold voltage extracted using the transconductance to current ratio (g_m/I_D) and the g_m/I_D change ($d(g_m/I_D)/dV_G$) methods. We analyze and compare the power correction factor (PEC) of these threshold voltage extraction methods using numerical simulations of a generic long-channel MOSFET (0.35 μm CMOS process) with a parametric voltage sweep in the drain voltage in a common source configuration. The numerical simulations were carried out using MATLAB®, and the MOSFET model implemented is based on the Advanced Compact MOSFET (ACM). It is shown that the correction procedure proposed for the g_m/I_D method is more accurate than the correction procedure proposed for the $d(g_m/I_D)/dV_G$ method.**

***Keywords*— MOSFET threshold voltage extraction, transconductance change method, transconductance-to-current ratio, Advanced Compact MOSFET;**

I. INTRODUCTION

The accurate determination of the MOSFET threshold voltage V_{th} is essential for CMOS device/circuit design and modeling, particularly for advanced ultra low power devices [1,2]. V_{th} represents the change from weak inversion (WI) to strong inversion (SI), and because this is a gradual process there is no specific point that can be directly identified as the threshold voltage in the I_D vs. V_G characteristic. This fact and sometimes poor modeling have produced numerous V_{th} definitions and extraction procedures [2]. The majority of the extraction procedures determine V_{th} from the static drain current versus gate voltage (I_D–V_G) characteristic of a single transistor [3]. Most of the I_D–V_G methods use the strong inversion (SI) region or the weak inversion (WI) region in the linear or the saturation regions. These extraction methods are based in a model valid for only one region of MOSFET operation (WI or SI), and extract the V_{th} from experimental data avoiding the transition region (in between WI and SI). Thus, the extracted V_{th} is inaccurate since it lies in the transition region [2]. With the development of all region CMOS models, new definitions and extractions methods of V_{th} had been introduced [4]. In particular, charge based threshold definitions and charge based extraction methods have been introduced for the charge-based models (i.e. EKV, ACM). With these physic-based V_{th} definitions, accurate extraction techniques had been proposed. This techniques are less influenced by parasitic effects (drain or source series resistances, channel mobility degradation) and less sensitive to short channel effects (DIBL, CLM and velocity saturation)[2]. It is important to understand that, the charge-based definitions and extraction methods can be applied to all MOSFET models, including surface potential-based models.

The purpose of this paper is to study the power error correction (PEC) of the drain voltage effect (γ_D) on the V_{th} extraction methods in long channel MOSFETs, introduced in [5, 6]. These methods are based in the transconductance to current ratio (g_m/I_D) MOSFET characteristic. In section II the MOSFET model is summarized, and in section III the V_{th} definition used in the g_m/I_D extraction methods is recalled. In section IV the drain voltage effect in the extracted threshold voltage is analyzed using analytical models. In section IV the g_m/I_D V_{th} extraction methods are presented. Finally, in section V the PEC of both procedures are analyzed in a generic long-channel MOSFET (0.35 μm CMOS process) by numerical simulations using MATLAB® .

II. ACM MODEL

A. ACM model equations used

The ACM model consists of simple, accurate, and single equations that represent the device behavior in all regimes of operation [5]. The expressions of ACM model used in this work are summarized below.

$$I_d = \mu \frac{W}{L}\left[\frac{\left(Q_{IS}'^{\,2} - Q_{ID}'^{\,2}\right)}{2C_{ox}' n} - \phi_T\left(Q_{IS}' - Q_{ID}'\right)\right] \tag{1}$$

$$V_P - V_{S(D)} = \phi_t\left[\frac{Q_{IP}' - Q_{IS(D)}'}{nC_{ox}'\phi_t} + \ln\left(\frac{Q_{IS(D)}'}{Q_{IP}'}\right)\right] \tag{2}$$

$$V_P = \phi_{sa} - 2\phi_F - \phi_t\left[1 + \ln\left(\frac{n}{n-1}\right)\right] \simeq \frac{V_G - V_{th}}{n} \tag{3}$$

$$\frac{g_m}{I_d} = \left(n\phi_T - \frac{\left(Q_{IS}' + Q_{ID}'\right)}{2C_{ox}'}\right)^{-1} \tag{4}$$

$$\frac{d}{dV_g}\left(\frac{g_m}{I_d}\right) = \frac{1}{2C_{ox}'}\left(\frac{Q_{IS}'}{n\phi_t - \frac{Q_{IS}'}{C_{ox}}} + \frac{Q_{ID}'}{n\phi_t - \frac{Q_{ID}'}{C_{ox}}}\right)\left(n\phi_t - \frac{Q_{IS}' + Q_{ID}'}{2C_{ox}'}\right)^{-2} \tag{5}$$

B. *ACM model implementation*

The numerical simulations were carried out using MATLAB®, and the implemented model solves the equations (1) to (5). We used the technological parameters from a standard 0.35 µm CMOS process: acceptor doping concentration N_A= $6x10^{16}$ cm^{-3}; oxide thickness t_{ox}=7.8 nm; low field mobility μ_0 = 0.*36238 m^2/Vs ; flat band voltage V_{FB}=0.8 V. A long channel NMOS transistor (W/L=32µm/3.2µm) at a temperature of 27C was considered. Using the approximate analytic expression below [4] for the equilibrium threshold voltage (V_{th}) we obtain V_{th} = 283.6 mV.

$$V_{th} = V_{fb} + 2\phi_f + \gamma\sqrt{2\phi_f} \qquad (6)$$

III. THRESHOLD VOLTAGE DEFINITIONS

A. *The g_m/I_D and the g_m/I_D change ($d(g_m/I_D)/dv_G$).*

The normalized charge (q_I) is defined in (7), the model equations (5) and (4) are normalized in (8) and (9). Equations (8) and (9) can be normalized to their maximum values as shown in (10) and (11). As shown in Fig. 2, the g_m/I_D characteristic is a monolithically gradual process without a transitional characteristic. Thus, one possible metric is the relative to the peak drop (RPD), i.e. if q_I=1 produce a RPD of 50%. In contrast, the $d(g_m/I_D)/dv_G$ presents a peak between high and low values of q_I, then one possible simple metric is the peak position located for q_I=0.5.

$$q_I = \frac{Q'_I}{Q'_{IP}} \quad ; \quad Q'_{IP} = -nC'_{ox}\phi_t \qquad (7)$$

$$-\frac{d}{dV_g}\left(\frac{g_m}{I_d}\right) = \frac{1}{(n\phi_t)^2}\left(\frac{q_{IS}}{1+q_{IS}} + \frac{q_{ID}}{1+q_{ID}}\right)\left(2+q_{IS}+q_{ID}\right)^{-2} \qquad (8)$$

$$\frac{g_m}{I_d} = \left[n\phi_T\left(1+q_{IS}+q_{ID}\right)\right]^{-1} \qquad (9)$$

$$\left(\frac{g_m}{I_d}\right)_{nor} = \frac{g_m}{I_d}\left(\left(\frac{g_m}{I_d}\right)_{max}\right)^{-1} = \frac{2}{2+2q_I(v_g)} \qquad (10)$$

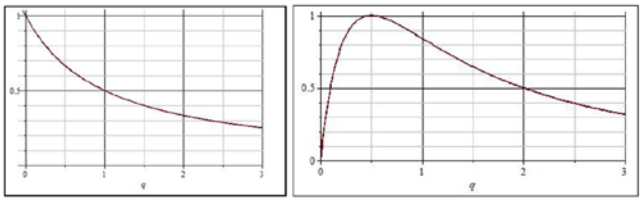
$$\left(-\frac{d}{dV_g}\left(\frac{g_m}{I_d}\right)\right)_{nor} = \frac{d}{dV_g}\left(\frac{g_m}{I_d}\right)\left(\frac{d}{dV_g}\left(\frac{g_m}{I_d}\right)_{max}\right)^{-1} = \frac{27}{4}\frac{q_I(v_g)}{\left(1+q_I(v_g)\right)^3} \qquad (11)$$

B. *Charge based threshold voltage definitions .*

V_{th} represents a physical change in the phenomenon that prevails in the current flow through the MOSFET as it goes from WI to SI. The charge-based definition of V_{th} used in this work and its difference with respect to the classical definition are summarized in Table 1. In the charge-based model V_{th} is the V_G value that produce a well defined normalized charge density ($q_{Ith} = q_I(v_g = V_{th})$) . If we choose q_{Ith}=1, this charge at threshold is defined as the point in which the drift and diffusion components of the drain current, are equal. On the other hand, if we choose q_{Ith}=0.5, this charge is defined as the point where the $-d(g_m/I_D)/dv_G$ characteristic is maximum.

IV. DRAIN VOLTAGE EFFECT (γ_D) ANALYTICAL MODELING

The effect of the drain voltage variation on the g_m/I_d V_{th} extraction techniques in long-channel MOSFETs can be regarded as an incremental error in the measured data with respect to the V_{th} point in the g_m/I_D MOSFET characteristic, as shown in Fig. 7. Additionally, for the $V_{thq0.5}$ this effect may be understood as a peak position shift in the $d(g_m/I_D)/dv_G$ MOSFET characteristic (Fig. 3). In [2, 5] it is presented the analytical analysis of $\Delta(g_m/I_D)$. From this analysis, the incremental error for V_{thq1} is given in eq. (12), and for $V_{thq0.5}$ it is given in (13). Another approach [1] is the calculation of Δv_G, which is developed for the calculus of the peak position shift in the $d(g_m/ID)/dv_G$ characteristic.



(a) (b)

Fig. 1 (a) g_m/I_D Vs q_I (b) $d(g_m/I_D)/dv_G$ Vs q_I characteristic.

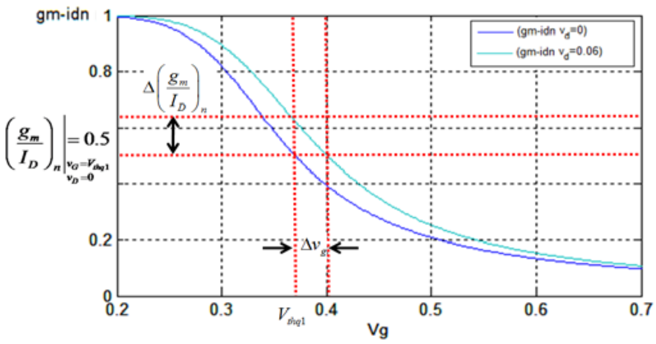


Fig. 2 Drain voltage effect in the g_m/I_D characteristic.

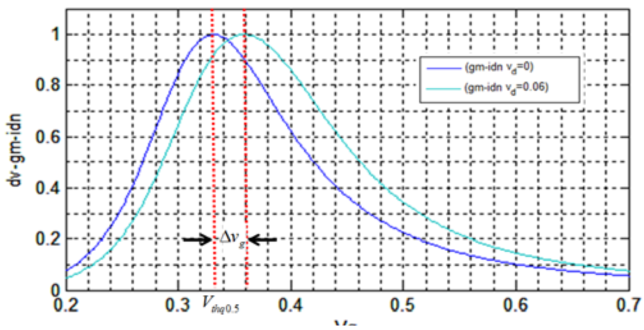


TABLE 1. Q BASED DEFINITION OF THRESHOLD VOLTAJE.

Notati.	V_{th} definition	Drop in Gm/Id V_{DS}=0 %	Value of q'_I $V_C=V_{th}$	Relative difference to classical definition $\phi_s = 2\phi_F$
V_{thq1}	$Q'_I = -nC'_{ox}\phi_t$	50	1	$\phi_t\left(1+n\ln\left(\frac{n}{n-1}\right)\right)$
$V_{thq0.5}$	$\max\left(-\frac{\partial}{\partial v_g}\left(\frac{g_m}{I_D}\right)\right)$	100/3	0.5	$\phi_t\left(1+n\left[\ln\left(\frac{n}{2(n-1)}\right)-0.5\right]\right)$

V. GM/ID METHODS USED FOR ϕ_t EXTRACTION

The circuit configuration for the gm/ID procedures is shown in Fig. 4. The g_m/I_D and $d(g_m/I_D)/dv_G$ characteristics are extracted as functions of the gate voltage for a parametric sweep of V_{DS}. In order to obtain these characteristics with less numerical error, both are calculated with the charge based expressions (4) and (5). These approaches avoid the numerical calculus of the derivates. Fig. 5 shows some normalized g_m/I_D vs. v_G simulated data and Fig. 6 shows some normalized $d(g_m/I_D)/dv_G$ vs. v_G simulated data.

$$\Delta\left(\frac{g_m}{I_D}\right)_{nq1} = \frac{2}{3+e^{1-\frac{V_D}{\phi_t}-\mathrm{LambertW}\left(e^{1-\frac{V_D}{\phi_t}}\right)}}-0.5 \tag{12}$$

$$\Delta\left(\frac{g_m}{I_D}\right)_{nq0.5} = \frac{2}{2.5+\left(\mathrm{LambertW}\left(0.5e^{\frac{\phi_t-2v_D}{2\phi_t}}\right)\right)^{-1}}-\frac{2}{3} \tag{13}$$

$$\Delta V_g = n\phi_t\left[\ln(0.5)+\ln\left(\sqrt{1+\frac{16}{1+e^{-\frac{2V_D}{3\phi_t}}}}-1\right)+0.25\left(\sqrt{1+\frac{16}{1+e^{-\frac{2V_D}{3\phi_t}}}}-3\right)\right] \tag{14}$$

A. g_m/I_D Method procedure

From (11), if we have $q_{Ith0.5}=0.5$, $q_{Ith0.5}=1$, we can calculate the g_m/I_D value for these q_I values, then $g_m/I_{Dnq0.5}=0.6666$, $g_m/I_{Dnq1} = 0.5$. Applying this criterion, valid for small values of v_{ds}, allows the extraction of the threshold voltage from the g_m/I_D characteristic (Fig. 2) by simply determining the gate voltage at which the normalized g_m/I_D characteristic is equal to $g_m/I_{Dnq0.5}$ or g_m/I_{Dnq1}. The slight variations of the slope factor and mobility with gate voltage are negligible over the required measurement range (linear region with small currents). In order to calculate a more accurate value of V_{th} without the γ_D influence, we use (12) and (13) to obtain the corrected value of g_m/I_D at V_{th} from (15) or (16), as indicated below

$$\left(\frac{g_m}{I_D}\right)_{nq0.5} = \frac{2}{2.5+\left(\mathrm{LambertW}\left(0.5e^{\frac{\phi_t-2v_D}{2\phi_t}}\right)\right)^{-1}} \tag{15}$$

$$\left(\frac{g_m}{I_D}\right)_{nq1} = \frac{2}{3+e^{1-\frac{V_D}{\phi_t}-\mathrm{LambertW}\left(e^{1-\frac{V_D}{\phi_t}}\right)}} \tag{16}$$

B. $d(g_m/I_D)/dv_G$ procedure

Equation (10) shows that at the threshold voltage ($q_{Ith0.5}=0.5$) the $d(g_m/I_D)/dv_G$ characteristic has its peak value. The application of this criterion, valid only for small values of v_{ds}, allows extracting the V_{th} from the $d(g_m/I_D)/dv_G$ characteristic (Fig. 3) by simply determining the gate voltage of the peak value of $d(g_m/I_D)/dv_G$ characteristic. In order to calculate a more accuracy value of V_{th} without the γ_D influence, from (14) we get the V_{th} corrected (17).

$$V_{th} = V_{gth}(V_{ds} \neq 0)_m - \Delta v_G \tag{17}$$

VI. POWER ERROR CORRECTION ANALYSIS

A. Threshold voltage numerical calculus

Using the circuit of Fig. 4 the g_m/I_D characteristic with $v_{ds}=0$ (Fig. 7) is obtained. From the v_{thq1} and v_{thq2} definitions, summarized in Table 1, the V_{th} voltages are calculated (18). In order to obtain an accurate value of n, this value (19) is extracted from the simulated n vs v_G characteristic . With the value of n and the relative difference to classical V_{th} definition, we obtain (20).

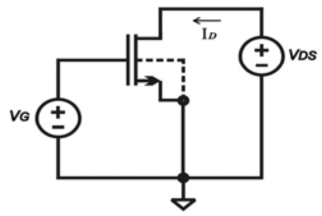


Fig. 4 Circuit topology for measuring the gm/ID characteristic.

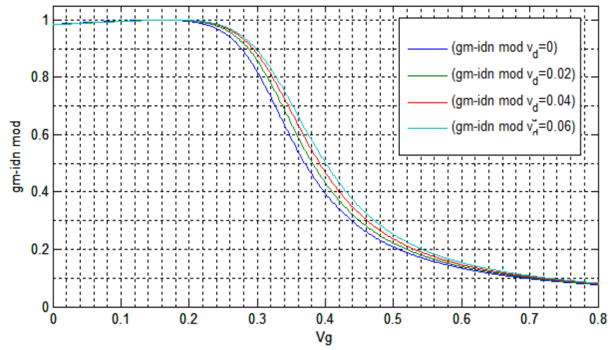


Fig. 5 Some normalized g_m/I_D vs. v_G characteristic results.

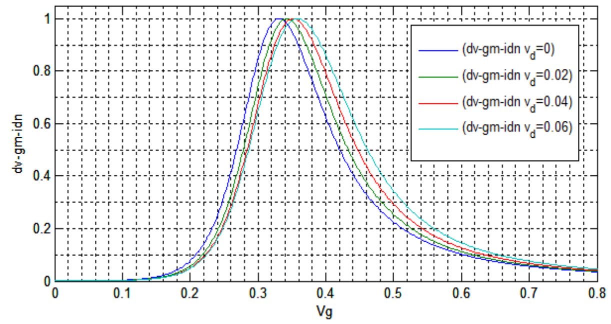


Fig. 6 Some normalized $d(g_m/I_D)/d\,v_G$ vs. v_G characteristic results.

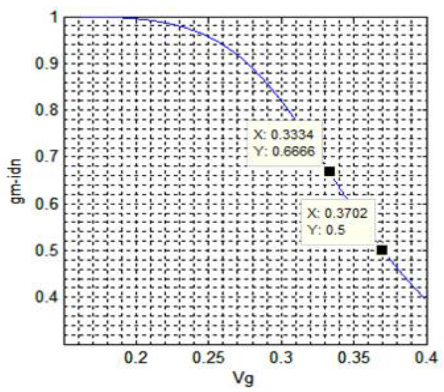


Fig. 7. Normalized g_m/i_d con $v_{DS}=0$

The consistency of a V_{th} extraction method can be checked through the simulation results (286.7 mV, 285.8 mV) and the V_{th} obtained for the analyzed fabrication process (283.6 mV) . Consistency means that the extracted value of V_{th} must be very close to the V_{th} calculated from the analytic expression.

$$v_{thq0.5} = 333.4 \text{ mV} \quad ; v_{thq1} = 370.2 \text{ mV} \tag{18}$$

$$n(v_{thq0.5}) = 1.177 \quad ; \text{n}(v_{thq1}) = 1.174 \tag{19}$$

$$v_{th1} = 286.7 \text{ mV} \quad ; v_{th2} = 285.8 \text{ mV} \tag{20}$$

B. V_{th} extarction from g_m/I_D and $d(g_m/I_D)/dv_G$ procedures

From the proposed procedures in section IV, we obtained the V_{thq} data with and without correction, from the g_m/I_D and $d(g_m/I_D)/dv_G$ characteristics simulated for a parametric sweep of the v_{DS} (0.1mV, 10mV, 20mV, 30mV, 40mV, 50mV). Following the topology of the Fig. 4, the V_{th} extracted with their error associated to the γ_D are presented in Table 2, Table 3, and Table 4.

Table 2. g_m/I_D Vth extraction procedure without correction results.

vd	(gm/Id)n (mV)		vds≠0 error without correction factor (mV)	
(mv)	Vthq1	Vthq0.5	Δ Vthq1	Δ Vthq0.5
0.1	370.7	334	0.5	0.6
10	375.9	339.1	5.7	5.7
20	381.5	344.2	11.3	10.8
30	386.7	348.9	16.5	15.5
40	391.6	353.2	21.4	19.8
50	396.3	356.9	26.1	23.5
mean	383.8	346.1	13.6	12.7
max	396.3	356.9	26.1	23.5

Table 3. g_m/I_D Vth extraction procedure with correction results.

vd	Δ (gm/id)n	(gm/Id)n (mV)		vds≠0 error with correction factor	
(mv)	(mv)	Vthq1	Vthq0.5	Δ Vthq1	Δ
0.1	2.4	370.1	333.4	0.1	0
10	24.1	370.1	333.4	0.1	0
20	47.5	370.1	333.5	0.1	0.1
30	69.6	370.1	333.6	0.1	0.2
40	89.7	370.1	333.8	0.1	0.4
50	107.3	370.3	333.9	0.1	0.5
mean	56.8	370.1	333.6	0.1	0.2
max	107.3	370.3	333.9	0.1	0.5

Table 4. $d(g_m/I_D)/dv_g$ Vth extraction procedure results.

vd	(d(gm/Id)/dvg)n (mV)	vds≠0 error without correction factor (mV)	Δ vth	(d(gm/Id)/dvg)n (mV)	vds≠0 error with correction factor (mV)
(mv)	Vthq0.5	Δ Vthq0.5	(mv)	Vthq0.5	Δ Vthq0.5
0.1	332.1	1.3	0.04	332.06	1.34
10	337.1	3.7	3.69	333.41	0.01
20	342.2	8.8	6.93	335.27	1.87
30	347.7	14.3	9.72	337.98	4.58
40	352.2	18.8	12.09	340.11	6.71
50	355.6	22.2	14.07	341.53	8.13
mean	344.50	11.50	7.80	336.70	3.80
max	355.60	22.20	14.07	341.53	8.13

C. PEC calculus of gm/Id Methods

Defining the PEC as in (21), we can calculate the PEC of the mean error and the PEC of the maximum deviation error for the gm/Id characteristics. The PFC obtained is presented in the Table 5. In spite of the significant PEC in the g_m/I_D, the accuracy of the v_{th} extraction was very high (>97%).

$$PEC = 100 \cdot \left(1 - \frac{E_c}{E_0}\right) \tag{21}$$

VII. CONCLUSION

This work extends that of [2] in the study of the gm/I_D power correction in present of drain voltage effect. The consistency of the numerical simulations implemented was cheeked. It is shown that the correction procedure proposed in g_m/I_D method is more accuracy than the correction procedure proposed in $d(g_m/I_D)/dV_G$ method, for long-channel MOSFETs in a 0.35 μm CMOS process.

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Table 5. Power correction factor summary.

Extraction procedure	Correction	Vthq	mean error		PEC	maximum deviation		PEC
		(mV)	(mV)	%	%	(mV)	%	%
(gm/Id)n	No	333.4	13.6	4.08	0.00	26.1	7.83	0.00
(gm/Id)n	Yes	333.4	0.1	0.03	99.26	0.5	0.15	98.08
(gm/Id)n	No	370.2	12.7	3.43	0.00	23.5	6.35	0.00
(gm/Id)n	Yes	370.2	0.1	0.03	99.21	0.5	0.14	97.87
(d(gm/Id)/dvg)n	No	333.4	11.50	3.45	0.00	14.07	4.22	0.00
(d(gm/Id)/dvg)n	Yes	333.4	3.80	1.14	66.96	8.13	2.44	42.18

REFERENCES

[1] T. Rudenko, V. Kilchytska, M. K. M. Arshad, J. Raskin, A. Nazarov and D. Flandre, "On the MOSFET threshold voltage extraction by transconductance and transconductance-to-current ratio change methods: part I—effect of gate-voltage-dependent mobility," Electron Devices, IEEE Transactions on, vol. 58, pp. 4172-4179, 2011.

[2] O. F. Siebel, M. C. Schneider and C. Galup-Montoro, "MOSFET threshold voltage: Definition, extraction, and some applications," Microelectron. J., vol. 43, pp. 329-336, 2012.

[3] A. Ortiz-Conde, F. Garcıa Sánchez, J. Liou, A. Cerdeira, M. Estrada and Y. Yue, "A review of recent MOSFET threshold voltage extraction methods," Microelectronics Reliability, vol. 42, pp. 583-596, 2002.

[4] M. C. Schneider and C. Galup-Montoro, CMOS Analog Design using all-Region MOSFET Modeling. Cambridge University Press, 2010.

[5] M. C. Schneider, C. Galup-Montoro, M. B. Machado and A. I. A. Cunha, "Interrelations between threshold voltage definitions and extraction methods," Proceedings of Nanotech, pp. 868-871, 2006.

[6] D. Flandre, V. Kilchytska and T. Rudenko, " Method for Threshold Voltage Extraction Applicable in Advanced MOSFETs With Nonlinear Behavior Above Threshold," Electron Device Letters, IEEE, vol. 31, pp. 930-932, 2010.