Study and Development of Interface Circuit for Power Harvesting using CMOS Technology

Leandro Ciscoto[1], Student Member, IEEE, and Nobuo Oki[1], Member, IEEE.
[1]Department of Electrical Engineering – UNESP – Ilha Solteira-SP, Brasil, leandrociscoto@gmail.com, nobuo@dee.feis.unesp.br

***Abstract*— The main objective of this study is the design and development of an interface circuit using CMOS technology, to Power Harvesting generated by piezoelectric transducers coupled to a mechanical system on the resonance frequency. The energy is stored in a capacitor for use later. A limitation of this system is the low amount of power generated. Conventional methods of converting AC current to DC current, like full-wave rectifiers using common diode, causing large voltage drops by decreasing the extraction power. A solution is to use integrated circuits which consume very low power and provide a reduction of losses and thus improve the efficiency of the system. We Will present some topologies using CMOS technology.**

Keywords— Power harvesting; piezoelectric transducers; CMOS technology; autonomous circuit.

I. Introduction

Energy harvesting is important in applications where battery replacement is impossible or the location is not favorable, such as embedded sensors in buildings, medical implants and remote sensors. In these applications, the problem is how to provide the power required by these devices autonomously [1].

A possible solution is to take advantage of some environmental energy to generate electricity. One alternative is the transformation of mechanical vibration into electrical energy using piezoelectric materials.

Piezoelectric materials are materials that can transform mechanical energy into electrical energy and vice versa. When the material is subjected to vibration there is a potential difference between its terminals, which can be stored and then used [2].

The electrical energy from a piezoelectric transducer coupled to a vibrational system is usually very low, dependent of load and in alternating current (AC), which makes the energy storage on capacitors or batteries impossible. Therefore, it is necessary to develop an interface circuit that makes the conversion to direct current (DC) with low consumption and reduced losses. The use of this energy has become possible thanks to the development of integrated circuits with low power consumption [1]. The focus of this work is study and develop an interface circuit using CMOS technology.

II. Power Harvesting

A. Mechanical system

On this study, it was considered the mechanical system of Fig. 1. It consists of a massive rigid support and a flexible steel beam where piezoelectric transducers are fixed. When the beam is subjected to an external force (the shaker machine), piezoelectric transducers are subjected to a vibration that is converted into electrical energy. The shaker represents the environment vibrations and excite the beam sinusoidly in the resonance frequency to increase the extraction power.

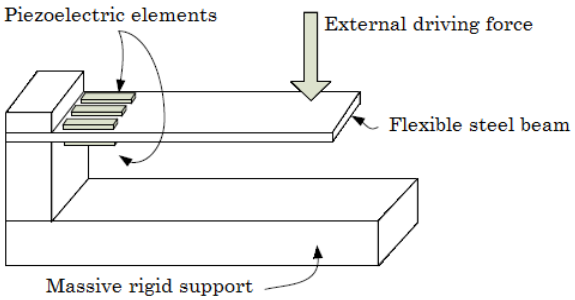

Fig 1: Electromechanical structure of a power generator. Adapted from: Souza (2011).

B. Electrical equivalent circuit

Consider the system of Fig. 1 in the resonance frequency, when the focus is only on the design of the interface circuit, the uncoupled model shown in fig. 2(b) can be used [3]. It consists of a current source in parallel with a capacitor, where the capacitor is an internal parameter of the piezoelectric transducer [2].

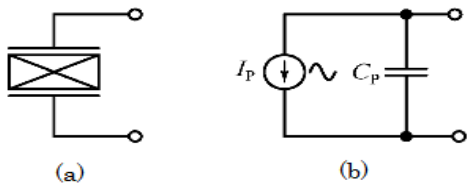

Fig 2: (a) Symbol, (b) uncoupled model of the piezoelectric harvester.

For this work, it was considered the piezoelectric transducer PSI - 5HE, 5H type, manufactured by Piezo Systems, Inc., whose parameters of the circuit are shown in Table I.

TABLE I: Parameters for simulation of the mechanical system.

Parameter	Value
I_P (μA)	390
C_P (nF)	100
F_P (Hz)	168.1

III. Performance Analysis

In this chapter it is discussed some of the literature and conventional circuits using CMOS technology proposed to optimize energy harvesting.

A. Piezoelectric connected to a full wave rectifier

A full wave rectifier is used in the conversion AC to DC and thus make possible the storage of energy generated by the piezoelectric. The circuit configuration is shown in Fig. 3. The diode MBR320 used is the type Schottky barrier and has a low voltage drop in conduction. A 10 μF capacitor is used to filter the ripple of the rectified wave.

The circuit was simulated and the value of the load resistance was varied, in order to analyze the system performance. The output power as a function of load is shown in Fig. 4. The output voltage is rectified with a small ripple voltage. Since the variable load is connected in parallel, the output power can be calculated using equation 1 [3].

$$P_{out} = \frac{Vout^2}{R_L} \qquad (1)$$

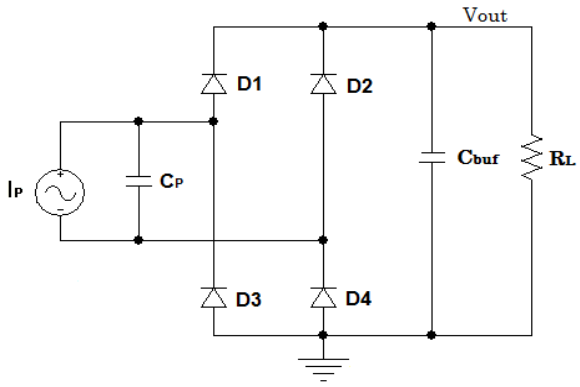

Fig 3: Piezoelectric connected to full wave rectifier.

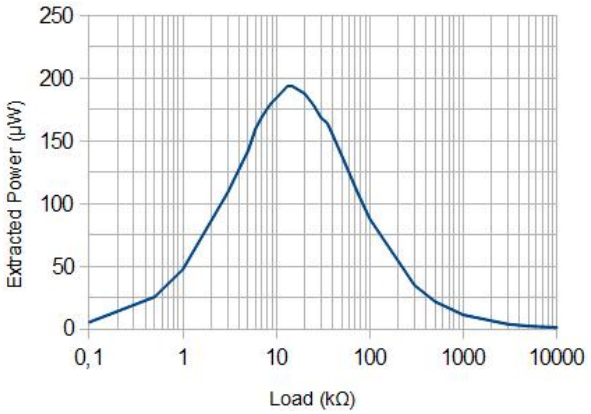

Fig 4: Extracted power using a full wave rectifier.

Analyzing the Fig. 4, the maximum output power is approximately 194 μW and occurs when the load is 15 kΩ. The average output voltage is V_{AVG}= 1.7 V and the drop voltage on the diode, for this load, is V_{AK} =0.16 V and the average current is 60.2 μA. Since there are a series of two diodes, the total drop voltage in the rectifier circuit is V_{AK}=0.32 V, so the losses in the diodes totalizes approximately 20 μW. The losses in the diodes appear to be small, however, as the output power is also small, this loss becomes significant. To minimize these losses, Peters et al. (2008) proposed a rectifier circuit using MOSFETs with very low losses, called passive negative voltage converter (pNVC).

B. Passive negative voltage converter

PNVC configuration is shown in Fig. 5. The circuit operates as a full-wave rectifier. The voltage of the MOS transistor is related to the threshold voltage (V_T), which strongly depends on the used process and temperature. Furthermore, V_T could increases during operation due to the body effect [4].

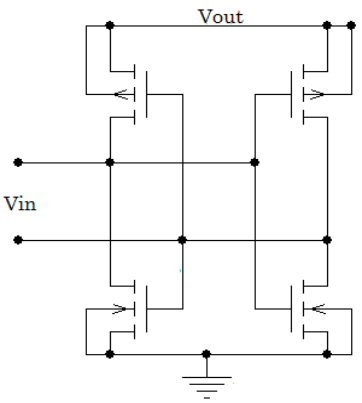

Fig 5: Passive negative voltage converter circuit.

However, this circuit cannot be used to charge a storage capacitor because it has not reverse current blocking capability. If the output voltage is higher than input thus, current can flow back. Due to this a second stage is necessary to realize a full rectifier as shown in fig. 6 [4]. The second stage can be a Schottky diode or an active diode. In this configuration, one drop voltage on the diode can be saved.

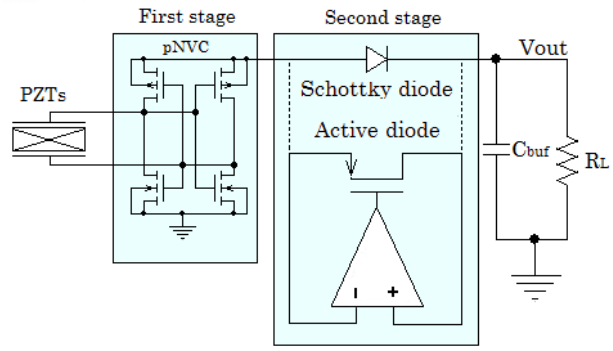

Fig 6: Active rectifier connected between the harvester and the Storage capacitor with ohmic load. Adapted from: Peters (2008)

The circuit was simulated using a Schottky diode, MBR320, in the second stage of the circuit. The load was varied to examine the behavior of the system. The diode conducts when the voltage at pNVC is greater than the voltage on the capacitor. Fig. 7 shows the output power as a function of load.

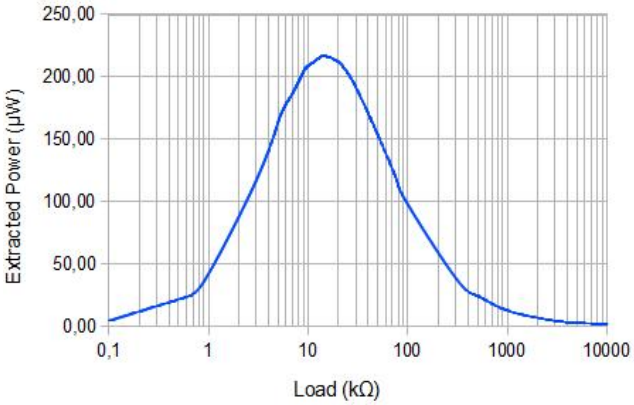

Fig 7: Extracted power using a pNCV rectifier with Schottky diode.

The maximum output power was increased of 11.3 %, from 194 µW to 216 µW for optimum load of 15 kΩ, compared with the full-wave rectifier using Schottky diode. The average output voltage is V_{AVG}= 1.8 V. However, in this configuration there is still a large drop voltage on the diode, V_{AK} =0.16 V, which decreases the output power. The alternative is to replace the Schottky diode by an active diode, decreasing the drop voltage significantly, and thus increasing efficiency. Now, however, the consumption of the control circuit should be taken into consideration. These simulations will still be held in the continuation of this study.

IV. Another Interfaces

In this chapter are presented some structures that will be studied and tested by simulations.

A. pNVC with active diode

Peters et al. proposed a circuit in which Schottky diode of the Fig. 6 is replaced by a PMOS transistor operating as switch, controlled by a comparator. The main objective is to reduce the drop voltage of the key in conduction and thus improve efficiency. When the voltage at pNVC is instantly higher than the capacitor voltage, comparator output drops to zero and the PMOS transistor conducts, transferring energy to the capacitor. When the voltage is instantly lower the pNVC, the comparator output voltage goes to high voltage level and the transistor is blocked, preventing discharge of the capacitor. In this structure the comparator is implemented using CMOS technology and requires no external power supply. Also, the circuit can start with the capacitor discharged, i.e. it is not necessary a preload on the capacitor.

B. SECE Interface

Hehn et al. proposed an interface called Synchronous Electric Charge Extraction (SECE) as shown in Fig. 8. Initially, there is an open circuit and the energy generated by the piezoelectric is stored in the electric field of the internal capacitor. When the voltage reaches the peak, the switch S_1 is turned on allowing the exchange of energy of the electric field of the capacitor to the magnetic field of the inductor. When the voltage is zero volts, the switch S_1 is turned off and the switches S_2 and S_3 are turned on. Now, there is a transfer of energy from the magnetic field of the inductor to the electric field of the storage capacitor. At the same time, the internal capacitor is being charged again. When the current is zero ampere on the inductor, all the energy has been transferred, then S_2 and S_3 are turned off, restarting the process. The circuit was also implemented using CMOS technology and will still be tested and simulated to compare with the results obtained in other settings.

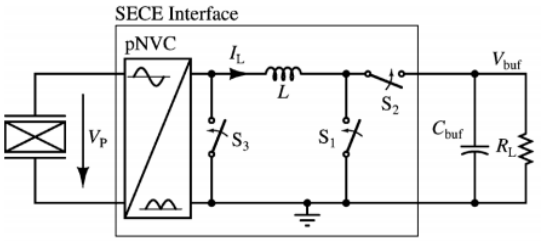

Fig 8: SECE interface configuration. Source: Henh (2012)

V. CONCLUSIONS

Full-wave rectifiers are generally used in interface circuits for energy harvesting from piezoelectric transducers. The conventional structures using passive diode are not interesting, because they have relatively high conducting drop voltage, decreasing the efficiency. So, topologies with active diodes using CMOS technology, like integrated circuits, has been a great alternative because it reduces considerably the losses in driving. Also, the interface circuit should be able to start with the capacitor discharged, otherwise, it makes impossible the practical applications in remotes places.

VI. REFERENCES

[1] Lefeuvre, E., Badel, A., Richard, C. E Guyomar, D. “Piezoelectric energy harvesting device optimization by synchronous electric charge extractions” J. Intell. Mater. Syst. Struct., Vol. 16, No. 10, pp. 865-876, 2005.

[2] Souza, F. S. Title: Power Harvesting System using Piezoelectric Transducers. 2011. (Master Degree in Electrical Engineering). Engineering College of Ilha Solteira, UNESP,SP.

[3] Hehn, T. et al., “ A fully autonomous integrated interface circuit for piezoelectric harvesters”, IEEE Journal of Solid State Circuits, Vol. 47, No. 9, pp. 2185-2198, September 2012.

[4] Peters, C., Spreemann, D., Ortmanns, D. M. E Manoli, Y., “A CMOS integrated voltage and power efficient AC/DC converter for energy harvesting applications,” J. Micromech. Microeng., vol. 18, p. 104005, 2008.

[5] A. Sedra, K. Smith. Microelectronic. Pearson Prentice Hall, 5th edition, 2007.