EFFECT OF TEMPERATURE REDUCTION ON ANALOG PARAMETERS OF SINGLE GATE SOI TRANSISTORS

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Abstract: In this paper we will discuss the temperature effects on analog parameters of single gate SOI transistors, both by comparing results obtained on two-dimensional numerical simulations and results obtained from measurements on fabricated devices. It is shown that the temperature reduction provides higher saturation transconductance, g_m/I_{DS} ratio and Early voltage, while higher output conductance and lower breakthrough voltage.

1. Introduction

SOI (Silicon On Insulator) technology is an alternative for the conventional CMOS technology for the fabrication of integrated circuits with ultra large scale integration [1]. In this technology, the devices are fabricated in a thin silicon layer, so that the device operates fully depleted, dielectrically insulated from other devices not only by the field oxide, but also by a buried oxide. SOI technology has shown to efficiently lower the performance degradation due to short channel effects and eliminating other undesirable effects, such as the parasitic tiristor and high parasitic capacitances [2]. In comparison to conventional MOS transistors, SOI MOSFETs offer higher transconductance and voltage gain, both important analog parameters [3]. Figure 1 shows the cross-section of a SOI transistor.

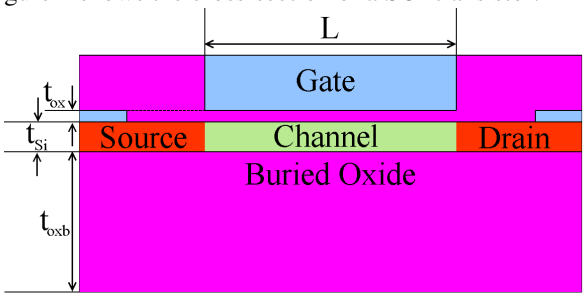

Figure 1 - Thin Silicon Layer SOI Transistor Structure

Additionally to the benefits provided by the use of SOI technology, the operation of MOSFETs at low temperature is known to improve devices characteristics. The combination of increased carrier mobility, improved saturation velocity and reduced subthreshold slope and leakage current, provided by the temperature roll-off, results in better device performance in comparison to room temperature operation [4]. The study of low temperature on the operation of microelectronic devices is particularly important for some applications, like aerospatial electronics, for example [5].

In this work, the effect of temperature over the analog parameters of SOI nMOS transistors is presented. The study is done by means of simulated and measured results.

2. Temperature Effects

The temperature has a lot of influence on MOS transistor characteristics. The electric field independent mobility (μ_0) is resulting by field independent scattering mechanisms due the lattice, neutral-impurities, ionized impurities and carrier-to-carrier [8, [**9**]. Their behavior with the temperature is so that μ_0 increases as the temperature goes down. The field independent mobility consists on the peak of mobility, and is reduced under the influence of the external fields caused by drain and gate voltage.

When silicon is submitted to low temperatures, carriers that were once free lose enough thermic energy to fall from the conductance band to the valence band, reducing both the intrinsic carrier concentration (n_i) and the extrinsic doping concentration (N_A). This leads to a rise on Fermi's potential (Φ_F). Since the average electric field on the channel (E_{eff}) is dependent on Φ_F, it will also increase, degrading the mobility as it can be seen below:

$$\mu_N = \frac{\mu_0}{1+\alpha_S \cdot |E_{eff}|} \quad (1)$$

Where α_S is the scattering coefficient and μ_N is the field dependent mobility. So, there is a higher peak of mobility at low temperature whereas a bigger mobility degradation. Despite the degradation, the overall value of μ_N is always larger in lower temperatures. It can be also noticed that not only because of Φ_F but also the bandgap width, which rises as the interatomic distance reduces in low temperature, V_{TH} increases.

One of the main figures of merit for the analysis of analog performance of MOS transistors is the intrinsic voltage gain, given by:

$$A_V = \frac{g_m}{g_D} = \frac{g_m}{I_{DS}} \cdot V_{EA} \quad (2)$$

Where g_m is the transconductance, g_D is the output conductance, V_{EA} is the Early voltage and I_{DS} is the current from drain to source, which are the parameters studied in this work.

The transconductance in saturation is given by [4] DE SOUZA, M.; Modelagem, Simulação e Fabricação de Circuitos Analógicos com Transistores SOI Convencionais e de Canal Gradual Operando em Temperaturas Criogênicas, São Paulo, 2008. :

$$\mathbf{g_m} = \frac{\mathbf{dI_{DS}}}{\mathbf{dV_{GS}}} = \frac{\mu_n \cdot C_{ox} \cdot W}{n \cdot L}(\mathbf{V_{GS}} - \mathbf{V_{TH}}) \quad (3)$$

Where n is the body factor, W is the channel width and L is the channel length. Considering devices biased at constant gate voltage overdrive ($V_{GS} - V_{TH}$), one can see that μ_N is the only variable influenced by the temperature. Therefore, it is possible to conclude that g_m improves at lower temperatures. A similar reasoning can be used for g_D [4]:

$$\mathbf{g_D} = \frac{\mathbf{dI_{DS,Sat}}}{\mathbf{dV_D}} = \frac{\mu_N \cdot C_{ox} \cdot W}{2 \cdot L \cdot n}(\mathbf{V_{GS}} - \mathbf{V_T})^2 \lambda \quad (4)$$

In this case, the current I_{DS} also contain the degradation factor λ, which accounts for the current dependence on V_{DS} in saturation and is a process dependent parameter [10]. So, in lower temperatures, the rise in saturation transconductance means better results, while the rise in the output conductance means worst results.

The g_m/I_{DS} curve translates the device capability to convert current in transconductance and establishes a relation between the output current obtained and its variation over V_{GS}. This relation reaches its maximum value in in weak inversion, given by:

$$\frac{g_m}{I_{DS}} = \sqrt{\frac{q}{n \cdot k \cdot T}} \quad (5)$$

And it can be seen that it is inversely proportional to the temperature. In strong inversion it can be given by:

$$\frac{\mathbf{g_m}}{\mathbf{I_{DS}}} = \sqrt{\frac{2 \cdot \mu_N \cdot C_{ox} \cdot \frac{W}{L}}{n \cdot I_{DS}}} \quad (6)$$

Where the dependence of the carriers mobility make it so the curve will present itself higher in low temperature when the on strong inversion. Ultimately, this parameter can be translated in efficiency for a transistor, since it shows the transitions between the inversion regimes in a clear manner.

3. *Discussion on Simulated Results*

Two-dimensional numerical simulations were performed with ATLAS program [11]. The models used for these simulations considers the mobility dependence on the doping concentration, ,transversal and perpendicular electric fields, band gap narrowing effects, carrier lifetime dependence on doping concentration , Auger recombination effect, impact ionization effects and incomplete ionization at lower temperatures [4].

The devices simulated are a single gated SOI nMOSFET transistors, with drain and source doping of $1x10^{20}cm^{-3}$, channel doping of $1x10^{16}cm^{-3}$, source and drain lengths of 0.25 µm, silicon thickness of 80nm, buried oxide thickness of 390nm and gate oxide thickness of 81 nm. Channel length was varied between 0.5 and 3 µm.

Figure 2 presents the simulated results obtained for the I_{DS} vs. V_{DS} and I_{DS} vs. V_{GS} curves for T = 100 K, 200 K, 300 K, 400 K, gate voltage overdrive of 200 mV ($V_{GT} = V_{GS} - V_{TH}$ = 200 mV) for the V_{DS} bias, drain voltage of 50 mV for the V_{GS} bias and channel length of 1.5 µm.

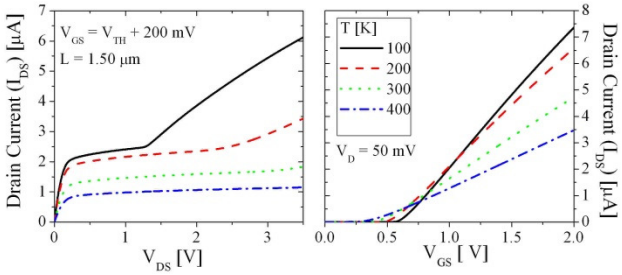

Figure 2 – Drain Current in Function of the Drain and Gate Voltages for $V_{GS} - V_{TH}$= 0.2 V and V_{DS} = 50 mV, L=1.50µm and different temperatures.

At the I_{DS} vs. V_{DS} curve, one can see that for lower temperatures the impact ionization effect, characterized by a sudden rise of current that happens because of carrier multiplication effect, is intensified [4]. This happens because the higher mobility and higher electric fields observed in this condition lead to more energized carriers, which facilitate the generation of hole/electron pairs.

On the I_{DS} vs. V_{GS} curve, the existence of voltage where the current is constant with temperature bias can be noticed. This point is called ZTC (Zero Temperature Coefficient) and happens due to the compensation of two effects: the higher V_{TH} in lower temperature, that lowers I_{DS} with constant V_{GS}, and the higher mobility, which raises I_{DS}. When these phenomena meet, the ZTC occurs.

From the I_{DS} vs. V_{DS} curves, the Early voltage has been extracted for $V_{GS} - V_{TH}$ = 0.2V and T = 100 K, 200 K, 300 K, 400 K, as a function of the temperature and is presented in Figure 3.

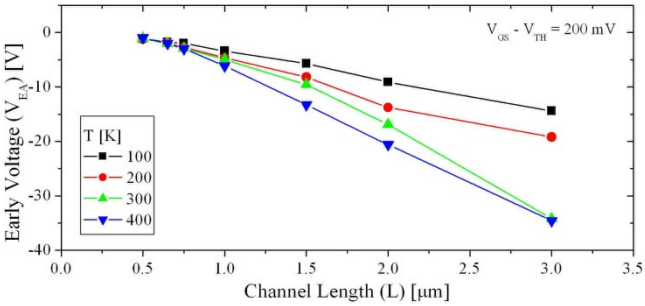

Figure 3 - Early Voltage in Function of the Channel Length for T = 100 K, 200 K, 300 K and 400 K and $V_{GS} - V_{TH}$ = 200 mV.

As it can be seen, the smallest absolute values for V_{EA} are attained at lower temperatures, with small difference between channel lengths. This reflects the intensified channel modulation effect, which happens because of the enlarged depletion region on the drain proximities and the pinch-off point dislocation.

By deriving the I_{DS} vs. V_{DS} curves the output conductance can be obtained, as shown below for the device with L= 1.50 µm biased at $V_{GS} = V_{TH}$ + 0.2 V. It can be seen that the conductance value shows to be worst in general, due to the mobility increase. Also, the temperature reduction promotes higher impact ionization, leading the device to breakdown at smaller drain voltages. To better analyze g_D, its values are shown in Figure 5, as well as the saturation transconductance values, both extracted the at V_{DS} = 1 V and V_{GT} = 200 mV, for different channel lengths.

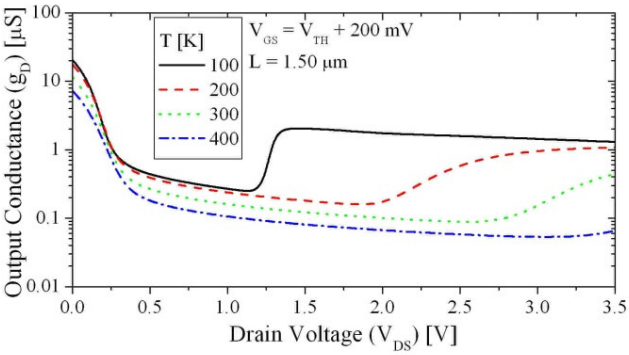

Figure 4 – Output Conductance in Function of the Voltage Between Drain and Source for Different Temperatures and Threshold Overdrive of 0.20V

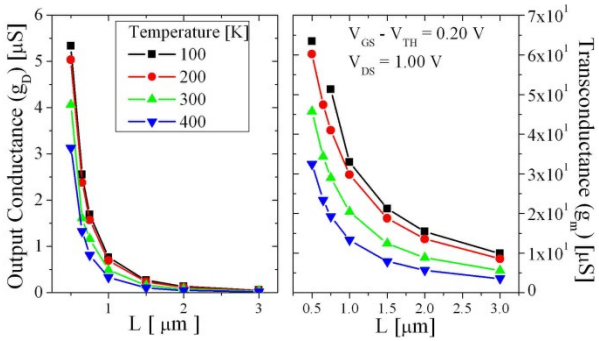

Figure 5 – Saturation Transconductance and Output Conductance for $V_{GS} – V_{TH} = 0.2$ V and $V_{DS} = 1$ V in Function of the Channel Length for for Temperatures of 100 K, 200 K, 300 K and 400K.

It can be noted that g_m rises with temperature lowering for all channel lengths, but it shows a more significant increase at shorter channel lengths. For L=3 µm, there is an increase of 178% with T reduction from 300K to 100K, while this increase is 95.24% for L=0.5um. As it can be seen, g_D also rises at lower temperatures. It is interesting to notice that, for longer channels, the differences between the results for different temperatures is more accentuated than in shorter devices. For example, with L=0.5 µm, the difference noted with temperature bias is about 2.21 µS while for L = 3 µm it is 0.034 µS.

The relation g_m/I_{DS} in function of the drain current, for L = 0.50 µm, 0.75 µm, 1.5 µm and 3 µm with V_{DS} = 1V, is shown in Figure 6 – The transconductance over the current between drain and source relation for VGS – VTH = 0.2 V and VDS = 1 V in function of the normalized current.

As this parameter is inversely proportional to temperature, higher values are observed at 100 K in comparison to room temperature. As seen above, the g_m/I_{DS} rise in strong inversion at lower temperature because of its dependence to the mobility (eq.6). Also, degradation can be noted at weak inversion for smaller channel lengths, due to short-channel effects.

By combining the results presented in Figure 5, the intrinsic voltage gain has been obtained and is exhibited below:

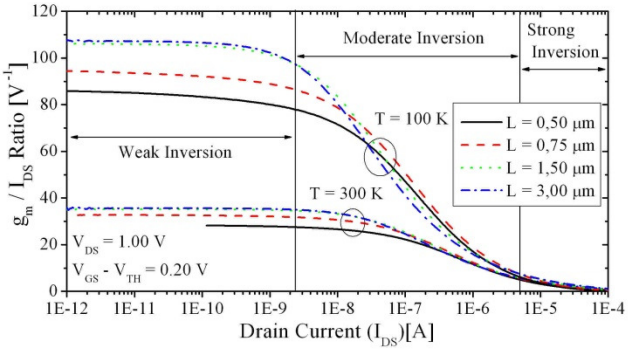

Figure 6 – The transconductance over the current between drain and source relation for $V_{GS} – V_{TH} = 0.2$ V and $V_{DS} = 1$ V in function of the normalized current.

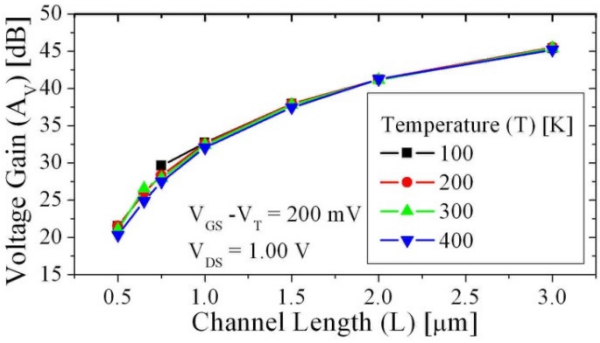

Figure 7 – Voltage Gain in Function of the Channel Length for Different Temperatures, Drain Voltage of 1 V and Threshold Overdrive of 0.20 V

As it can be seen, the voltage gain exhibits little dependence to the temperature, only visible at channel lengths smaller than 1 µm, when the output conductance is the most degraded due to short-channel effects.

4. Experimental Results

For this study, SOI transistors fabricated at the Microelectronic Laboratory of *Université Catholique de Louvain* (UCL) were used [13]. The devices were fabricated on SOI wafers with initial doping concentration of 10^{15} cm^{-3}, buried oxide thickness of 390 nm, gate oxide thickness of 30 nm, with silicon thickness of 80 nm. The threshold voltage is adjusted by doping the channel region with a concentration of 6 x 10^{16} cm^{-3}.The channel width is 18 µm, varying the channel length of 0.75, 1.00 and 2.00 µm.

The transistors were measured at temperature of 90 K, 150 K, 200 K, 250 K, 300 K and 380 K. The temperature was controlled using the equipment Variable Temperature Micro Probe System, model K20, from MMR Technologies, and the current curves were traced using the parameter analyzer Agilent 4156C.

The saturation transconductance and output conductance results are exhibited below. As in simulation results, the transconductance in higher V_{DS} is so that it is larger at lower temperatures. Also, smaller channels also present better g_m. It can also be seen that both simulated and experimental results present similar tendencies.

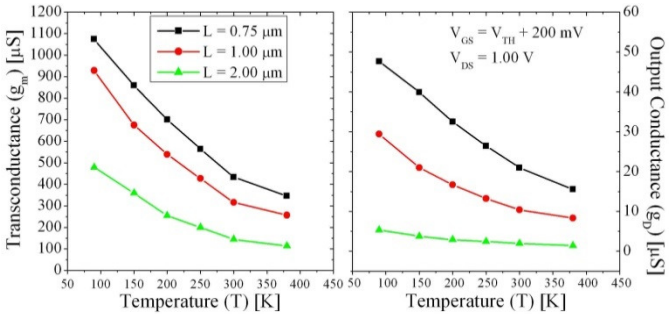

Figure 8 – Saturation Transconductance and the Output Conductance for $V_{GS} - V_{TH} = 0.2$ V and $V_{DS} = 1$ V in Function of the Temperature for Channel Lengths of 0.75 µm, 1µm and 2µm.

Figure 9 shows the measured results for the Early voltage as a function of the temperature, for different channel lengths and $V_{GS} = V_{TH} + 200$mV.

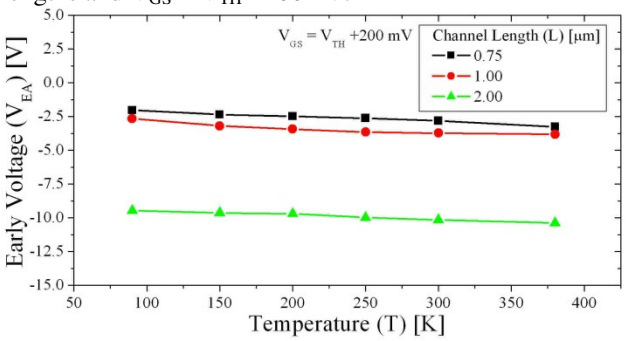

Figure 9 – Early Voltage in Function of the Temperature, with $V_{GS} - V_{TH} = 200$ mV and for L = 0.75µm, 1µm and 2 µm.

It can be noticed that V_{EA} shows to be almost constant in the studied temperature range. Still, the worst results were obtained at smaller L.

Due to the higher mobility, g_D degrades with lower temperatures. Even so, the rise on the transconductance compensates its degradation, maintaining the voltage gain as shown in Figure 10, confirming the simulated predictions presented in the previous section. Also, the channel length reduction has proven to decrease the intrinsic voltage gain.

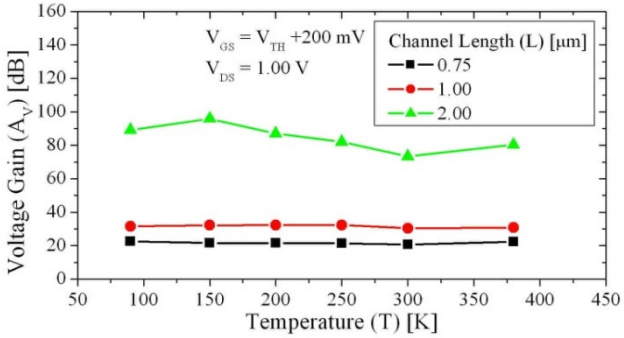

Figure 10 – Voltage Gain in Function of the Temperature, for $V_{GS} - V_{TH} = 0.2$ V and $V_{DS} = 1$ V na L = 0.75 µm and 1.00 µm

The relation g_m/I_{DS} is displayed in Figure 11 for the device with L=1um at several temperatures. It can be seen that lower temperatures will result in better g_m/I_{DS} values, especially in weak inversion. As device move to strong inversion, the temperature effect over this parameter is less pronounced.

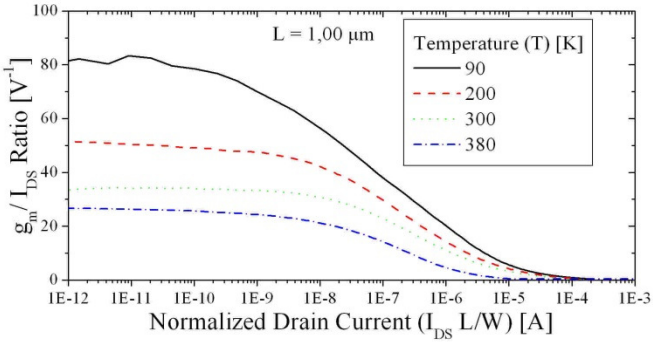

Figure 11 – Transconductance Over the Drain Current in Function of the Normalized Current with Channel Length of 1µm for Different Temperatures ($V_{DS} = 1$ V).

5. Conclusions

This paper showed the influence of the temperature lowering on the analog parameters of SOI transistors, both measured and simulated for different channel lengths. As we could see, shorter channel lengths degrade these parameters, especially the g_m/I_{DS} relation and the intrinsic voltage gain. The temperature reduction increases the transconductance and the output conductance, which compensate each other, resulting is the voltage gain nearly independent of the temperature.

6. References

[1] COLINGE, J.P. Silicon-On-Insulator Technology: Materials to VLSI. 3rd Ed. Massachusetts: Kluwer Academic Publishers, 2004.

[2] FLANDRE, D. et al; Comparison of SOI versus bulk performances of CMOS micropower single-stage OTAs. Electronics Letters, v.30, n.23, p.1933-1934, 1994.

[3] COLINGE, J.P.; Fully-depleted SOI CMOS for analog applications IEEE TED, v. 45, n. 5, p. 1010-1016, 1998.

[4] DE SOUZA, M.; Modelagem, Simulação e Fabricação de Circuitos Analógicos com Transistores SOI Convencionais e de Canal Gradual Operando em Temperaturas Criogênicas, São Paulo, 2008.

[5] GUTIERREZ, E. A., DEEN, J.; CLAEYS, C. L.; Low Temperature Electronics: Physics, Devices, Circuits and Applications, Academic Press, 1991.

[6] HAMMOUD, A. et al; Electronic Components and Circuits for Extreme Temperature Environments, Proceedings of the 2003 10th IEEE International Conference on Electronics, Circuits and Systems, vol. 1, p. 44-47, 2003.

[7] SAH, C. T. et al; Effect of zinc impurity in silicon solar-cell efficiency, IEEE Transaction on Electron Devices, v. 28, n. 3, p. 304-313, 1981.

[8] CONWELL, E.; WEIAAKOPF, V. F.; Theory of impurity scattering in semiconductors, Physics Review, v. 77, n. 3, p. 388-390, 1950.

[9] CAUGHEY, D. M.; THOMAS, R. E.; Carrier mobilities in silicon empirically related to doping and field, Proc. IEEE, v. 52, p. 2192-2193, 1967.

[10] SEDRA, A. S.; SMITH, K. C. Microeletrônica. Prentice Hall, 2007.

[11] ATLAS User's Manual, SILVACO (2007).

[12] SZE, S.M.; Physics of semiconductor devices, 2nd Ed. New York (EUA): John Wiley and Sons, 1981.

[13] IC Station, Mentor Graphics, U. S. A.