Sigma-Delta Modulator for high resolution A/D converters

José A. A. Andrade, Gilvandson C. Cavalcante, Guilherme M. Silva, Sandro A. P. Haddad, Fábio G. Costa
University of Brasília: Gama College – Gama-DF, Brazil
andrade.jaa.unb@gmail.com

***Abstract*—This paper presents a complete design of a Sigma-Delta modulator. The modulator system consists of a 1st order switched-capacitor integrator, a comparator with hysteresis, a bandgap voltage source (Vref), a 1-bit DAC and a current source circuit. This modulator is suitable for high-resolution and low-frequency A/D converters. The whole circuit was simulated using the CMOS AMS 0.35um IC process and the simulation results demonstrates a good performance of the implemented sigma-delta modulator.**

Keywords— Analog integrated circuit; mixed-signal design; Analog-to-Digital converters.

I. INTRODUCTION

The Sigma-Delta modulators represent an important function in several application nowadays in which is necessary to treat a signal according with the kind to continuous signal quantization. However, with the advent development of VLSI technology, there are several kinds of modulators to make some kind of digital communication. The Sigma-delta is the most used to convert signal analog-to-digital. Thus It is enables to design of complex and integrated system able to provide high conversion fidelity in the order of 20 to 30 bits of resolution, overcoming traditional converters [1].

This paper provides a brief survey about Sigma-Delta Modulator using AMS 0.35um technology. At the article will be approached the behavior of such a circuit block to explain better the parts of design. After will be showed the results reached with the circuit simulations. In the section *I* it presented some points about the motivation for using the Sigma-Delta Modulator. A description about the circuit and its blocks will be presents in the section *II*. The simulations results are given in the section *III*. In the section *IV* it shown the conclusions about this paper.

II. CIRCUIT DESCRIPTION

A simplified block diagram of the implemented Sigma-Delta modulator is shown in Fig.1. The modulator circuit consists of a 1st order switched-capacitor integrator, a hysteresis comparator, a bandgap voltage source (Vref), a 1-bit DAC and a current source circuit, which will provide the reference current to all the blocks inside the modulator.

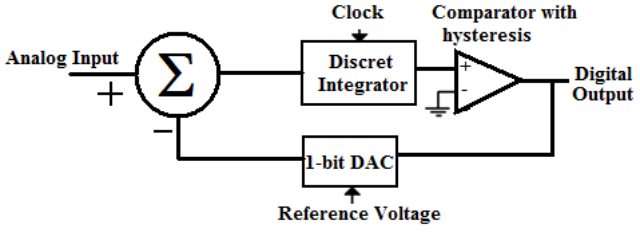

Fig. 1. Simplified block diagram of a first order Sigma-Delta Modulator [2].

A. Sigma-Delta Modulator

Usually, the operation of A/D converters is based on Nyquist principles, where the sampling frequency is minimum twice the desired signal bandwidth [3]. During the sample period some high frequency components from interference or noise could produce harmonics inside the signal bandwidth, resulting in an effect called aliasing. In order to reduce this effect, is necessary to limit the bandwidth of the input signal, i.e., an anti-aliasing low-pass filter must be implemented at the system input to remove all the undesired high frequency components.

Moreover, A/D converters present quantization noise (error), which is caused by uncertainty of the signal value between two consecutive levels of quantization [1]. It means the quantization noise is higher when the A/D resolution is lower.

With goal to obtain an A/D converter with lower quantization noise, and thus, with higher resolution, an oversampling frequency is required. It may reduce the quantization error through high speed switching. Introducing an oversampling in the sigma-delta modulator it is possible to obtain a higher Signal-to-Noise (SNR) ratio.

An A/D converter based in Sigma-Delta modulator shows optimal performance related to bit resolution. Usually, using this topology, it is possible to obtain 12 to 30 bits A/D converters. On the other hand, Sigma-Delta modulators present low or medium conversion speed, with sampling frequency varying from kHz to few MHz

A Sigma Delta converters architecture in composed of two main blocks: Sigma-Delta modulator and decimator filter. This paper focuses on the Sigma Delta modulator.

Sigma-Delta modulators allow the implementation of Analog-to-Digital converters, high-performance [3]. Among several option available for integrated implantation of this modulator, the technique of switched capacitor is adequate.

Conventional converters are implemented using the Nyquist sample rate.

$$SNR_{dB} = 6{,}02N + 1{,}76 = 20\log_{10}(L) + 1{,}76 \quad (1)$$

N-number of bits

L – number of levels ($L=2^N$)

Therefore, in the design of a analog-to-digital converter with resolution of 16-bits is necessary to have a Signal-Noise-Ratio (SNR) of about 98.08 dB. For a resolution of 24-bits it is necessary a SNR of 146,24 dB.

Nevertheless, in order to reduce the quantization noise, very often oversampling rate is used, i.e., a sample rate of more than twice the highest input frequency. In this way the SNR becomes.

$$SNR_{dB} = 6{,}02N + 1{,}76 + 10Log_{10}(OSR) \quad (2)$$

$$OSR = \frac{f_s}{f_{sig}} \quad (3)$$

The effect of oversampling to increase of ratio Signal-Noise (SNR) for a factor equal to 10 Log(k). Therefore, to get a resolution of one bit extra, in other words, to increase the SNR to 6dB it is necessary a oversampling rate of four times (k=4). The advantage of oversampling is a relaxation in the requirements of attenuation of the analog filter.

It can be said that using a higher oversampling ratio (OSR) allows better resolution of analog-to-digital converters for the same bits number.

In order to keep the oversampling rate with reason value a inside the threshold of technology it is possible to frame the frequency spectrum of quantization noise, called Noise Shaping.

Therefore, the accuracy of an oversampling ADC can be further increased by filtering the quantization noise in such a way that most of its power lies outside the signal band.

The switches which generates the charge transfers in the switched capacitor can be made in several ways, moreover, according to other sources it is recommended to design the switches complementary CMOS in which the reference voltage input can be any point of the circuit, this is an advantage in relation if compared to the MOS switched in which the necessary reference voltage needs to be the VDD of system.

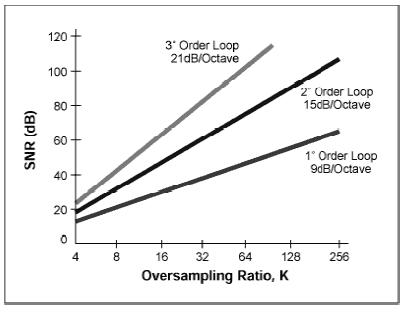

Fig. 2. The SNR of a modulatur $\sum\Delta$ of order N if expressed by

$$SNR_{dB} = \frac{3}{2}.\frac{2N+1}{\pi^{2N}}.OSR^{(2N+1)} \quad (4)$$

B. Switched Capacitor

In application at low-frequency filter is necessary resistor or capacitors with large values. Due to this fact, is not possible to design integrated circuit. For this purpose is necessary to use the Switched-Capacitor circuit i.e., is possible to get resistors large values with small values of clock frequency and capacitors. Care has to be taken that the overlapping clocks do not occur with the MOS switches.

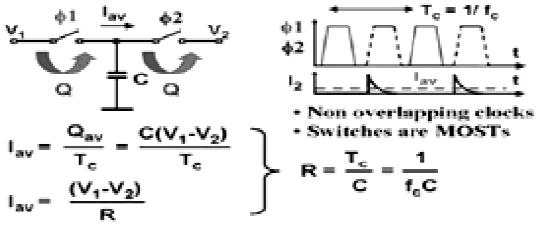

Fig. 3. Principle of operation switched-capacitor circuit [7].

One way to build non overlapping clocks are with latchs NAND circuts , i.e., the clocks have intervals defined for each time delay due to the propagation time in each inverter gate. As shown in Fig. 4.

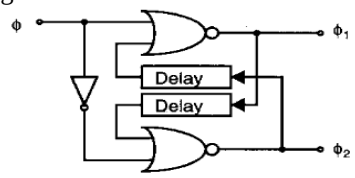

Fig. 4. Generate of non-overlaping clock[4].

Moreover, the switched-capacitor circuit can be used to build a simple-and-hold circuit, where the sampled signal frequency must be smaller twice time clock frequency looking at the principle of Nyquist Criterion. The large function of integrator is current into voltage convert, moreover, it does hold the sample defined by switched-capacitor circuit according Nyquist Criterion.

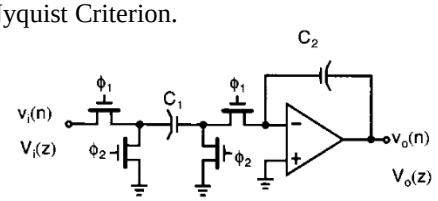

Fig. 5. Circuit used for sample and hold data by switched-capacitor and the discret integration.

In this work, the opamp topology chosen was the folded Cascode because this topology can offers a good Slew-rate, bandwidth and the gain necessary. The opamp implemented is shown in the Fig. 6.

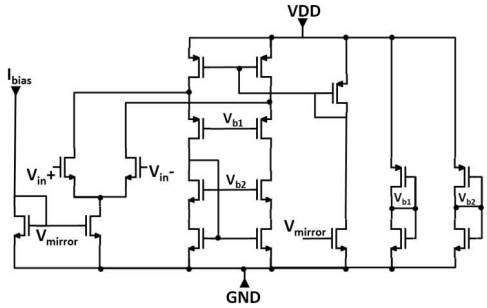

Fig. 6. Schematic of opamp Folded Cascode implemented.

C. Hysteresis Comparator

A comparator works like an operational amplifier, but specific for comparing two voltages, or currents, between their inputs [5]. It is done by comparing an analog signal with another, or with a voltage reference. In the end there is a comparison binary based exit signal that is basically a one bit convertor (analog to digital).

It is the quality of the comparator in which the input signal (*threshold)* vary depending on input (positive or negative trip). Simplifying, it's the difference between the levels of signal, where the comparator turns on or off. A little amount of hysteresis can be useful in a comparator circuit, since when, it reduce the circuit noise sensibility and help reducing multiple exit transitions, when the state change occurs. These methods can be divided in internal or external hysteresis. The external hysteresis uses positive feedback. When an input signal is affected by noise, the change can be slow. Since the input

voltage is similar from the reference voltage, a little noise can make the input voltage vary from the reference voltage. This very noise can cause some glitches that tend to release the circuit power away. Below its demonstrated the topology implemented of a hysteresis comparator.

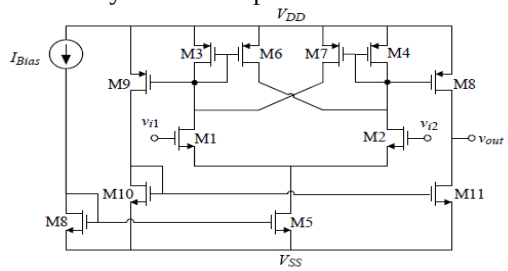

Fig. 7. Schematic of the comparator circuit [5].

D. Bandgap and Current Source

The voltage value and current in an integrated circuit depends on some parameters such as fabrication process variation, power supply and temperature. The purpose of circuit which can generate voltage reference or current which allow to keep a constant voltage or current independent of some fluctuation. This circuit are called current reference and BandGap.

Currente Reference

In a reference current source, wait to generate a current which has the minimum of dependence of fluctuation of circuit power supply [6]. Thus, the topology chosen for this job introduces a high independence grade of power supply (Vdd). The topology is illustrated in the Fig. 8.

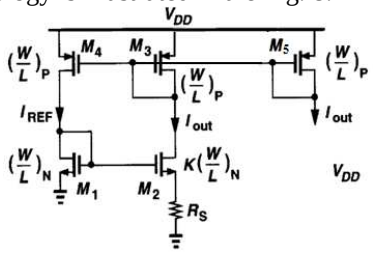

Fig. 8. Topology chosen to generate a reference current [6].

In the circuit of Fig. 6. the device M3 works as current mirror to M4. As both devices are iquals, the currents (Iref) and (Iout) have the same intensity. Observing the relation between M1 and M2 it can be noticed that there isn't any relation of current mirror between them, because they have different Vgs voltages due the Rs presence. The Rs resistor allows for defining the current in the circuit and supplies the difference between M1 and M2. For this circuit, the output current is illustrated in (5).

$$I_{OUT} = \frac{2}{\mu_n C_{ox}\left(W/L\right)} \cdot \left(\frac{1}{R_S{}^2}\right)\left(1-\frac{1}{\sqrt{K}}\right)^2 \quad (5)$$

For the adjustment of dimension of this circuit, did consider which it was considered the Iout current of 1uA and the voltage in the M2 terminal of 50mV. Thus, the Rs value is of 50kΩ. It was also considered that the proportionality constant K equal to 2. Therefore, the aspect reason of M2 was 0.59 and the M1 was half the value. Lastly, for M3 and M4, the value was defined with the same value of M1, therefore The Important is which the dimensions shall be equals.

Circuito Bandgap

The bandgap is a circuit to keep the voltage reference with minimum fluctuation due to the influence of temperature. The use of a bandgap circuit is justified to generate a reference voltage independent of temperature fluctuation relative to the reference voltage called bandgap [6]. This voltage has to be fixed in 1.25V. In this work, the bandgap circuit implemented is shown in the Fig. 9.

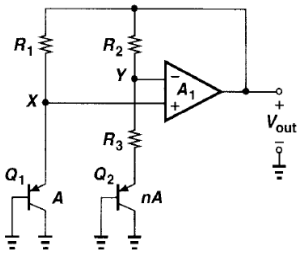

Fig. 9. Topology implemented for a bandgap circuit in this work [6].

In this circuit, in the voltage between the emitter and the base of transistor Q1 occurs a negative fluctuation with the increase of temperature. But the voltage difference between the emitters of Q1 e Q2 occurs a positive fluctuation with the increase of temperature. The opamp A1 is used for generating a virtual short circuit in the nodes X and Y. Adjusting the values of R1,R2 and R3, a Vout voltage of 1,25V can be gotten. In (6) illustrates the output value (Vout) of the circuit.

$$V_{OUT} = V_{BE2} + V_T \ln n \cdot \left(1+\frac{R_2}{R_3}\right) \quad (6)$$

In (6) V_{BE2} is the voltage between the base and the emitter of Q2, Vt is the thermal voltage of transistor and *n* and the number of time which Q2 is greater than Q1. The literatures show which R2 and R3 shall be calculated so that the constant of gain not inverter of A1 is close to 17.2 and R1 equal the R2 [6]. In this paper, the value of R1 and R2 are 10KΩ and R3 igual the 660Ω. The value calculated of (n) was 6, according with the calculations were put iguals transistor side by side for replace Q2.

III. Simulations Results

In this section some simulation results are presented. Each of the blocks was simulated with the objective of checking if its responses are within an acceptable range for this application. In this simulation the power supply in each circuit was of 3V and 1uA the bias current. The features of Sigma-Delta modulator are illustrated in Table 1.

TABLE I. Table Styles Summarized Performace of the Modulator

Technology	**CMOS AMS 0.35um**
Bias current	1uA (Self-bias)
Supply voltage	3V
Power dissipation	645uW
Order	1º
Sample frequency	1MHz
Bandwidth	1kHz

The bandgap circuit was simulated to check if the voltage reference of 1.25V was achieved. According said in the section 2.4, this circuit shall generate a constant voltage and independent of temperature. So, this circuit was simulated

considering which the temperature varies of -40ºC the 120ºc and which Vdd varies of 2.5V the 3.3V. Thus, the behavior of bandgap voltage generated can be see in the Fig. 10. The value of bandgap voltage is within 1.23V and 1.32V with a range variation aceitable for this first application.

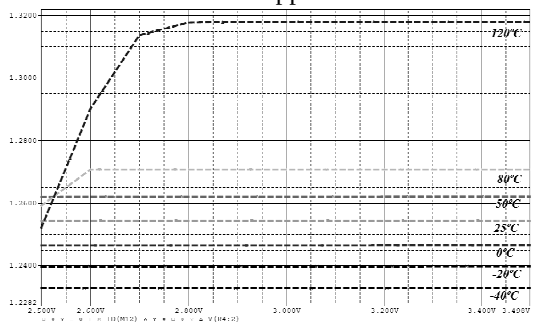

Fig. 10. Result of simulation of bandgap circuitWere checked the behaviors for 8 value of temperature within of fabrication scale.

The current source, also cited in section 2.4, shall generate a reference current, with the greater independence of Vdd possible. Its this simulation considered a fluctuation of Vdd between 2.5V and 3.5V. The reference current generated can be view in Fig. 11 in which within this fluctuation, the reference current was of 0.98uA the 1.04uA, having a low grade of dependence of Vdd.

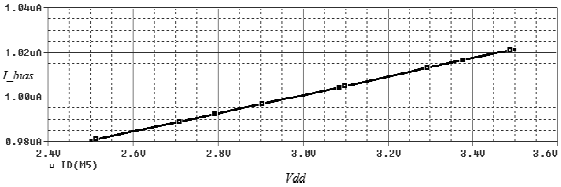

Fig. 11. Result of simulation of reference current souce.

For the simulation of comparator with internal hysteresis, consider a triangular input signal which fluctuates between 0 and Vdd. For this circuit, it is expected a positive and negative hysteresis of 0.01V in around of reference voltage in which was half of Vdd. The Fig. 12 illustrates the behavior of the output circuit, thus the histese checked was lower which 0.01V considered acceptable.

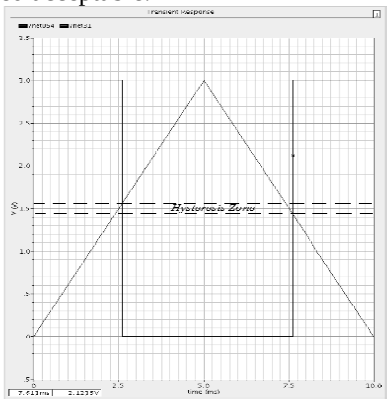

Fig. 12. Result of simulation of comparator.

The simulation of Switched-Capacitor can be view in the Fig. 13. The signal test had an amplitute of 1V and a frequence of 10kHz. The clock frequence of control switchs was 1Mhz and the delay of non-overlaping clock was 1.4 ns.

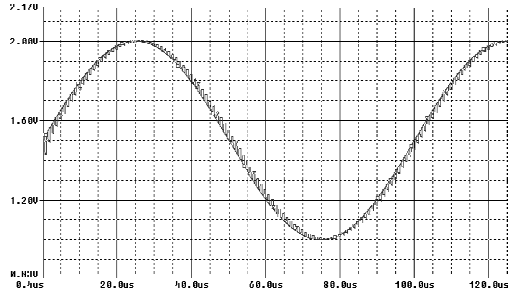

Fig. 13. Output Simulation of swiched-capacitor.

In the Fig. 14, is shown the output of modultator and the input signal. In this simulation, the input signal frequence was 100kHz and 1V of amplitute. The sampling frequence was 1Mhz. It can seen the modulation pattern varing with the amplitute of input signal.

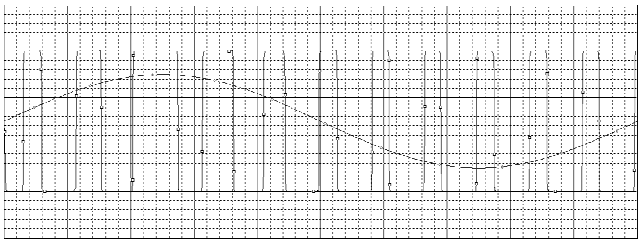

Fig. 14. Output Simulation of analog-to-digital converter.

IV. CONCLUSION

This paper has presented a Sigma-Delta modulator of 1ª stage using AMS 0.35um technology. In the circuit design was taken into account the simulation of each circuit block. i.e., due to this fact was possible to study the private behavior of the switched-capacitor, the band-gap and hysteresis comparator circuit. After the review, each circuit block were connected where the resulted was Sigma-Delta Modulator. In the next work will be increased the a 2nd order of circuit switched-capacitor integrator and included an anti-aliasing filter.

REFERENCES

[1] S. R. Norsworthy, R. Schreier and G. C. Temes, Delta-Sigma Data Converters: Theory, Design and Simulation, International Edition, IEEE PRESS, 1997, p. 500.

[2] S. P. Kommana, "First Order Sigma-Delta Modulator of an Oversampling ADC Design in CMOS Using Floating Gate Mosfets," Master of Science in Electrical Engineering, Thesis, Agricultural and Mechanical College – Lousiana State University, p. 118, December 2004.

[3] P. M. Aziz, H. V. Sorensen and J. V. Der Spiegel, "An Overview of Sigma-Delta Converter: How a 1-bit ADC achieves more than 16-bit resolution," IEEE Signal Processing Magazine, pp. 1053-5888, January 1996.

[4] D. Jhon and K. Martin, Analog Integrated Circuits Design, John Wiley & Sons, 1997, pp.394-444.

[5] P. E. Allen and D. R. Holdberg, CMOS Analog Circuit Design, 3ºed., Oxford, 2011, p. 784.

[6] B. Razavi, Design of Analog CMOS Integrateds Circuits, International Edition, McGraw-Hill, 2001, p. 706.

[7] Sansen, Willy M.C Analogo Design Essentials, published by Springer, 2006, p.485.