INFLUENCE OF LIGHTLY DOPED REGION LENGTH ON THE ELECTRICAL CHARACTERISTICS OF GRADED-CHANNEL SOI nMOSFET

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ABSTRACT

In this paper, we investigate, through two-dimensional simulations and experimental results, the analog characteristics of Graded-Channel Fully Depleted SOI nMOSFET Transistors, looking for the optimum L_{LD} length at different total channel lengths. The figures of merit for this analysis are the voltage gain and breakdown voltage. To attend this goal, experimental and simulated results will be presented, looking at the $I_D(V_D)$ and $I_D(V_G)$ characteristics, as well as the transconductance and output conductance.

1. INTRODUCTION

The Graded-Channel SOI nMOSFET Transistor (GC SOI nMOSFET) is a device proposed to improve the analog characteristics of SOI technology. It has an asymmetrical doping profile of acceptor impurities in the channel [1]. The highly and lightly regions are near, respectively, to the source and drain, as shown in Figure 1. In this figure, T_{oxf}, T_{oxb} and T_{Si} are the front gate oxide, the buried oxide and the silicon film thicknesses, respectively. L and L_{Ld} are the channel and lightly doped region lengths, respectively.

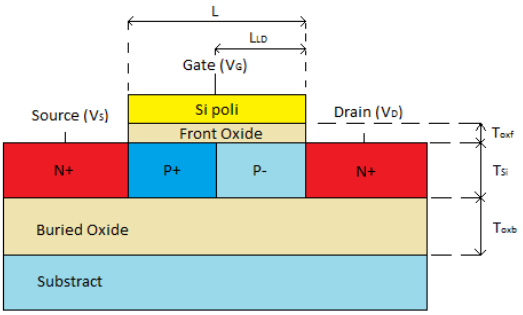

Figure 1 - GC SOI schematic cross section.

The threshold voltage (V_{TH}) is dependent on the doping concentration in the channel. As larger the doping level, higher the threshold voltage. This way, the lightly doped region (LD) reaches inversion before the highly doped on (HD). Therefore, the lightly doped region behaves as a drain extension towards the channel, therefore, the drain voltage is shifted to the interface between the lightly and highly doped regions, reducing lowering the effective channel length (L_{eff}) [1], which is approximately equal to L - L_{LD}. This channel length reduction increases the drain current and the lower doping concentration reduces the electric field peak, since the potential drop in the drain/channel junction is lower to the GC transistor in comparison to the uniformly doped transistor [1]. As a result, GC structure presents several advantages over the uniformly doped transistor, namely increase of drain current (I_D), tranconductance (g_m), that are related to the reduction of the effective channel length, increase of breakdown voltage (BV_{DS}) and the decrease of output conductance (g_D) and impact ionization effect, related to the reduction of doping concentration, and hence lower electric field near to the drain [2].

2. MATERIAL AND METHODS

In this study, experimental results obtained with transistors developed in 2µm technology by UCLouvain, Belgium [4] were initially used to verify the analog performance of GC transistors. The devices studied present total channel length of 0.75, 1 and 2µm, channel width (W) of 20µm, silicon film thickness of 80nm, gate oxide thickness of 31nm and buried oxide thickness of 380nm, highly doped region with doping concentration of $6.5\times10^{16}cm^{-3}$ and lightly doped region with $1\times10^{15}cm^{-3}$.

In order to investigate the existence of an optimized length for the lightly doped region, two-dimensional numerical simulations were performed with software ATLAS® [3], varying the total channel length and L_{LD}/L ratio.

3. EXPERIMENTAL RESULTS

Experimental samples of GC transistors are initially presented in order to show the advantages of this structure in comparison to uniformly doped transistors with same total channel length. Figures 2 and 3 present the $I_D(V_G)$ and $I_D(V_D)$ characteristics, respectively, GC SOI transistors with L=2µm and varying the L_{LD}/L relation. The $(L_{LD}/L)_{eff}$ relation can be calculated using the equation (1), which is obtained through the division between the drain currents for uniformly doped transistor and graded channel transistor, only valid at the beginning of the saturation [2].

$$(L_{LD}/L)_{eff} = 1 - I_D/I_{D,GC} \quad (1)$$

We can see that increasing the L_{LD}/L relation causes a larger drain current, which is related to the reduction of the effective channel length. Another advantage for this

structure is the increase of the breakdown voltage due to the reduction of the electric field in the channel/drain junction.

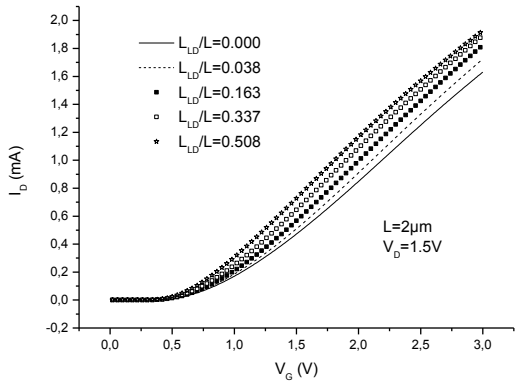

Figure 2 - $I_D(V_G)$ characteristic for L=2µm GC SOI, biased with V_D=1.5V.

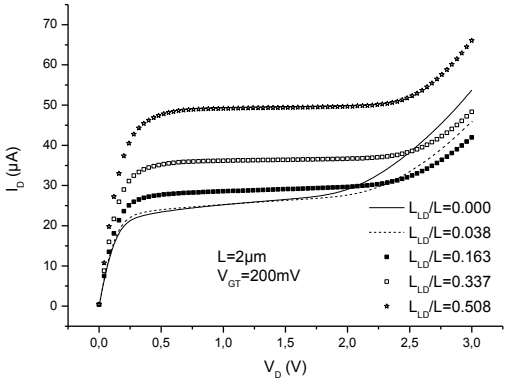

Figure 3 - $I_D(V_D)$ characteristic for L=2µm GC SOI, biased with V_{GT}=200mV.

Table I exhibits the breakdown voltage extracted for a GC SOI with L=2µm.

Table I - Breakdown voltage for L=2µm GC SOI.

$(L_{LD}/L)_{eff}$	BV_{DS} (V)
	V_{GT}=200mV
0.00	1.84
0.16	2.26
0.34	2.29
0.51	2.31

As reported in the literature, the breakdown voltage rises with the increase of the lightly doped length, as a result of the reduction of the electric field peak at the channel/drain junction to the GC transistor which lowers the impact ionization effect and, consequently, increases the breakdown voltage for all studied L_{LD}/L.

Figure 4 shows the transconductance and the output conductance as a function of L_{eff} for three different total channel lengths, extracted at $V_{GT} = V_{GF}-V_{TH}$ =200mV and V_D=1.5V. The results show that the reduction of L_{eff} benefits the transconductance, as expected. On the contrary, the effective channel length reduction contributes to reduce the output conductance, due to the reduction of electric field and the consequent effects.

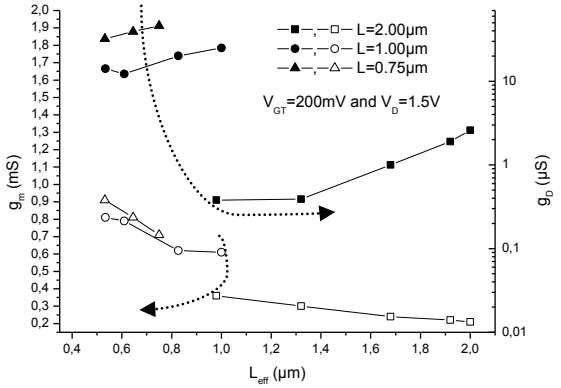

Figure 4 - Transconductance and output conductance as a function of L_{eff} with V_{GT}=200mV and V_D=1.5V.

The intrinsic voltage gain of the transistors is described by the equation (2) [5] and has been obtained using the previous results and is presented in Figure 5:

$$A_V = g_m/g_D \quad (2)$$

Figure 5 also presents the threshold voltage as a function of L_{eff} for the same channel lengths analyzed before.

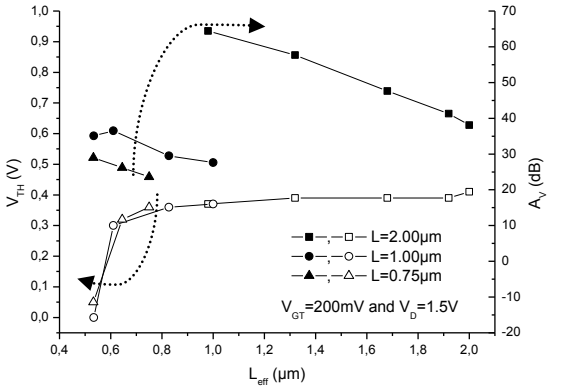

Figure 5 - Threshold voltage and voltage gain as a function of L_{eff} with V_{GT}=200mV and V_D=1.5V.

Analyzing these figures, we can note that for the same total channel length, the reduction of the effective channel length lowers the threshold voltage, indicating the occurrence of short channel effects for higher L_{LD}/L ratio. If the channel length is reduced, it is noted the increase of transconductance and output conductance for all effective channel length. Since the output conductance degradation is larger than the increase of transconductance, there is a reduction in the voltage gain for larger effective channel lengths.

4. TWO-DIMENSIONAL NUMERICAL SIMULATIONS

Figure 6 presents the $I_D(V_D)$ and $g_D(V_D)$ characteristics for several L_{LD}/L relations and L=2µm, biased with V_{GT}=200mV. As exposed before, the drain current suffers an increase when the L_{LD}/L relation rises because of the effective channel length reduction.

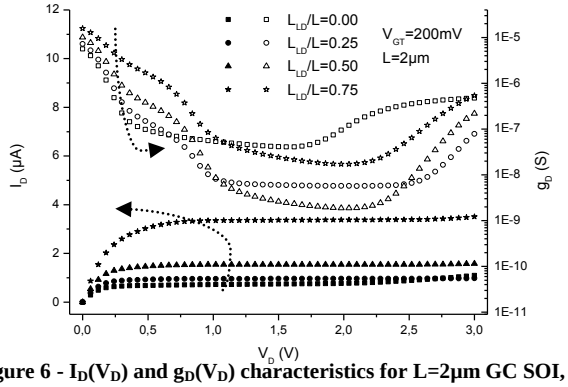

Figure 6 - $I_D(V_D)$ and $g_D(V_D)$ characteristics for L=2µm GC SOI, biased with V_{GT}=200mV.

We can see another good characteristic from the GC technology, which is the low effect of channel length modulation that reduced the variation of drain current with drain bias. This feature allows to state that the current I_D stays constant in saturation, lowering the output conductance, increasing the Early voltage, until the limit where the SCEs become important, in this case, L_{LD}/L=0.75.

Figure 7 presents the transconductance as a function of V_G for GC transistor with different L_{LD}/L relations and L=2µm. For low gate voltages, the increase in L_{LD}/L relation (smaller L_{eff}) causes a rise in the transconductance. However, from V_G=1.5V, it is verified that g_m is similar among the transistors. The reason is related to the electron concentration, when the V_G rises, the electron concentration increases in both regions. While at low V_G, the LD region presents higher electron concentration than HD one, for high V_G, both channel regions has similar electron concentration, that means, the GC transistor is behaving as a uniformly doped transistor.

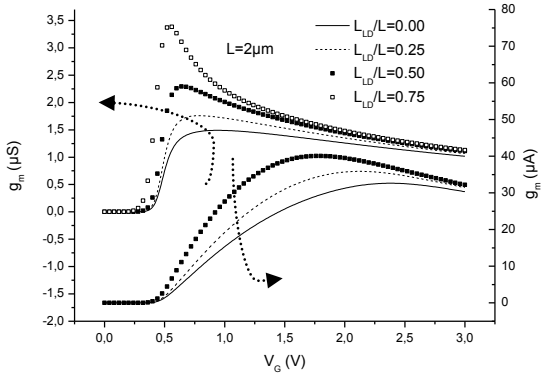

Figure 7 – Transconductance (V_D=50mV and V_D=1.5V) as a function of V_G for L=2µm GC SOI.

5. OPTIMIZATION OF L_{LD} FOR ANALOG APPLICATIONS

Due to these great characteristics for analog applications presented by GC transistor, simulations were performed to find the optimum L_{LD} to maximize the voltage gain and the breakdown voltage. Figures 8 and 9 show the transconductance and the output conductance, respectively, as a function of L_{LD} for different total channel lengths. Notice that the g_m and g_D raise for lower total channel length, but the increase of g_D is more significative, which causes a degradation in the voltage gain. When the L_{LD} increases, g_m rises as a consequence of reduction of L_{eff}, and g_D reduces due to the reduction of electric field provided by the LD region. This reduction is observed until the limit where SCEs occurs, when g_D starts to increase. According to this analysis, there is a specific L_{LD} which optimizes the voltage gain.

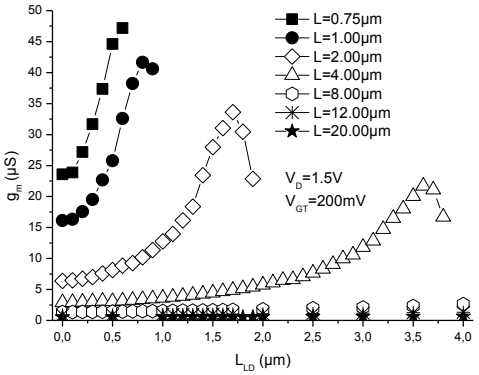

Figure 8 - Transconductance as a function of L_{LD}, extracted with V_D=1.5V and V_{GT}=200mV.

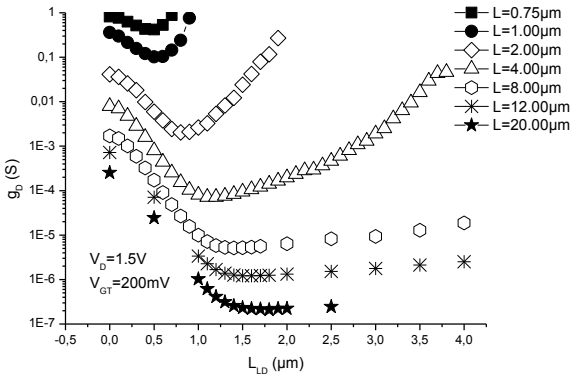

Figure 9 - Output conductance as a function of L_{LD}, extracted with V_D=1.5V and V_{GT}=200mV.

Figure 10 presents the voltage gain as a function of L_{LD}, extracted with V_{GT}=200mV and V_D=1.5V for different total channel lengths. Notice that there is an optimized L_{LD}, which allows larger voltage gain. Initially, the voltage gain rises with the increase of L_{LD}, but after a specific L_{LD}, A_V suffers a considerable reduction because of the short-channel effects. By Figure 10, it is verified that the L_{LD} optimized tends to saturate with the increase of the total channel length, being possible to state that L_{LD} around 1.2µm presents the maximum voltage gain for L>2µm.

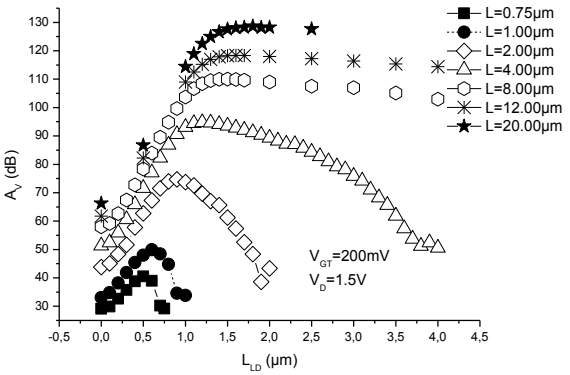

Figure 10 - Voltage gain as a function of L_{LD}, extracted with V_D=1.5V and V_{GT}=200mV.

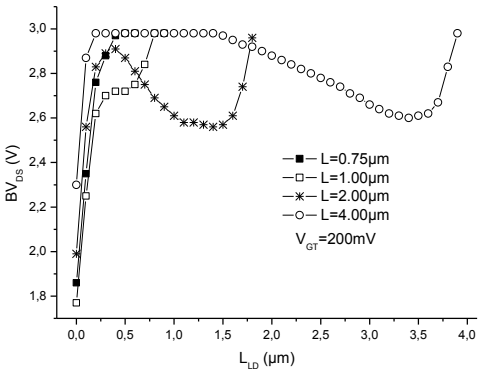

Figure 12 - Breakdown voltage as a function of L_{LD}, extracted with V_{GT}=200mV.

In Figure 11, it is presented the optimum L_{LD} as a function of the channel length for V_{GT}=200mV and V_{GT}=400mV. As we can see, the optimum L_{LD} rises with the increase of L, its behavior is not linear and the L_{LD} optimized is not constant even for equal channel lengths, but shows the same tendency for both V_{GT}.

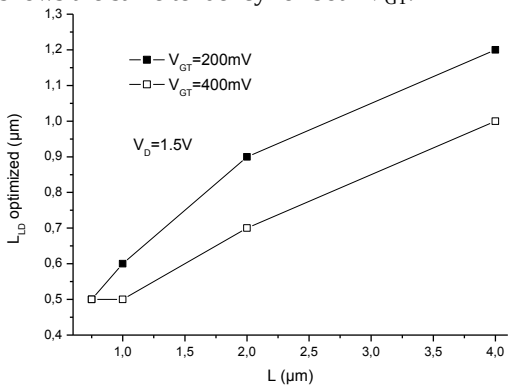

Figure 11 - Optimized length of the lightly doped region as a function of the channel length.

After analyzed the voltage gain, another important point for analog applications is the breakdown voltage, which results in larger output swing in analog circuits. The obtained results are showed in Figure 12. By plotting the breakdown voltage versus the L_{LD}, we can see that BV_{DS} also exhibits a maximum value for a given L_{LD} that means that there is also an optimized L_{LD} related to breakdown voltage.

The presence of a lightly doped region diminishes the electric field in the drain/channel junction, as mentioned before, but if the L_{LD}/L relation reaches a high value, the drain current increases, rising the impact ionization and, consequently, lowering BV_{DS}. When the channel is almost lightly doped, the breakdown voltage rises again, in reason of the low electron concentration which is not sufficient to initiate considerable impact ionization.

The transistors with total channel lengths equal to 0.75µm and 1µm presented only an increase with the rise of L_{LD} because they are in the limit of this technology, which is L=2µm.

6. CONCLUSIONS

In this work experimental and simulated results were used to investigate the influence of lightly doped region length on the analog characteristics of GC transistors. The simulations performed showed a great capability for the GC transistor concerning to applications in analog circuits because of the increase of voltage gain and the breakdown voltage.

Our studies demonstrate that there is an optimized L_{LD} for each transistor, as related to voltage gain as breakdown voltage, these parameters suffer an increase with the rise of L_{LD} until at a certain limit, in both cases the breakdown voltage and voltage gain tend to saturate for an specific L_{LD} optimized. For larger BV_{DS}, L_{LD} is near to 0.4µm and for larger A_V, L_{LD} is near to 1.2µm, varying a little for larger total channel length.

7. REFERENCES

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