Design of an 1.2V, 2.4GHz, LC-Tank Voltage-Controlled Oscillator

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ABSTRACT

This paper presents the design of an LC-Tank voltage-controlled oscillator (VCO), implemented in a standard 130 nm CMOS process. The proposed VCO operates within the spectrum defined in the standards Bluetooth and IEEE 802.11b and achieves phase noise as low as -104.62 dBc/Hz at 1 MHz offset from a 2.4 GHz carrier frenquency. The figure of merit (FOM) obtained, at 2.4 GHz, is around -167 dBc/Hz at 1 MHz offset. The power consumption is 3.6 mW.

Keywords

VCO, LC-Tank, CMOS.

1. INTRODUCTION

Voltage-Controlled Oscillator (VCO) is a functional block used in radio frequency (RF) communication systems. VCO in the Phase Locked Loop (PLL) generates a local oscillator signal that is used to transport the RF signal in the target frequency. For a good operation, some parameters must be taken into account, such as: phase noise, power consumption and, a wide frequency operation range [1].

In addition to the mentioned parameters, other features of the VCO must be observed, as gain, pushing, pulling and a figure of merit (FOM), which is a measure of its performance and is useful to compare a specific design to another one. The design of an LC (where L is the inductor and C is the capacitor) tank topology was chosen, in this work, since it has lower phase noise, regarding other classic topologies such as Colpitts and ring oscillators [2].

Still, in designing VCOs it is important to define to which standard must be specified. For the communication standards Bluetooth and IEEE 802.11b the spectrum is 2400 to 2483.5 MHz [3][4].

This paper is organized as follows: Section II talks about LC VCO basics, Section III describes the design of the proposed VCO, Section IV presents simulation results, Section V presents comparisons against other designs found in the literature and Section VI concludes this paper.

2. LC VCO BASICS

An LC VCO with negative resistance is depicted in Fig 1.

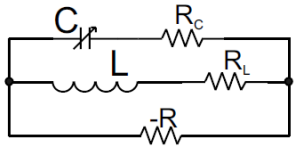

Fig. 1. LC VCO basic model [1].

The oscillator consists of an inductor L and a capacitor C in parallel, R_L and R_C represent inductor and capacitor losses respectively. The element -R is achieved by an active device, and is necessary to compensate for the losses [1]. The central angular frequency (ω_c) of this circuit is given by:

$$\omega_C = \frac{1}{\sqrt{LC}} \quad (1)$$

A classical way to implement the circuit in Fig. 1 is the well known LC CMOS (complementary metal-oxide-semiconductor) cross-coupled differential oscillator, shown in Fig. 2.

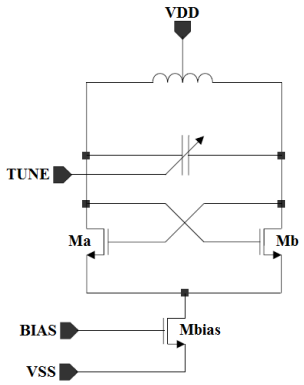

Fig. 2. LC-Tank cross-coupled differential topology [1].

According to Fig. 2 oscillating frequency is adjusted by the voltage (V_{TUNE}) applied to varactor C. The LC-tank losses are compensated by means of transistors Ma and Mb, biased by the current source Mbias. For this circuit the negative resistance (R) is given by

$$R = \frac{-2}{gm} \quad (2)$$

where *gm* is the transistor transconductance.

A real oscillator offers frequency fluctuations. These fluctuations are generally characterized by the single sideband noise spectral density normalized to the carrier signal ($\mathcal{L}_{TOTAL}$) and is defined as [1]

$$\mathcal{L}_{TOTAL}(f_C, \Delta f) = 10log\left[\frac{P_{SIDEBAND}(f_C+\Delta f,1Hz)}{P_{CARRIER}}\right] \quad (3)$$

where $P_{SIDEBAND}$ (fc + Δf,1Hz) denotes the single sideband power at the offset frequency Δf from the carrier f_C at a measurement bandwidth of 1Hz and $P_{CARRIER}$ is the carrier signal power at the carrier frequency fc.

To compare VCOs with different center frequencies, power consumption (P_{SUPPLY}), and phase noise over an offset frequency a figure of merit (FOM) is used [1]. A VCO with a more negative value or higher absolute value of the figure of merit is regarded to be better. One of the ways to determine the figure of merit of VCO is

$$FOM = \mathcal{L}(f_0, \Delta f) - 20log\left(\frac{f_0}{\Delta f}\right) + 10log\left(\frac{P_{SUPPLY}}{[mW]}\right) \quad (4)$$

where $\mathcal{L}(f_0,\mathbf{\Delta}f)$ is the single-side-band noise at the offset frequency **Δ**f from the carrier frequency f_0.

3. LC VCO DESIGN

The designed VCO is presented in the Fig. 3 and consists of two inductors (L_1 and L_2) connected in parallel with a capacitor (C_1) and two nMOS varactors (C_2 and C_3), in addiction to the cross-coupled pair (T_1 and T_2) biased by current mirror (T_3 and T_4). Vdd is the voltage reference and gnd is the ground reference.

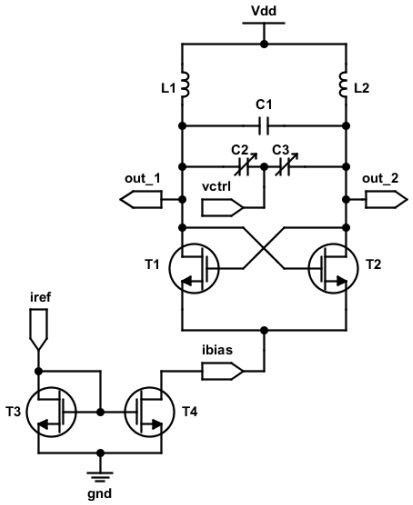

Fig. 3. VCO Designed.

LC-tank varactors capacitance changes as a function of the controlled voltage (V_{CTRL}) applied between C_2 and C_3, and consequently the oscillation frequency of the VCO varies within a given range. Still, the VCO output results from the difference between the outputs OUT_1 and OUT_2. The designed parameters of the circuit are shown in Table 1:

TABLE 1 – VCO PARAMETERS.

Parameter	Value	Unit
V_{DD}	1.2	V
i_{BIAS}	3	mA
i_{REF}	100	µA
L_1 e L_2	3.2	nH
C_1	465	fF
C_2 e C_3	117.4 to 593.9	fF
T_1 e T_2	W = 2.75 L = 0.12	µm
	5 fingers x (W = 0.55)	µm
	Multiplicity = 2	---
T_3	W = 0.6 L = 0.12	µm
T_4	W = 6.6 L = 0.12	µm
	12 fingers x (W =0.55)	µm
	Multiplicity = 4	---
A	40	---

In Table, A is the current mirror ratio, and the reference current (i_{REF}) is provided by the current source shown in Fig. 4.

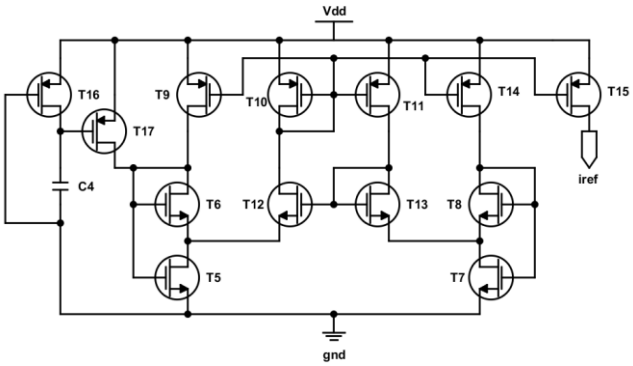

Fig. 4. Current source reference circuit.

This circuit is a SBCS (self-biased current source) and was designed according the work presented in [5]. It has two SCM (self-cascode MOSFET), one SBS (self- biased structure) circuit, and also a start-up circuit, this last based on [6].

In this circuit: T_5 and T_6 are the transistors of SCM 1 circuit; T_7 e T_8 are the transistors of SCM 2 circuit; T_{10}, T_{11}, T_{12} and T_{13} are the transistors of SBS circuit; T_9, T_{14}, T_{15} are the others transistors of SBCS circuit; T_{16} and T_{17} are the transistors of start-up circuit; C_4 is the capacitor of start-up circuit; Vdd is the voltage reference, gnd is the ground reference and i_{REF} is the out of current source reference.

4. RESULTS

The post-layout simulation results, obtained for the VCO are presented in Table 2:

TABLE 2 – VCO PERFORMANCE SUMMARY.

Parameter	Value	Unit
Power Supply	1.2	V
Central Frequency	2.45	GHz
Tunning Range	108	MHz
Phase Noise	-114	dBc/Hz@1 MHz
Power consumption	3.6	mW
Gain of VCO	252	MHz/V
Pushing	150	MHz/V
Area	647 x 274	μm^2
Temperature of operation	40	°C

From Table 2 it is observed that the VCO tuning range is about 108 MHz, and according to Fig. 5 the oscillation frequency range is from 2.396 to 2.504 GHz. At the range of 0 to 0.9 V the average gain is 252 MHz/V.

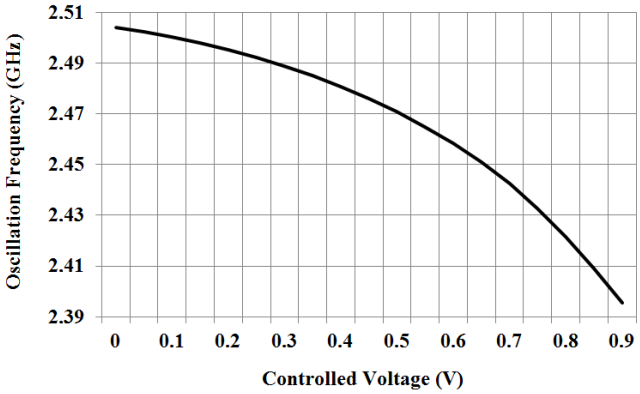

Fig. 5. Oscillation Frequency x Controlled Voltage.

Figure 6 shows the output power result obtained for controlled voltage range from 0 to 0.9 V. In this range the output power is between 13.294 and 15.195 dBm. For oscillation frequency of 2.4 GHz output power is 13.36 dBm and controlled voltage is 880 mV.

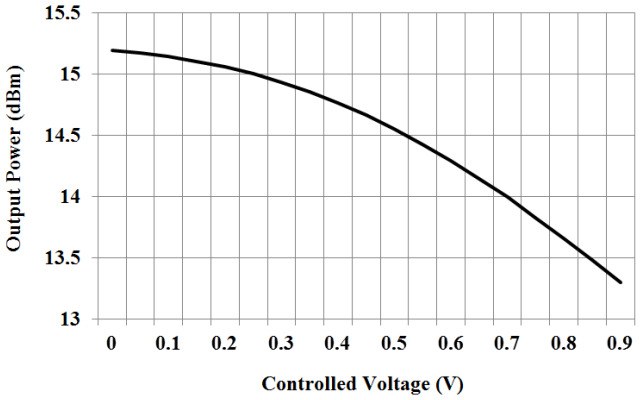

Fig. 6. Output Power x Controlled Voltage.

The phase noise for the frequency of 2.45 GHz is shown in Fig. 7, for the offset frequency of 1 MHz phase noise is -114 dBc/Hz:

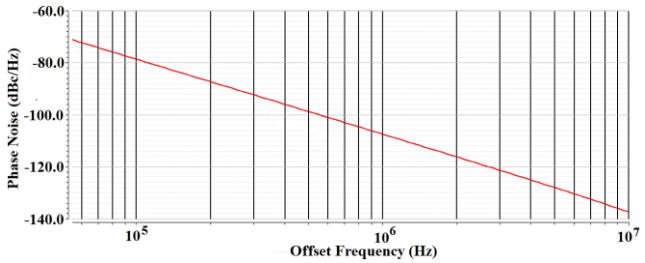

Fig. 7. Phase noise for the frequency of 2.45 GHz.

Figure 8 shows the layout of the VCO and according table II the area is 647x274 μm^2.

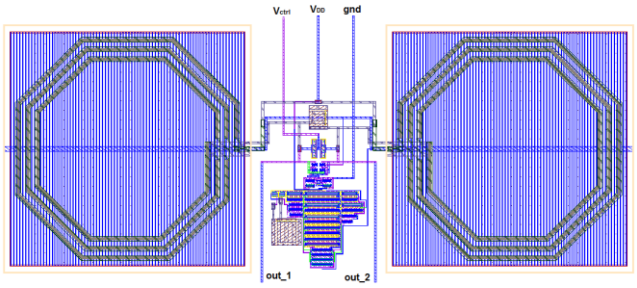

Fig. 8. Layout.of the proposed VCO.

5. DISCUSSION

The VCO designed was compared with other works as shown in Table 3:

TABLE 3 – VCO DESIGN COMPARISON WITH OTHER WORKS.

Work	f (GHz)	Tuning range	Tech (nm)	Process	Supply Voltage (V)	Power Cons. (mW)	ℒ@1M (dBc/Hz)	FOM (dBc/Hz)	Year
[7]	2.4	2.06 a 2.5 (440 MHz)	180	CMOS	1.0	2.6	-116.8	-180.25	2006
[8]	2.4	2.20 a 2.68 (480 MHz)	180	CMOS	1.8	7.2	-110.0	-169.03	2009
[9]	2.4	2.24 a 2.56 (320 MHz)	65	CMOS	1.2	0.799	-119.3	-187.88	2009
[10]	2.4	1.70 a 2.94 (1,24 GHz)	180	CMOS	1.8	15.12	-123.8	-179.61	2010
[11]	2.4	2.36 a 2.53 (170 MHz)	130	CMOS	0.5	0.06	-111	-190.82	2012
This work	**2.4**	**2.396 a 2.504 (108 MHz)**	**130**	**CMOS**	**1.2**	**3.6**	**-104.62**	**-166.66**	**2013**

The results of phase noise and FOM in this work present in Table 3 are related to the frequency of 2.4 GHz. Works used for comparison have the following common features, topology LC-tank, same frequency and same process. The works [7], [8] and [11] have the simulation results and works [9] and [10] have the measure results.

According to Table 3, this work presents a power consumption much larger than the obtained in work [11], that was also implemented in 130 nm, because the circuit proposed in work [11] is based on the current-reuse N-P-FET switching.

Although the tuning range of our VCO is less than the other works, it spans the spectrum defined in the standards Bluetooth and IEEE 802.11b.

The power consumption has an average value in relation to other works, the phase noise is slightly larger and because of this the FOM also presented a value. Thus, to decrease the phase noise, one of the ways would be to decrease the value of the parasitic capacitances of the circuit, as suggested in [1] for projects of low phase noise VCO. The bias circuit could be redesigned because it is one of the sources of noise.

The FOM can be improved also with the decrease in power consumption, either with a smaller supply voltage or with a smaller bias current.

6. CONCLUSION

The design of a LC VCO in a 130 nm CMOS process has been presented. This VCO achieves phase noise as low as -104.62 dBc/Hz at 1 MHz offset from a 2.4 GHz carrier frenquency and FOM obtained, at 2.4 GHz, is around -167 dBc/Hz at 1 MHz offset with 3.6 mW of power consumption.

Despite the present proposed VCO present phase noise and FOM a little larger than the other works, the tuning range is according to the standards Bluetooth and IEEE 802.11 b.

The VCO's performance can be improved by reducing the parasitic capacitances of the circuit by redesigned of bias circuit and with the decrease in power consumption. Since way, it is possible to obtain smaller values of phase noise and the FOM.

7. REFERENCES

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