Comparative Study of Threshold Voltage Extraction Methods applied to SOI nMOSFETs

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ABSTRACT
This paper shows a comparison between different extraction methods for the threshold voltage, analyzing the variation of this parameter with channel length and temperature for SOI nMOS transistors. The study has been carried out through two-dimensional numerical simulations and experimental measurements of fabricated devices. Threshold voltage was extracted using different methods reported in the literature, which are mainly based on drain current curves as a function of gate voltage at low drain bias.

Categories and Subject Descriptors
J.2 [**Physical Sciences and engineering**]: *electronics, engineering.*

General Terms
Measurement, Performance, Experimentation**.**

Keywords
Threshold voltage, parameter extraction, SOI MOSFET, temperature.

1. INTRODUCTION
SOI (Silicon-On-Insulator) technology was developed to minimize the effects of parasitic capacitances and suppress the parasitic thyristor of the CMOS structure. It consists in deploying a silicon oxide layer (buried oxide) between substrate and the active part of the transistor [1], as it is schematically shown in Fig. 1. On this figure, the thicknesses of the silicon layer (T_{Si}), gate oxide (T_{oxf}) and buried oxide (T_{oxb}) are indicated, as well as channel length (L) and the electrodes of gate (V_G), drain (V_D) and source (V_S).

Threshold voltage (V_{th}) is one of the most basic parameters of a MOS transistor and is defined as the minimum required voltage applied on the gate to have a formation of an inversion layer composed by minority carriers, which connects source and drain regions, allowing current to flow between these two terminals. The depletion region caused by the application of a positive gate voltage (V_G) in a nMOSFET devices is given by equation (1).

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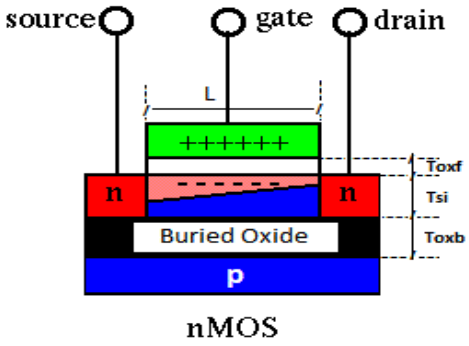

Figure 1 - Transistor SOI nMOSFET.

$$d = \sqrt{\frac{2\varepsilon si \,.2\phi F}{q\,.NA}} \quad (1)$$

After reaching its maximum depth, further increase of gate voltage makes minority carriers to move from substrate and form a channel that will connect drain and source terminals. For nMOSFET transistors built on bulk Si wafers, threshold voltage is expressed by equation (2).

$$V_{th} = V_{fb} + 2\phi F + \frac{q.NA\,.\,xdmax}{Cox} \quad (2)$$

where V_{fb} is the flat band voltage, expressed by $V_{fb} = \phi_{ms} - Q_{ox} / C_{ox}$, q is the elementary electric charge, ϕ_{ms} is the work function difference between the metal and semiconductor, Q_{ox} is the oxide fixed charge density per unit area and C_{ox} is the oxide capacitance per unit of area, N_A is the acceptor impurity concentration and ε_{Si} is the permissivity of Si.

There are several methods to extract the threshold voltage of a MOS transistor [2, 3]. On this work, five methods will be compared: Constant-Current (DC), Linear Extrapolation (LE), Second-Derivative (SD), Current-to-square-root-of-the-Transconductance Ratio (CsrTR) and Transconductance-to-Current-Ratio (TCR) Methods [3]. The selected methods will be applied to extract the value of Vth from the simulated and measured transfer characteristics of a SOI nMOSFETs with different channel lengths and under a wide ranges of temperatures, in order to compare them.

2. TEMPERATURE EFECT ON V_{TH}
In a semiconductor material, there is a rate of ionization for dopants according to the applied temperature (T). When temperature starts to become lower, thermal energy is not enough to ionize dopants throughout the material [4]. Fermi potential (ϕ_F) depends of temperature and ionizing rate, and increases substantially with temperature decreasing. Also, interface traps

can affect threshold voltage at low temperature. Therefore, threshold voltage as a function of temperature is given by Equation (3) [5].

$$Vth = \phi ms - \frac{Qox}{Cox} + \frac{q.Nitf.\phi F}{Cox} - \frac{Qdepl}{Cox} + 2\phi F \quad (3)$$

On conventional or partially depleted MOS devices, charge density of the depletion (Q_{depl}) is given by $Q_{depl} = - q.N_A.x_{dmax}$. In this case the rate dV_{th}/dT can be expressed by equation (4), where $\alpha_{VT} = 1$.

$$\frac{dV_{th}}{dT} = \frac{d_{\phi F}}{dT}\left[1 + \alpha_{V_T}\frac{q}{C_{ox}}\left(\frac{\varepsilon_{SiN_A}}{kTln(N_A/n_i)}\right)^{\frac{1}{2}} + \frac{qN_{itf}}{C_{ox}}\right] \quad (4)$$

For fully depleted devices $\alpha_{VT} = 0$, only if V_{th} is independent of the depth of the depletion layer, and becomes a function of the thickness of the silicon layer, thus depletion is negligible.

3. TWO-DIMENSIONAL NUMERICAL SIMULATIONS

Two-dimensional numerical simulations were performed with ATLAS software [6]. The models employed for the simulation of physical effects consider band gap narrowing, incomplete ionization of impurities, mobility dependence on the temperature, doping concentration and electric field.

The simulated devices are FD SOI nMOSFET with gate oxide thickness (T_{oxf}) of 31nm and buried oxide thickness (T_{oxb}) of 400 nm, silicon layer (T_{Si}) of 80 nm, doping concentration in the channel region (N_A) of $6\times10^{16}cm^{-3}$ and polysilicon as gate material.

3.1 Variation of the channel length

Setting T=300 K and the channel width (W) by 1 µm, channel length varied between 0.5 µm and 10 µm. Drain current as a function of the gate voltage at drain bias of 50 mV was simulated. The values of V_{th} were obtained using the five methods mentioned in section 1, and are shown in Fig. 2.

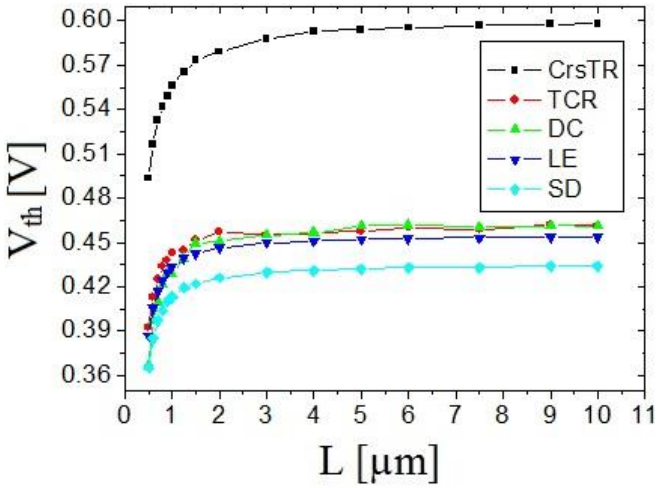

Figure 2 - Comparison of threshold voltage values as a function of channel length extracted using five different methods in the temperature of 300 K.

It can be noted that on channel lengths larger than 4 µm, V_{th} remains constant, although the differing values for each method. For CrsTR method, devices with channel lengths below 4 µm, the threshold voltage begins to decrease indicating the occurrence of short channel effects [4]. For other methods that is only observed for L < 2 µm. This effect occurs when the transistor channel length is very short, such that the control of depletion charges in the channel is not fully realized by the gate electrode, but also the junctions drain/channel and source/channel [4]. Furthermore, it is noted that the value of threshold voltage is strongly dependent on the extraction method used, as shown in Figure 2. For values obtained through CsrTR method there is a larger displacement in comparison to others methods, because data are obtained in the region of strong inversion. Another factor found was the similarity of the curves of TCR, LE and DC methods, which presented very close values in almost all simulated lengths.

For long channel transistors, the highest value of V_{th} was found in CsrTR method (0.598 V) and the lowest value for SD method (0.434 V). The same tendency is found with the shortest simulated length (0.5 µm), with V_{th}= 0.493 V for CsrTR method and V_{th}= 0.365 V for SD method, although the difference between obtained values with different methods is reduced with channel shortening.

3.2 Variation of Temperature

Transistors with L=1 µm and 4 µm, W=1µm operating in temperatures ranging between 100 K and 400 K were simulated. The extracted results for V_{th} as a function of temperature are shown in Fig.3. From this figure, one can see a variation of the slope of V_{th} x T characteristic, depending on the method used. The extracted dV_{th}/dT is presented in Table 1.

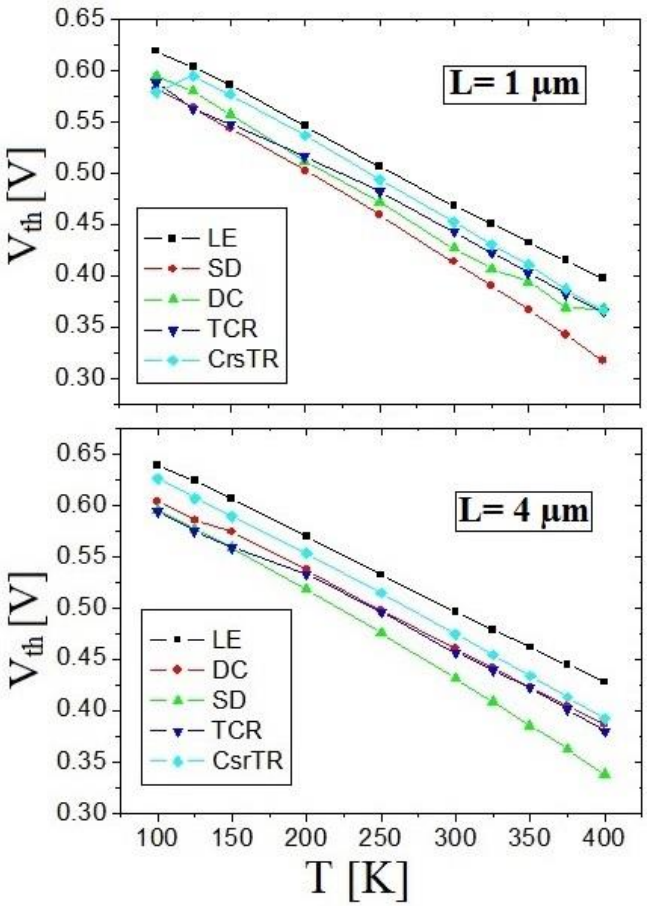

Figure 3 - Comparison of 5 methods studied with L=1µm and 4 µm.

Using equation (4), dV_{th}/dT results in $6.46x10^{-4}$ V/K, considering $N_{itf} = 0$. Comparing this value to those presented in Table 1, we find that TCR method was the closest one to the theoretical value in both channel lengths.

Table 1 – Simulated dV_{th}/dT slopes obtained with different extraction methods.

METHOD	dV_{th}/dT [V/K]	
	L= 1 µm	L= 4 µm
DC	$8.043\ 10^{-4}$	$7.323\ 10^{-4}$
CsrTR	7.52310^{-4}	$7.148\ 10^{-4}$
LE	$8.813\ 10^{-4}$	$8.591\ 10^{-4}$
SD	$7.777\ 10^{-4}$	$7.781\ 10^{-4}$
TCR	$7.321\ 10^{-4}$	$7.023\ 10^{-4}$

4. EXPERIMENTAL RESULTS AND DISCUSSION

The devices measured were fabricated by UCLouvain, Belgium [7], with L of 0.75µm, 1µm, 1.5µm, 2µm, 3µm, 4µm, 5µm, 8µm and 10µm, and W=20µm. The other technological characteristics were the same used in the simulations.

4.1 Variation of channel length

Room temperature data was measured using the Keithley 4200 SCS semiconductor parameter analyzer along with a Cascade MicrotechmicroproREL 3600. In Figure 4 values of V_{th} are presented using the five selected methods.

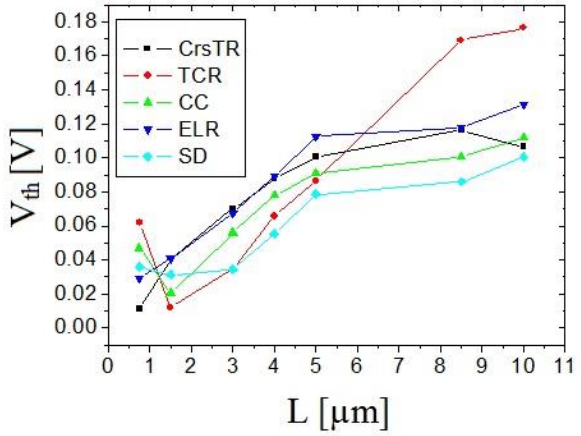

Figure 4 - Change the channel length (L) with fixed temperature at 300 K, V_D = 50 mV.

One can note that channels smaller than 5µm there was a decrease in the values of the threshold voltage due to the short channel effect, which reduces the control of gate terminal (V_G) on the channel between source and drain [4], as it was already seen in the simulate data. TCR method shows an irregularity compared to other presented methods, since this method based on the maximum value of gm /I_D ratio, obtained at very low values of V_G, and hence, very susceptible to any leakage current that may occur.

On long channel transistors, the highest value of V_{th} was found in TCR method of 176 mV, and the lowest for SD method, was 100mV. For the smaller length measured (L=0.75 µm) the highest value of V_{th} was found in TCR method of 62mV and the lowest for CsrTR method 10.8mV.

4.2 Variation of temperature

For the variation of temperature, devices with L=0.75µm, 1µm and 2µm under operating temperatures ranging between 90K and 380K were measured. Data were extracted using variable temperature Micro Probe System, Model K20, from MMR Technologies.

The extracted results for the threshold voltage are presented in Figure 5.

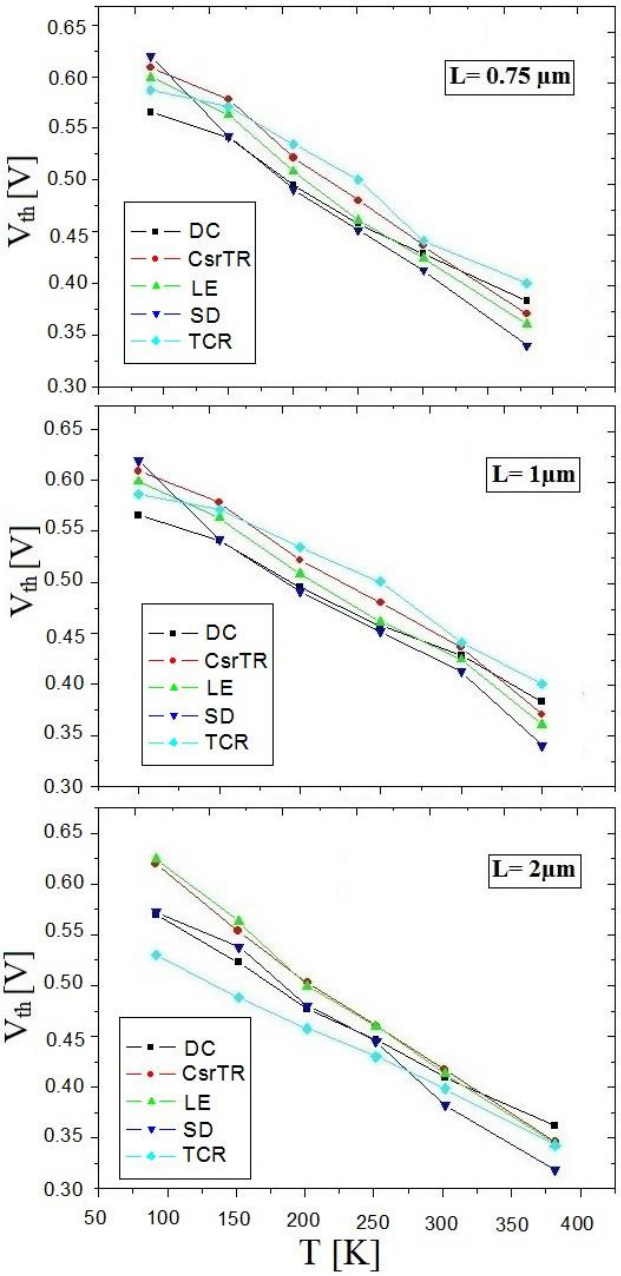

Figure 5 - Variation of the temperature (T) for L = 0.75µm, 1µm, 2µm and V_D = 50 mV.

Table 2 presents the values of the slope coefficients extracted from figures 5. According to Figure 5 and Table 2, we see that the TCR method suffered a slight variation of dV_{th}/dT in relation to

other applied methods, showing that temperature dependence is not the same for all methods.

From Table 2, it is seen that the highest dV_{th}/dT coefficient was found for the SD method with L = 0.75µm and the lowest rate was on TCR method with L = 2µm. As mentioned before, using equation (4) and the technological parameters, dV_{th} / dT is $6.46364x10^{-4}$ V/K, considering $N_{itf} = 0$. Comparing with the table below we find that LE method was the closest one among the presented values.

Table 2–Experimental dV_{th}/dT slopes obtained with different extraction methods.

METHOD	dV_{th}/dT [V/K]		
	L= 0.75 µm	**L= 1 µm**	**L= 2 µm**
DC	$6.573\ 10^{-4}$	$7.143\ 10^{-4}$	$7.205\ 10^{-4}$
CsrTR	$8.488\ 10^{-4}$	$9.112\ 10^{-4}$	$9.327\ 10^{-4}$
LE	$8.461\ 10^{-4}$	$8.978\ 10^{-4}$	$9.668\ 10^{-4}$
SD	$9.357\ 10^{-4}$	$9.012\ 10^{-4}$	$9.075\ 10^{-4}$
TCR	$6.928\ 10^{-4}$	$6.303\ 10^{-4}$	$6.341\ 10^{-4}$

5. CONCLUSIONS

This work presented the influence of threshold voltage extraction method on nMOSFET at different temperatures and channel lengths. Simulated and experimental results showed that the reduction of threshold voltage due to short channel effect and its variation with temperature is strongly dependent on the selected method.

6. ACKNOWLEDGMENTS

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