Design of a telescopic operational amplifier using a semi-automatic synthesis

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ABSTRACT
This paper presents a semi-automatic design methodology for operational amplifiers including multi design stages containing electrical simulations and manual adjustments. The methodology is based on the joint use of traditional manual design and some rounds of simulations performed by UCAF automatic synthesis tool. We applied the proposed methodology for the design of a telescopic operational amplifier in 0.18 µm technology and compared the resulting specifications with a manual design. The semi-automatic synthesis proved to be very useful for this topology for designing operational amplifiers.

Keywords
Analog Design; Telescopic Amplifier; UCAF tool.

1. INTRODUCTION
Due to the ever-increasing complexity in the field of analog integrated circuit design, there is the need of CAD tools that help designers to size circuits and to achieve satisfactory results in a reasonable design time.

The large number of free variables turns the design of a small building block such as an operational amplifier a very complex task.

Due to the lack of tools for automatic synthesis of operational amplifiers available in the market, the manual design of operational amplifiers is still in use. It is based on the designer experience in order to explore the design space for sizing the transistors. However, it involves a huge amount of difficulty in dealing a high number of free variables (W / L's and bias voltage) and design specifications. Each transistor has a number of degrees of freedom related to their physical characteristics (gate width and length) and a manual design requires a lot of time and skill to scale these variables aiming at the highest possible efficiency.

Some works have already described the design of a telescopic amplifier, both aiming easier to design the circuit with a high level of efficiency [1][11][12].

The telescopic amplifier is formed by some current mirrors with input bias voltage, pair of differential input voltage and has cascode structure.

Some designers contribute to the development of operational amplifiers bringing new design methodologies such as the bias of the transistors of the current mirrors [6], using common- mode feedback (CMFB) implementation techniques [9] adding PMOS differential pairs among others [10]. If both designers were using automatic synthesis tools, these would save time and would get more accurate results when compared with a design done manually.

This paper describes the design of a telescopic amplifier having already done a project as reference [3] adopted a semi-automatic methodology using the tool for automatic synthesis UCAF [5].This tool models the sizing as an optimization problem and performs a series of perturbation on the free variables, exploring the design space by means of a given optimization heuristic. Also, it executes a series of electrical simulation for verifying the convergence and quality of the results.

A methodology for a semi-automatic design of a telescopic amplifier is presented. It is based on an automatic synthesis followed by a small manual design - allowing the designer to make some empirical adjustments - and a final automatic synthesis.

This methodology proved to be effective and the obtained operational amplifier has good characteristics in terms of power consumption, area and stability, when compared to a hand-made reference amplifier.

The remaining of this paper is organized as follows: Section II describes the design methodology; Section III describes the design of a telescopic amplifier with the results and Section IV present conclusions.

2. DESIGN METHODOLOGY
The goal of this work is to design a telescopic amplifier using the UCAF automatic analog synthesis tool and to verify if the obtained results are better than a traditional manual design.

The main idea is to gradually reduce the size of the design space making the implementation faster and accurate.

The design methodology is divided in 3 steps. First, an automatic synthesis procedure is performed for the full range of values for the variables. It implies on executing the automatic synthesis with the UCAF tool with a complete set of design parameters and with a large variability range for the free variables. The convergence for the required circuit specifications is very difficult, since the exploration of the large design space in a reasonable processing time is unpractical. So, the automatic tool is configured to finish

the exploration with a relaxed stop condition. The resulting sized circuit is expected to present electrical characteristics close the desired specifications, but still not acceptable. The second step is a manual adjustment of the circuit variables, given as reference the circuit generated by the first design step. It implies a few verifications by electrical simulations and small perturbations in the transistors sizes and bias voltages and currents. Again, the resulting sized circuit does not need to achieve all desired specifications. The purpose of this step is to correct any possible bad feature, which cannot be observed in the first step of the design. The third and final design step is another automatic optimization with the UCAF tool, but now having as initial solution the sized circuit previously obtained. Also, the range of the free variables is reduced in order to limit the design space and to efficiently explore it in the search for an optimized solution.

The following subsections present the configuration of the UCAF tool and details about each proposed design step.

2.1 UCAF Tool

UCAF is a tool for automatic synthesis of analog building blocks based on non-linear optimization algorithms. It was developed in Matlab ® environment and it interacts with HSPICE for circuit verification by means of electrical simulations. It uses optimization heuristics such as Genetic Algorithm (GA) or Simulated Annealing (SA) in order to efficiently explore the design space and to find optimal solutions that meet certain required user specifications.

The main purpose of this tool is to efficiently explore the design space in order to reduce the search time in sizing the transistors. Also, it optimizes some circuit specifications, such as power dissipation or silicon area [5].

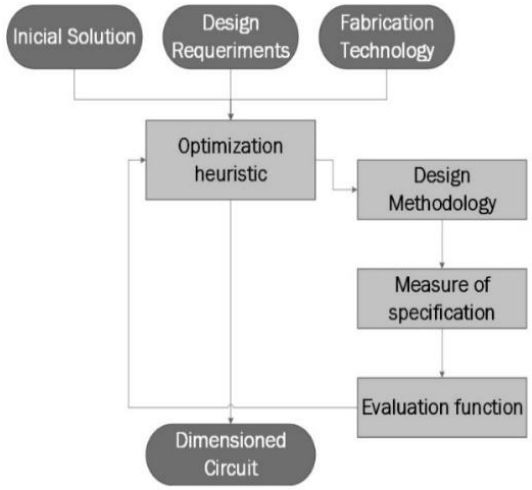

Figure 1: Block diagram of the UCAF framework

Fig. 1 describes the UCAF design flow. The block containing the heuristic optimization receive inputs such as an initial solution, the desired design specifications and the desired technology parameters. The electrical simulation for evaluating the sized circuit is performed by a SPICE simulator.

With the values of the circuit specifications, it is possible to evaluate the circuit using a cost function, which relates, for example, area and dissipated power. This procedure is performed repeatedly until finding a solution that minimizes the cost function. This is the optimal solution for the circuit. [5].

2.2 Step I – Automatic Design

In the first design step, the UCAF tool is configured to perform a full search of the design space. The circuit netlist and technology parameters are the inputs, followed by the information about the free variables and the desired circuit specifications and constraints. The range of free variables values is set to be large, in order to guarantee that the optimization algorithm will explore all regions of the design space. For example, the range of variation for all gate widths can be from 0.22 µm to 50µm, with a step of 0.05µm, and for all gate lengths can be from 0.18µm to 10µm, with the same step. For 4 different gate widths and 4 different gate lengths, this generates a design space with 1.46×10^{21} possible solutions.

The initial solution is set to be random, since in this first step it is difficult to estimate a good guess.

The optimization stop condition can be a given maximum number of iterations or a maximum processing time.

2.3 Step II – Manual Adjustment

Giving as reference the solution generated in the first design step, a manual adjustment can be made. This design step demands a certain designer skill, but in a very lower degree when compared to a full manual design.

For the CMOS transistors to obtain the saturation condition, the values of the DC voltages that govern the behavior of the transistor should obey the following equation:

$$V_{ds} \geq V_{gs} - V_t \tag{1}$$

The drain current I_{ds} of all devices can be estimated by (2) for saturation region [4][7]. This is a simplified equation that models the relation between terminal voltages and drain current of a CMOS transistor.

$$I_{ds} = \frac{k(V_{gs}-V_t)^2 W}{2L} \tag{2}$$

The constant k is fixed by the fabrication technology and it is related to the material forming the transistor. Thus, isolating W/L and defining the current value and V_{gs} considering (2) – it is possible to estimate the aspect ratio of all transistors[8].

With the sized values of W/L for all transistors the verification of electrical characteristics can be performed by SPICE simulation, block by block, until all transistors are saturated. Small-signal parameters (*gm* and *gds*) also need to be monitored.

2.4 Step III – Automatic Refinement

The last design step is a refinement of the previously generated circuit in order to optimize some electrical characteristic. In this round, the values of W / L calculated manually in the second design step will serve to constrain the limits of the free variables. The UCAF tool is configured to explore a sub-region of the design space determined by the initial solution (the circuit

generated by the second design step) and its immediate neighborhood. For example, if the width of a transistor was set to 1um in the previous design step, its variability range can be limited from 0.5µm to 2µm. This reduces drastically the design space and the optimization algorithms can easily perform a search for an optimal solution.

3. DESIGN TELESCOPIC AMPLIFIER

Telescopic amplifiers are widely used due to its compact structure, high swing, high voltage gain and efficiency [3].

The resulting degradation in differential gain, *common-mode rejection ratio* (CMRR), and other amplifier characteristics are compensated by applying regulated cascode differential gain enhancement and a replica-tail feedback technique [2].

The telescopic amplifier is biased by a pair of differential input voltage (V_{in} + and V_{in} -), an output voltage (V_{out}) and their inputs to supply voltage V_{dd} (+) and V_{ss} (-). Also, there are two bias voltages, V_{cp} and V_{cn}.

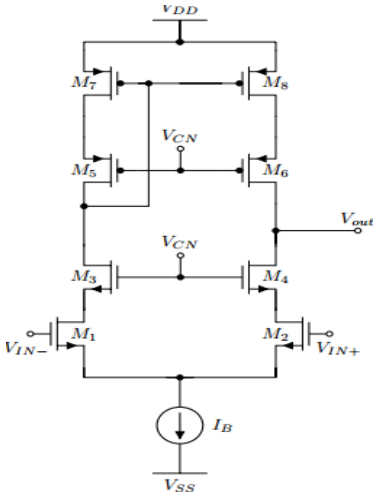

Figure 2: Schematics of the telescopic amplifier.

The design was implemented in 0.18µm CMOS technology.

The manual design was performed by adopting a current I_{BIAS} = 50 µA, V_{dd} =-V_{ss} = 0.9 V, V_{cp} = 0V and V_{cn} = 0.5 V.

One of the characteristics of the telescopic amplifier is its current mirrors. The amplifier can be splitted into four blocks of transistors, each one being formed by a pair that should be equally sized.

The supply voltage of the amplifier is 1.8 V. This voltage must be divided among the transistors so that it satisfies Eq. 1.

In the first round of simulations, the amplifier was inserted into the UCAF tool having as design constraints values similar to the characteristics of a reference amplifier described by [3]. A manual design allows some empirical adjustments. However, not all specifications were met. Then a third round of automated synthesis based on results of manual design constrain the limits allowed for W and L. After this step, all desired specifications were achieved.

The Bode plots for a better view of gain and phase margin of the amplifier after steps 1, 2 and 3 are depicted in figures fig. 3, fig. 4 and fig.5, respectively.

Table 1 shows the specifications, transistors sizes, and voltage and current sources values for the sized amplifier for each design step and the reference amplifier.

All specifications are better than the reference amplifier, with exception to GBW, which does not compromise the results.

Table 1 : Electrical characteristics and sizes of transistor for the telescopic amplifier in each design step.

Parameters	Reference amplifier [3]	Telescopic Amplifier UCAF Step I	Telescopic amplifier Manual Step II	Telescopic amplifier refinement Step III
W1 (μm)	*	21.4	31.77	32.38
L1 (μm)	*	3.04	0.7	0.485
W2 (μm)	*	18.07	7.28	7.84
L2 (μm)	*	0.61	0.35	0.741
W3 (μm)	*	46.75	5.36	3.99
L3 (μm)	*	4.49	0.3	0.791
W4 (μm)	*	47.55	15.54	15.81
L4 (μm)	*	0.28	0.6	0.4434
V_{cp} (V)	0	-0.14	0	-0.445
V_{cn} (V)	0.5	0.89	0.5	0,461
I_B (μA)	50	13.68	50	30.96
Power (μW)	90	24.63	90	55.728
Gain (dB)	60.5	41.25	84.22	84.89
Phase margin (°)	81	69	76	105
GBW(MHz)	65	58.8	56.234	47.18
CMRR (1kHz)	106.3	156.54	*	112

* Not available.

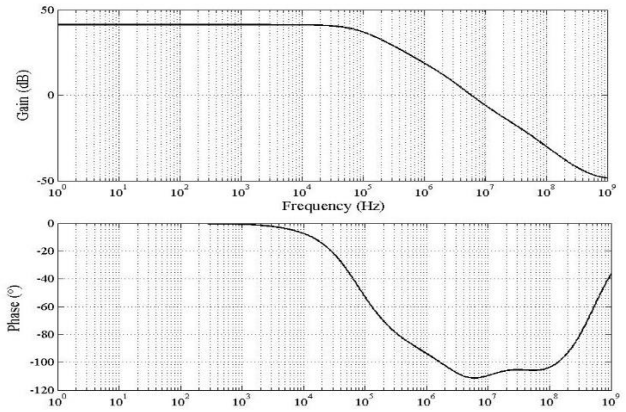

Figure 3 : Bode diagram for amplifier designed in the first phase.

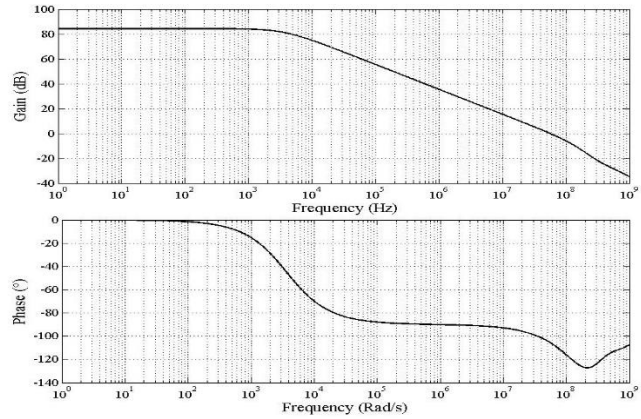

Figure 4: Bode diagram for amplifier designed in the second phase.

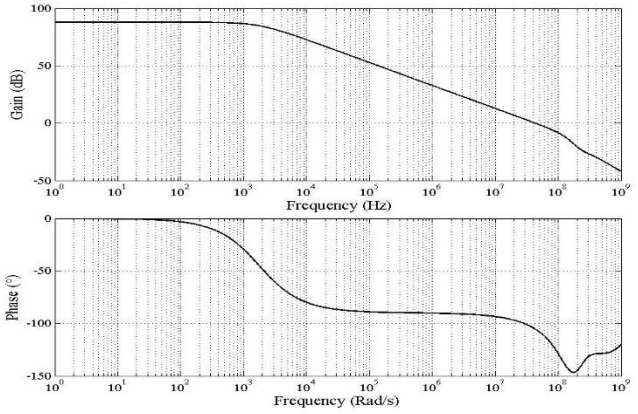

Figure 5: Bode diagram for amplifier designed in the third phase.

4. CONCLUSION

The proposed design methodology proved to be possible generated sized operational amplifiers with better electrical characteristics than a manual design.

The application of the methodology generated a telescopic amplifier with high gain and low power consumption when compared to a traditional manual design. In the first design setup, the generated amplifier obtained a near satisfactory result, but not for all specifications.

With the manual adjustment (second step), it was possible to refine some characteristics and generate a new sized circuit that was used as the initial value for the UCAF tool. The design space was reduced by constraining the variation range of the free variables. So, the last design step generated an amplifier with high gain and low power consumption when compared with the reference, in an acceptable processing time.

All these data the improvement obtained with this methodology are shown in Table 1 formed by the results of the design steps. Bode diagrams that were used together with the values tabulated for comparison of the results in each step of the project were also for better viewing, plotted.

Thus, we can conclude that the telescopic amplifier generated served to refine the UCAF tool, exploring efficiently the design space in the search for optimal solutions with advantages such as reduced complexity of design and quality results.

5. ACKNOWLEDGMENTS

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