3D Transistor Behavior from Room to Low Temperature

Carlos Augusto Bergfeld Mori[1], João Antonio Martino[1], Paula Ghedini Der Agopian [1,2]

[1]Laboratório de Sistemas Integráveis, Universidade de São Paulo, Brazil

[2]Centro Universitário da FEI, S.B. do Campo, Brazil

e-mail: carlos.mori@usp.br

ABSTRACT

This paper shows the main electrical characteristics behavior of a 3D transistor from room to low temperature (100K). This work was carried out by numerical simulation. When the temperature decreases, it was observed an improvement on maximum transconductance thanks to the carrier mobility increase. The subthreshold swing becomes steeper (better) and consequently the Ion/Ioff also increase. The threshold voltage increases due to the Fermi level. It was also observed a ZTC (Zero temperature coefficient) where the drain current does not change as a function of temperature. This bias condition can be useful for some special low voltage circuits.

Keywords

Silicon-On-Insulator (SOI), multiple-gate devices (MuGFET), low temperature

1. INTRODUCTION

With the advance of technology, all electronic components must scale down, in order to increase components density in ICs, and therefore increase the performance of the devices where they are used. Nowadays, almost all electronic circuits are based on MOSFET technology; however, as it is scaled down, some undesired effects start to take place, such as the short channel effects (SCE), rendering the device almost useless, since it is impossible to properly control it [1]. One solution presented to solve this problem are the multiple gate MOSFET (MuGFET) devices, which greatly improve the control over the channel region, even as the devices are reduced [2]. Particularly, Intel is already using devices known as 3D transistors (also known as triple-gate FinFETs or MuGFETs devices), as for example the Ivy Bridge device, first announced on May 4, 2011 [3].

During the last years, the importance of studying electronic circuits at low temperatures has grown, mainly due to space and cryogenics applications. A simple example that is of great relevance nowadays is the Magnetic Resonance Image, which requires superconductor magnets, and therefore extremely low temperatures to function properly [4].

The aim of this work is to better understand the basic parameters behavior of 3D transistors at low temperatures. In order to do so, the Atlas simulator from Silvaco was used.

2. DEVICE'S CHARACTERISTICS

In this study, the device was simulated using Atlas simulator from Silvaco. The used n-channel FinFET has the following characteristics: channel length (L) of 150nm, fin width (W_{FIN}) of 20nm, fin height (H) of 65nm, gate oxide (t_{oxf}) and buried oxide thicknesses of 2nm and 145nm respectively. The software Atlas was used to simulate this device, considering only a two-dimensional approximation, as the one represented in red on the figure below:

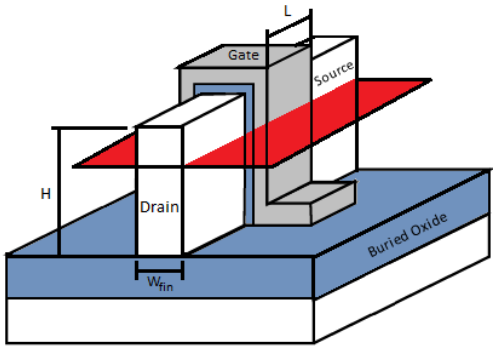

Figure 1. 3D transistor structure.

Besides the traditional channel, source and drain doping, a structure called Lightly Doped Drain (LDD) was also employed, in order to help improve the device's performance. As the name suggests, an additional and weaker doping is considered between channel and drain. The following values were used: 10^{15} atoms/cm² p-type dopant for the channel, 10^{18} atoms/cm² n-type dopant for the LDD, and 10^{20} atoms/cm² n-type dopant for source and drain.

3. RESULTS AND ANALYSIS

Figure 2 shows the drain current (I_{DS}) as a function of the gate voltage (V_{GS}) at drain bias of 50mV, varying the temperature from room temperature down to 100K.

As temperature decreases, it is expected an increase in the carriers mobility (in this case, electrons), since the doping is relatively low, resulting in a greater influence of the lattice scattering (which increases mobility with the decrease of temperature), than of the impurity scattering (which decreases mobility with the decrease of temperature). Therefore, above the threshold voltage, where the predominant conduction mechanism is carrier drift, as temperature reduces, the current drive increases [5].

This relation between gate voltage and drain current is shown in Figure 2.

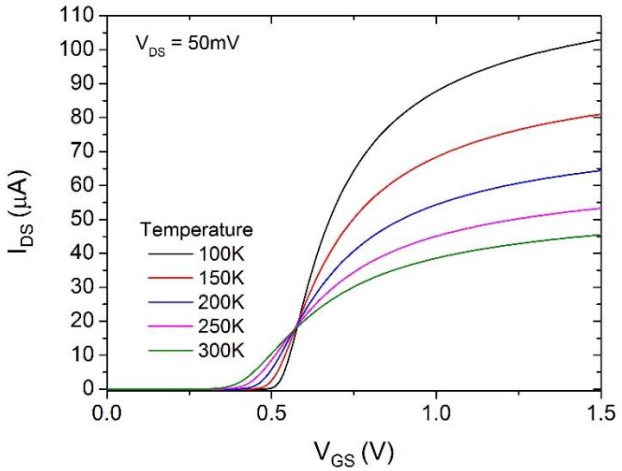

Figure 2. Drain current vs gate voltage for different temperatures

Since the current in subthreshold voltages increases exponentially, it is interesting to use a logarithmic plot to observe the conduction in this region, as can be seen on Figure 3:

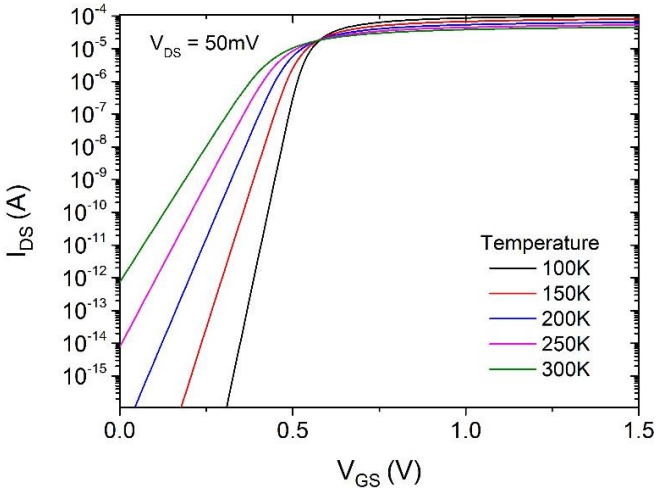

Figure 3. Drain current vs gate voltage

In this case, the predominant conduction mechanism is carrier diffusion from source to drain, which depends on the thermal energy. For that reason, as the temperature is reduced, there are less energetic electrons, so there is a smaller current drive. There is also a direct relation between the temperature and the inverse subthreshold slope (usually referred just as subthreshold slope, or SS): as the temperature lowers, so does the slope.

Finally, close to the threshold voltage, there is a point where both effects previously mentioned compensate each other, creating an intersection between all curves, practically independent of temperature. This point is known as Zero-Temperature-Coefficient (ZTC), and is a critical parameter to design circuits that are expected to suffer great temperature variations, since devices biased around this point present almost no change in their currents as the temperature is modified.

To evaluate this device's inverse subthreshold slope as temperature sinks, the curves illustrated in Figure 4 are used.

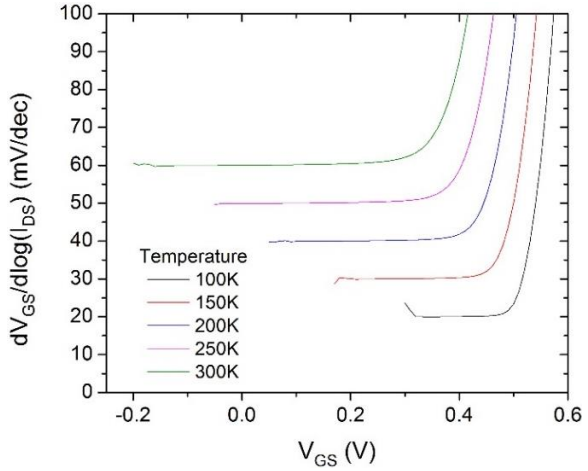

Figure 4. Curves used for extracting the subthreshold slope as the point observed in the planar region.

The graph above comes straight from the equation (1).

$$SS = \frac{dV_{GS}}{d(\log I_{DS})} \quad (1)$$

The value for each temperature is the constant part in the beginning of the curves (since the derivative of a linear curve is a constant). In the following crescent part, the device is already entering its normal conduction region, and therefore this part is not relevant for the subthreshold slope.

It can be demonstrated that, if interface traps and the effect of internal capacitances are neglected, SS can be obtained by equation (2).

$$SS \cong \frac{kT}{q}\ln(10) \quad (2)$$

Where k is the Boltzmann constant, q is the fundamental charge and T is the temperature. This equation indicates a linear relation between temperature and the slope, and actually presents a theoretical limit for the value of SS (~60mV/dec at room temperature), since it is the ideal case, with no parasitic effects.

In order to better observe the values of the subthreshold slope as the temperature decreases, the graph in Figure 5 is presented.

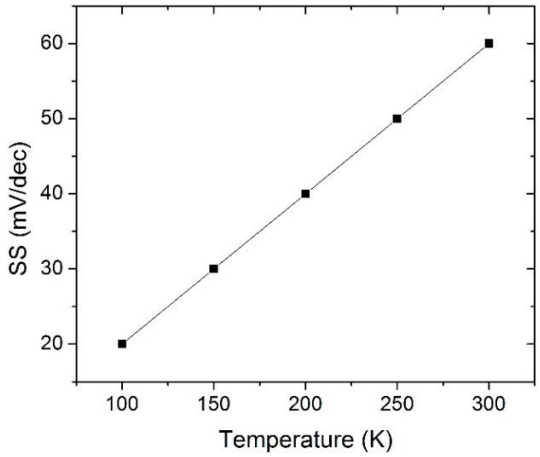

Figure 5. Subthreshold slope vs temperature

It can be immediately noticed that the curve simulated is practically identical to the one expected in the ideal case, starting at 60mV/dec at room temperature, and falling approximately 20mV/dec for every 100K. Such behavior may be explained through a very low internal capacitance and a strong electrostatic coupling, since the width of the fin is rather small, when compared to the other dimensions.

The threshold voltage may be extracted from the maximum of the second derivative of the $I_{DS}xV_{GS}$ curve, as the one shown on Figure 6.

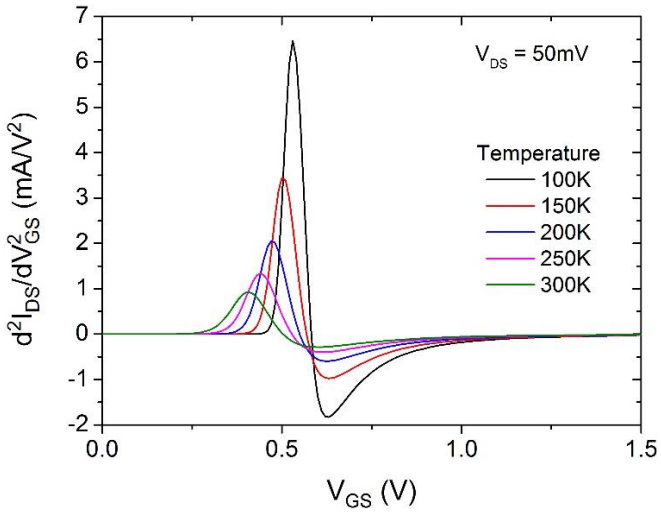

Figure 6. Second derivative of drain current for V_{th} extraction

It is possible to notice a shift of the peaks to the right (towards greater gate voltages) as temperature lowers. The threshold voltages extracted from those peaks and their relation with the temperature are observable in the next graph on Figure 7:

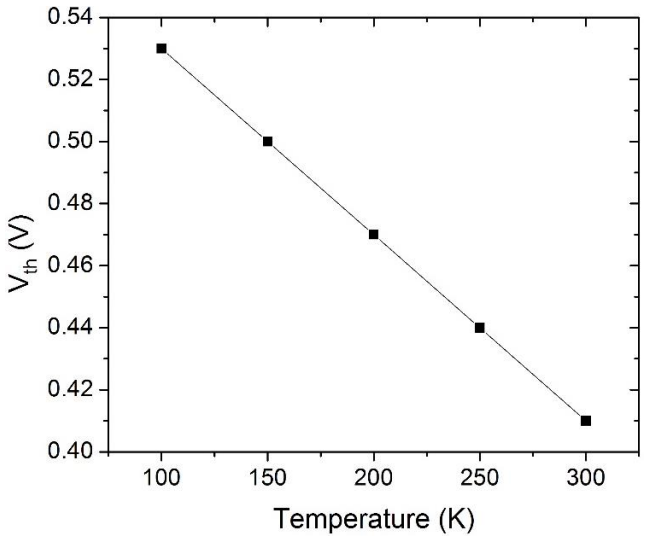

Figure 7. Threshold voltages vs temperature

The simulated device clearly shows that, as the temperature falls, the threshold voltage increases. Such behavior may be better understood observing the Fermi potential (ϕ_F), given by equation (3)

$$\phi_F = \frac{kT}{q}\ln\left(\frac{N_A}{n_i}\right) \quad (3)$$

Where k is the Boltzmann constant, T is temperature, q is fundamental electric charge, while N_A and n_i are the acceptor and intrinsic carrier concentrations. At first glance, it should be expected that, as temperature decreases, the Fermi potential should also fall. However, that is not the case, since the number of electrons and holes per unit of volume in an intrinsic semiconductor is also temperature dependent like shown in equation (4).

$$n_i = BT^{\frac{3}{2}}e^{-\frac{E_g}{2kT}} \quad (4)$$

Where B is a material-dependent parameter and E_g is the bandgap energy. The combination of both expressions shows that, for lower temperatures, the Fermi potential does indeed rise (that is, the energy necessary to add electrons to the depletion region increases), and consequentially the threshold voltage must increase, just as obtained from the simulations.

After extracting the threshold voltages, it should be possible to obtain the Drain Induced Barrier Lowering (DIBL), that is, a measure of how much the drain voltages affects the threshold voltage. However, the values found for different temperatures were quite similar, and lower than 20mV/V, excessively small to be considered relevant. These results suggest that the simulated device actually has a channel proportionally longer than expected, and does not suffer from short channel effects.

Another relevant characteristic to be analyzed is the transconductance of the device, which may be seen on Figure 8:

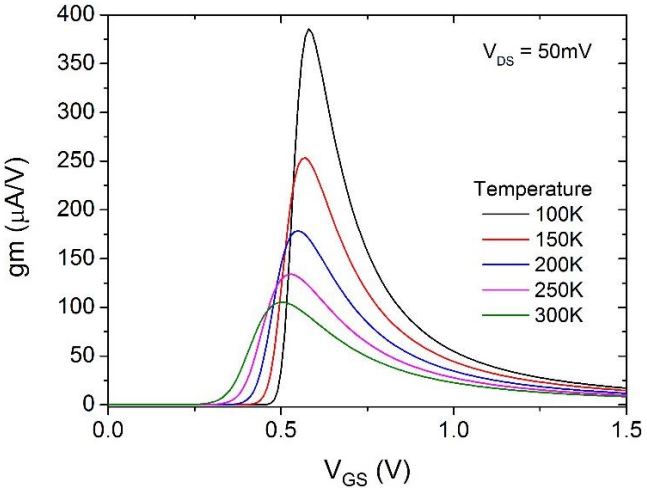

Figure 8. Transconductance vs gate voltage

The transconductance reflects the capacity of controlling the drain current through the gate voltage, as can be observed by equation (5).

$$gm = \frac{dI_{DS}}{dV_{GS}} \quad (5)$$

The maximal points obtained for the transconductance as a function of the temperature are presented below on Figure 9:

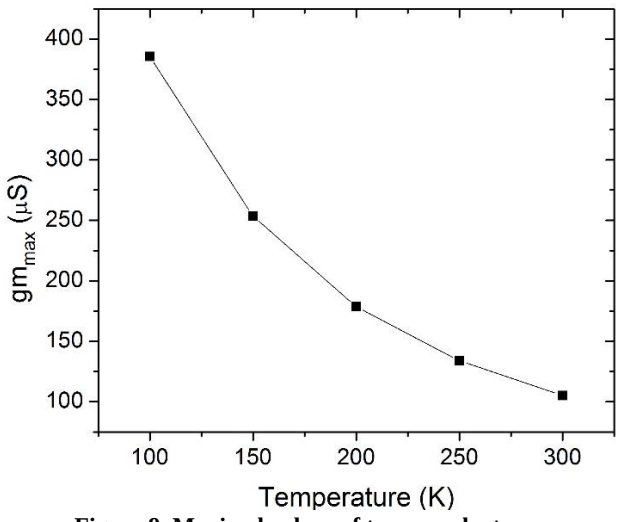

Figure 9. Maximal values of transconductance

As previously discussed, the carriers present a higher mobility for low temperatures, which explains why the transconductance increases at lowering temperatures. This relation is even clearer when analyzing the maximum transconductance values for each temperature, since they depend directly on the low field mobility values. This is the reason why, in many applications, the mobility value itself is extracted from the transconductance curves.

Other important characteristic to be considered is the ratio between ON-state current and OFF-state current (I_{ON}/I_{OFF}), presented on Figure 10:

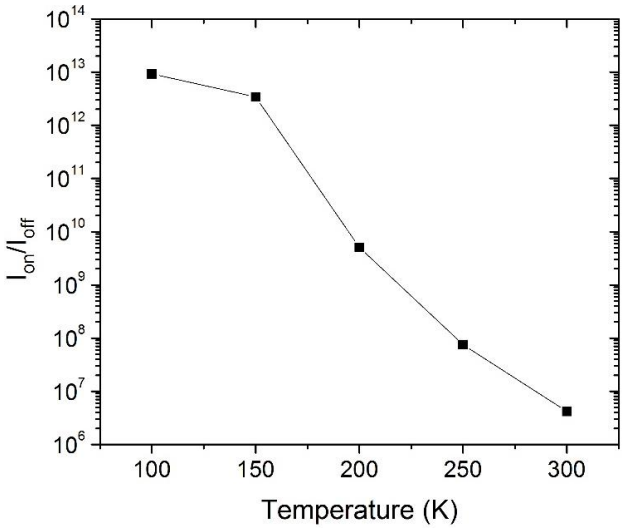

Figure 10. Relation between I_{ON}/I_{OFF}

It has also been previously discussed that, at low temperatures, the off current (that is, the drain current when the gate voltage is below threshold) should be smaller than the one at higher temperatures; while the on current (that is, the drain current when the gate voltage is above threshold) should be greater than the one at higher temperatures. It is noteworthy that most of the increase in the I_{on}/I_{off} ratios is due to the OFF-state current, which sinks much faster with the temperature variation than the on current rises, as can be noticed on Figure 3. However, the results at lower temperatures are excessively high, indicating an OFF-state current too low: considering that the ON-state currents are around 100μA, the off current at 100K should be around 10^{-17}A. The explanation for such a low value lies on the gate leakage and interface traps. Since both were neglected, the OFF-state current approaches the ideal case.

4. CONCLUSIONS

The basic parameters of 3D NMOSFET behavior were analyzed from room to low temperatures. It was observed a reduction of the subthreshold swing as temperature goes down, assuring an almost abrupt transition from OFF-state to ON-state. The obtained theoretical values were guaranteed, since the interface traps were neglected in the simulations. In spite of that, the ON-state current is higher, because the mobility is also higher at lower temperatures, increasing the current drive. This opposite trends of the drain current results in the ZTC point, in which a similar current drive for all temperatures is obtained. The mobility improvement can also be observed through the transconductance increase at low temperatures. The threshold voltages also presented higher values for lower temperatures, as predicted by the theory. The very small fin width of the studied device (20 nm) allows an almost complete control over the charges in the channel, keeping the subthreshold slope near to the theoretical limit, resulting in an almost ideal OFF-state current that, in turn, rises strongly the I_{ON}/I_{OFF} ratio.

5. ACKNOWLEDGMENTS

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6. REFERENCES

[1] Colinge, J. P., Silicon-On_Insulator Technology: Materials to VLSI, Kluwer Academic Publishers, NY, 2004.

[2] Colinge, J. P., FinFETs and Other Multi-Gate Transistors. 1ª Edição Springer, 2008.

[3] "Intel Reinvents Transistors Using New 3-D structure". Intel. Retrieved 2014-05-23, from Intel's site: http://newsroom.intel.com/community/intel_newsroom/blog/2011/05/04/intel-reinvents-transistors-using-new-3-d-structure

[4] Obasih, K. M.; Mruzek, M. T. (1996). "Thermal design and analysis of a cryogenless superconducting magnet for interventional MRI therapy". In Timmerhaus, K. D. Proceedings of the 1995 cryogenic engineering conference. New York: Plenum Press. pp. 305–312. ISBN 0-306-45300-2.

[5] Van Zeghbroeck, B. J., Principles of Semiconductor Devices, University of Colorado, 2004

[6] Goel, N.; Tripathi, A., "Temperature effects on Threshold Voltage and Mobility for Partially Depleted SOI MOSFET". In International Journal of Computer Applications 42(21):56-58, March 2012. Published by Foundation of Computer Science, New York, USA.