Power nMOSFET devices under X-Ray effect

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***Abstract* — This work presents an analysis of a commercial power MOSFET transistors used in DC-AC converters at UPS devices. It was observed an increase on the threshold voltage. A slight reduction on the drain bias and transconductance was also seen. Moreover, these devices indicating a larger breakdown voltage, which can be useful, considering the hard working conditions of theses power devices.**

Keywords – Power MOSFET, DC-AC converters, X-Ray effect.

I. Introduction

The power metal–oxide–semiconductor field effect transistors (MOSFET) have been widely used in DC-AC converters and in power supplies thanks to their low conduction power loss, high input impedances and high switching speed [1-4]. These converters can be found in many different environments and places, such as in locomotive electrical circuit; power substations; space stations and others. Some of these environments can expose the electrical circuits to radiation, and in some cases can damage the circuits [5-10].

Radiation refers to any physical processes of emission and propagation of energy, or by wave phenomena either by particles with kinetic energy. Ionizing radiation has a higher energy electron energy of binding of an atom with its nucleus, whose energy is enough to start their electron orbitals. Figure 7 below shows the electromagnetic spectrum indicating that due to the radiation frequency is regarded as ionizing, and what are the types [11-16].

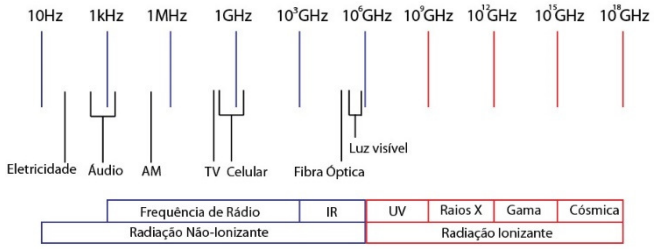

Fig. 1 - Electromagnetic spectrum [12].

This ionizing radiation can be absorbed by semiconductor devices, changing its main parameters or may even damage them permanently. We can consider three effects of radiation being predominant to achieve a device: Total ionizing dose, displacement damage and single event effects [17].

Basing on this analysis, the motivation for this work is to investigate the behavior of a commercial power nMOSFET transistor used on DC-AC converters when submitted to Total Ionizing Dose Effects, using X-Ray beam.

II. Experimental setup and device analyzed

The X-Ray Diffractmeter XRD-7000 (Shimadzu) was used to produce X-ray radiation for power MOSFET testing, with an exposure rate of 1.15 Mrad/min (Fig. 2). For the characterization it was used the Semiconductor Characterization System Keithley 4200. The commercialized Power n-type MOSFET used in this analyzed has a R_{DS} (on) of 0.077 Ω, a drain current of a 28 A and drain bias of 100 V. The package is a TO-220AB. It is worth noting that it was not made to correct the total dose of radiation absorbed by the epoxy coverage of the devices, but it is estimated that only 20% of the total radiation dose value has really hit the device.

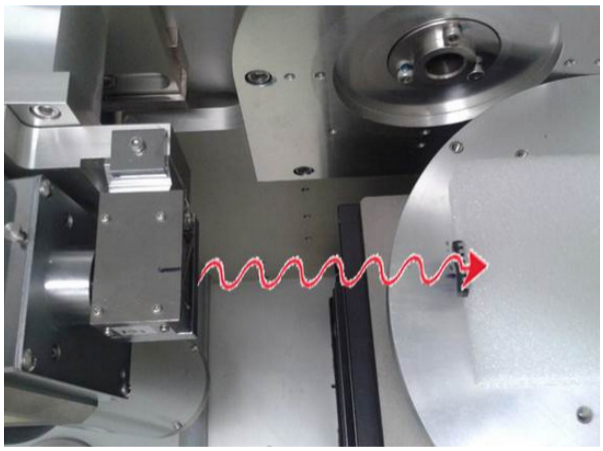

Fig. 2 – Photography of the equipment used for the X-ray radiation.

A. *Drain current*

Fig. 3 presents the drain current as a function of the gate bias extracted pre- and post-radiation. A small reduction can be seen on the drain current. Additionally, a deviation on the drain current transition was also observed. In order to analyze it, the threshold voltage (V_T) was extracted, through second derivative method [18]. An increase on V_T could be observed (pre-rad 3.08V and post-rad 3.52V).

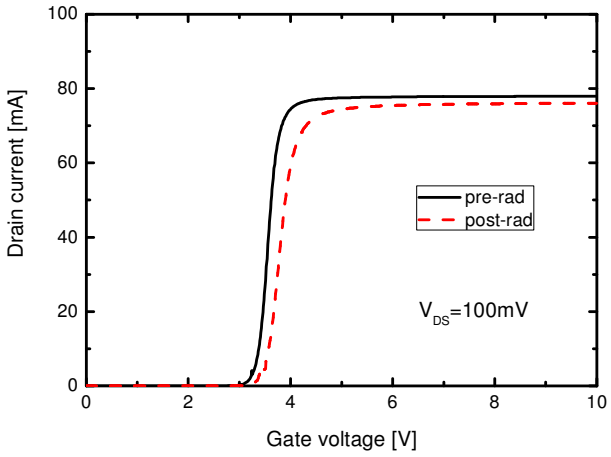

Fig. 3 - Drain current as a function of the gate voltage.

Fig. 4 shows a schematic energy band diagram of a MOS structure, where positive bias is applied to the gate, so that electrons flow toward the gate and holes move to the Si substrate. The most sensitive parts of a MOS system to radiation are the oxide insulators, and some effects are involved as showed [19-24]:

- Electron/hole pair generated: when radiation passes through a gate oxide, electron/hole pairs are created by the deposited energy. In the insulator, the electrons are much more mobile than the holes and they are swept out of the oxide. Some fraction of the electrons and holes will recombine. The holes, which escape initial recombination, are relatively immobile and remain near their point of generation, where they cause a negative threshold voltage shift in a MOS transistor.

- Transport of holes to the silicon/oxide interface: this process is very sensitive to the applied field, temperature, oxide thickness, and (to a lesser extent) oxide processing history.

- Hole trapping that reaches the Si interface: some fraction of the transporting holes fall into relatively deep long-lived trap states and can cause a remnant negative voltage shift.

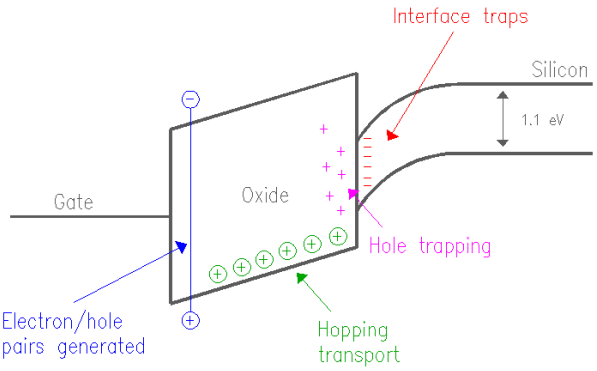

Fig. 4. Energy band diagram for a MOS structure, indicating physical effects due to the radiation response.

- Interface traps: these traps are localized states with energy levels in the Si band-gap. Their occupancy is determined by the Fermi level (or by the applied voltage), giving rise to a voltage-dependent threshold shift. Interface traps are highly dependent on oxide processing.

The accumulation of positive charges trapped in the oxide creates a vertical electric field at the surface of the substrate by attracting electrons to the silicon / oxide interface. The attracted negative charges decrease the concentration of positive charges near the surface of the substrate, which makes it easier to reach the threshold inversion of the substrate, and the visible effect would be to reduce the threshold voltage. But the effect we observed in our devices was the opposite. Another alternative is the presence of loads at the interface between silicon and gate oxide that could cause this increase on the threshold voltage.

B. Transconductance

The transconductance was also analyzed indicating a reduction in its maximum, according Fig. 5. The following equation describes the behavior of the transconductance, and as can be seen the mobility and the gate capacitance reduction could cause a reduction in transconductance. The literature reports that traps induced at the interface between the gate oxide and silicon degrades the mobility of carriers in MOS transistor channel. W is the channel width, µn is the mobility, Cox is the oxide capacitance, L channel length and VDS is the drain bias [25].

$$gm = \frac{W*\mu n*Cox}{L} VDS \quad (1)$$

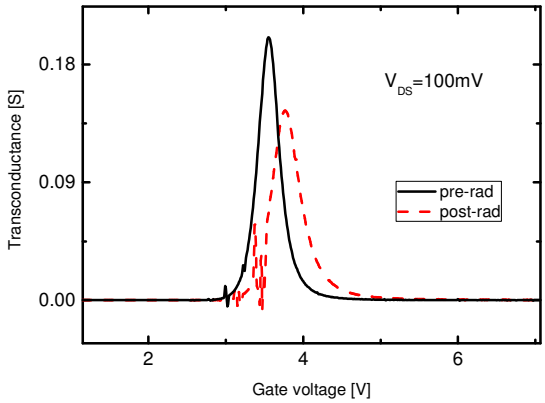

Fig. 5 – Transconductance behavior.

The mobility can be extracted by the equation below, where: μ_{n0} is the mobility before irradiation and ΔNit is the increase in the number of interface traps per unit area. It is possible to see the dependence of the number of traps with the mobility [25].

$$\mu n = \frac{\mu n0}{1+\alpha(\Delta Nit)} \quad (2)$$

C. Gate to drain capacitance

The behavior of the capacitance between drain and source depending on the drain voltage was also analyzed, as shown in Fig. 6 below. The measurement was performed between the drain and source electrodes, with the gate grounded. The device when spouse to X-Ray can present a reduced gate to drain capacitance.

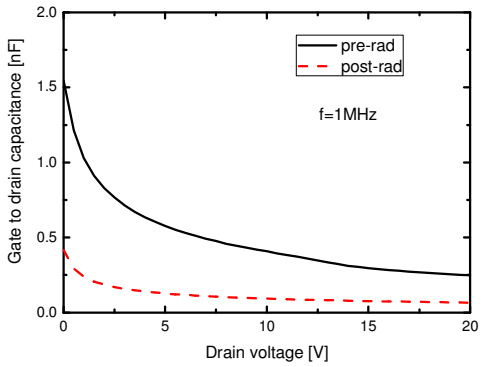

Fig.6 – Gate do drain capacitance as a function of the drain voltage.

D. Breakdown voltage

The breakdown voltage is the maximum voltage that the transistor can withstand without damage. From this voltage begins to increase the current between the source and the drain avalanche process, while the gate and the source are short circuited. Fig. 7 shows the drain current as a function of the drain bias for a zero voltage at the gate. At the voltage of the abrupt increase on the drain current, it is possible to estimate the breakdown voltage that is around 107 V been in agreement with the datasheet of the devices. As shown on Fig. 7 larger voltage can be achieved after the radiation (134V).

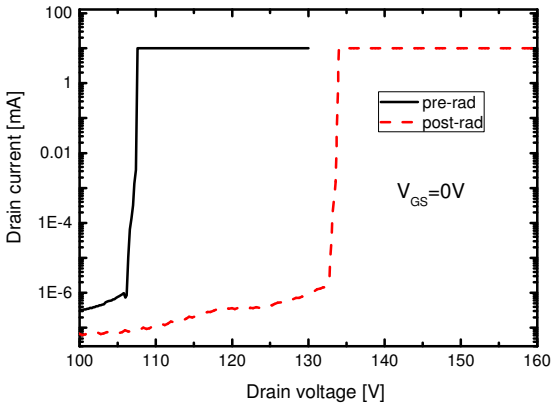

Fig. 7 – Breakdown voltage behavior.

With the interface traps increase there is a lifetime carries rise, this lifetime variation dependence in the leakage current and breakdown voltage was studied from of simulation results. Two-dimensional numerical simulations were performed using the Atlas program [26]

Figure 8 presents the drain current as a function of the drain bias, simulated for different lifetime carriers, during operation in the blocking mode (V_{GS}=0 V). As can be seen through this figure a reduced breakdown voltage with the increased lifetime carriers. The power MOSFET structure contains a parasitic bipolar transistor formed between the N+ source region, the P-base and the N-drift region. With the increase on the lifetime carriers, it is known that the current gain of the N-P-N bipolar transistor is enhanced. As a result, a reduction in the breakdown voltage is observed for larger lifetime carriers [27].

Another important issue is related with the electric field variation. Equation (3) presents the breakdown voltage (V_B) estimation where D is the total dose (rad); t_{ox} is oxide thickness; G is the generation constant for electron-hole pairs in the oxide; F is the fractional number of holes that are transported and trapped at the oxide; q is the electron charge; Ec is the electric field and ε are the dielectric constant. It is know that trapped holes decrease the electric field, causing an increase on the breakdown voltage [25].

$$\frac{\Delta V_B}{V_B} = \frac{qDt_{ox}GF}{\varepsilon E_c} \quad (3)$$

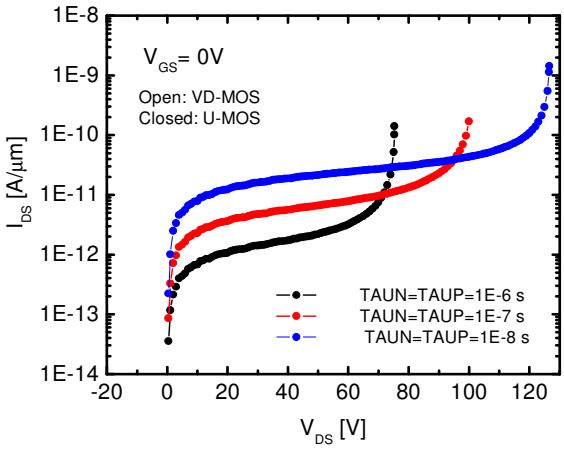

Fig. 8 – Breakdown voltage behavior.

III. Conclusions

This paper presented an analysis about the behavior of power transistors when submitted to X-Ray. It was observed a transconductance decreased due to Coulomb scattering (scattering of one or more particles interact with the electrostatic field of a nucleus) that reduces the mobility. The charges trapped at the interface exert a greater influence on carrier mobility compared to charges trapped in the oxide; with

a higher value of these influences is less mobility. As a result of lower mobility and transconductance and consequently a smaller drain current was observed.

An increase in the threshold voltage was also observed, because the ionizing radiation exposure can induce accumulation of charges at the oxide/silicon interface. Due to TID effect, loads are trapped that produces electrostatic effects causing the deviation of the threshold voltage. This deviation is given by the accumulation of positive charges trapped in the interface, causing the increase of concentration of positive charges on the substrate surface, which makes it harder to reach the threshold for inversion of the substrate. As a result of the increase in threshold voltage, it was also observed an increase in the breakdown voltage of the power transistors when subjected to radiation.

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