Design and characterization of a 2.4 GHz LNA in 180 nm CMOS Technology

Elmo Sette, Ranieri Saldanha, Antonio Souza
Universidade Federal da Paraíba
João Pessoa, Brazil
elmo.sette@cear.ufpb.br

Emmanuel Dupouy
IFPB
João Pessoa, Brazil
emmanuel.dupouy@ifpb.edu.br

***Abstract*— In this paper, we present the design and characterization of a low noise amplifier (LNA) operating at 2.4 GHz and implemented in a 180 nm CMOS IBM technology. Inductive source degeneration topology is used, because of its good trade-off between input matching and Noise Figure. Simulation results show a gain of 9.96 dB and a Noise Figure of 2.09 dB for a power consumption of 11.7 mW. All the design steps are presented: gain optimization and bias point analysis, input and output matching, insertion of a cascode stage, stability, Noise Figure analysis and layout design. The circuit was fabricated, and we obtained a gain of 7.7 dB centered at 2.24 GHz and a bandwidth of about 700MHz. The experimental results are presented at the end of the paper.**

Keywords*— *Low Noise Amplifier; Characterization; Inductive source degeneration; S-parameters.

I. INTRODUCTION

One of the main blocks in a receiver system is the Low Noise Amplifier (LNA). Its main function is to provide enough gain to overcome the noise of the following stages (e.g. a mixer) [1]. The LNA should add as little noise as possible to minimize the effect on overall performance, since its Noise Figure directly impacts the signal to noise ratio of the whole system [2]. Another challenge is to accommodate signals as large as possible without distortion, i.e., provide a good linearity, and to present a specific input impedance to guarantee a good performance of the band pass filter following the antenna and maximum power transfer. Most transceivers operate with standard termination impedances, generally 50Ω [2]. An additional requirement is low power consumption, which is especially important for battery-powered communication systems [3].

This paper is organized as follows. Section II reviews the properties of inductive source degeneration topology used in this work. Section III presents the LNA design. Results and conclusions are discussed in Section IV. Finally, in Section V we draw some conclusions.

II. TOPOLOGY

The low noise requirement leads us to the use of only one active device at the input of the LNA [4]. By analyzing MOSFET two-port noise parameters, the source impedance that yields minimum noise factor is inductive and generally unrelated to the conditions that maximize power transfer. Moreover, it's difficult to provide a good matching for 50Ω source impedance without degrading the noise performance, because the MOSFET input impedance is inherently capacitive [1]. A good compromise between input matching and noise figure may be achieved by using inductive source degeneration shown in Fig.1, which allows obtaining real input impedance without the use of a resistor.

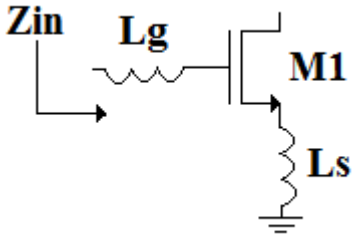

Fig. 1. Inductive source degeneration topology.

To simplify the analysis, consider a MOSFET model that includes only a transconductance and a gate-source capacitance. In this case, the input impedance of the circuit shown in Fig. 1 (Z_{in}) has the following form:

$$Z_{in} = \frac{1}{sC_{gs1}} + s(L_s + L_g) + \frac{g_m L_s}{C_{gs1}} \quad (1)$$

where C_{gs1} is the gate to source capacitance of M1, L_s is the degeneration inductor, L_g is the gate inductor and g_m is the transconductance. As can be seen from (1), the input impedance is composed of two parts, one real part which is independent of frequency and an imaginary part which is frequency dependent. The amplifier will be matched to 50Ω at the input, which leads us to two different equations:

$$\frac{1}{sC_{gs1}} + s(L_s + L_g) = 0 \quad (2)$$

$$\frac{g_m L_s}{C_{gs1}} = 50\Omega \quad (3)$$

Thus, the input impedance is the same of an RLC series circuit with the resistive term directly related to inductance L_s. But we can also note from the equations that the input impedance is purely resistive only at the resonant frequency [1].

III. LNA DESIGN

A. Gain optimization and bias point analysis

Our work started by studying transistors available in the IBM CMOS 7RF 180 nm technology. We chose the nfet_rf transistor because it is made for RF applications. To analyze its ability to provide gain at high frequencies, the maximum gain (Gmax) of the transistor is extracted from S-parameters simulations for various bias currents and values of transistor length and width.

A sweep simulation of gate voltage and drain voltage is then made to help selecting a bias point that ensures the transistor is in the saturation region, while avoiding problems such as avalanche.

B. Choice of inductors

Inductive degeneration should be as small as possible, because a small L_s leaves room for a high transconductance (and gain), as we can see from (3). The inductance L_g gives us an additional degree of freedom to satisfy (2) and should be ideally large to improve circuit performance in terms of noise. Maximizing L_g implies an increase in quality factor (Q) of the input network which minimizes the Noise Figure. The choice of the inductances is shown in Fig. 2.

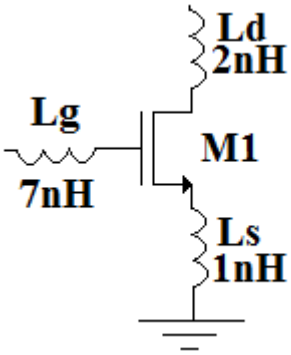

Fig. 2. Circuit with inductors of the technology.

C. Input and output matching

In cases that we want to maximize the gain, the LNA should be matched at input and output to provide minimum reflection as possible, consequently a maximum power transfer, and present a specific input impedance (in this case 50Ω) to guarantee a good performance of the bandpass filter following the antenna. Here, S-parameters are fundamental too, because we can easily analyze input and output impedances as S11 and S22 respectively, with the support of the Smith Chart.

The best way to match the input is manipulating values of C_{gs} and L_s from (3), but this is an approximation because some factors are neglected such as C_{gd}. In our case, we fixed a small inductance L_s to let us increase g_m as we want, leading us to vary only C_{gs}. By analyzing simulation results, we concluded that the transistor had a very small C_{gs} even with the maximum value of width allowable and a large number of fingers, preventing the input matching. The solution was to insert an external capacitor (C_{gs2}) between gate and source, to increase the total gate-to-source capacitance.

The next step is to match the output, which can be achieved with series and parallel capacitors. After matching the output, a small change occurs at the input, which is easily solved by reducing the capacitance of C_{gs2}.

D. Cascode stage

Cascode stages are often used in this topology to enhance reverse isolation (S12) by reducing effect of C_{gd} of the main transistor [1]. After the insertion of the cascode stage, the reverse isolation improved as well as the gain.

E. Stability

The LNA may become unstable due to the presence of feedback paths from the output to the input for certain combinations of source and load impedances. To test the stability of a circuit, we used the K and Δ parameters [2]. If $K>1$ and $\Delta<1$, then the circuit is unconditionally stable, i.e., any combination of source and load passively realizable impedances will not result in oscillation. The difficulty in using K is that it needs to be calculated for a wide frequency range [2].

In this work, we observed in simulations that K remains greater than one and Δ smaller than one for the frequency range considered (1Hz to 100GHz). Another way to visualize stability is to look for oscillation conditions (Barkhausen criterion) at the frequency range considered. This method was also tested, and showed that indeed there is no condition for oscillations.

F. Noise figure analysis

One of the main specifications of an LNA is its Noise Figure. It accounts for the degradation in the signal-to-noise ratio when the signal crosses the device, and corresponds to the noise factor expressed in dB.

G. Layout design

Once all the schematic simulations were performed and specifications were met, we started the layout. DRC (*Design Rules Check*) simulations ensure that the design rules of the technology are being fulfilled while LVS (*Layout versus Schematic*) simulations show that the layout corresponds to the circuit schematic. Then, we extracted all circuit parasitics through PEX (*Parasitic Extraction*) simulations, to know the

real circuit performance. The circuit, layout and results are presented in the next section.

IV. RESULTS AND DISCUSSIONS

In Table I, we summarize the performance of our LNA after the parasitics extraction in terms of S-parameters, Noise Figure (NF) and power consumption. Fig. 3 and Fig. 4 present the schematic and layout respectively.

TABLE I. POST-LAYOUT LNA PERFORMANCE

Parameter (@ 2.4 GHz)	Value
S11	-26.567 dB
S12	-44.96 dB
S21	9.96 dB
S22	-9.6 dB
NF	2.09 dB
Power consumption	11.7mW

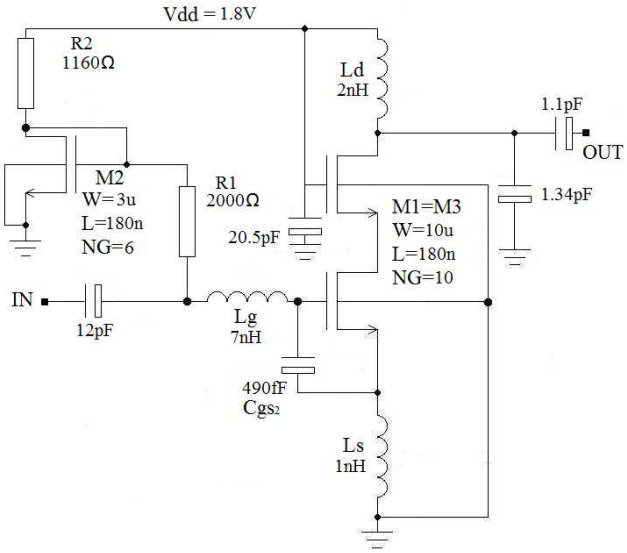

Fig.3. LNA Schematic.

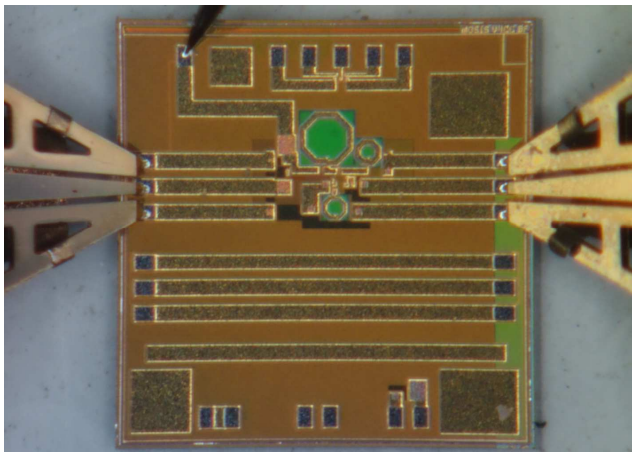

Fig. 4. Microphotography of the LNA.

To accommodate another design and some test structures, our LNA was included in a 2 mm x 2 mm die. To be able to place the LNA pads on the periphery of the die, we had to add lines for ground and signal paths (see Fig. 4).

Fig. 5 compares the data from post-layout simulations with actual measurements.

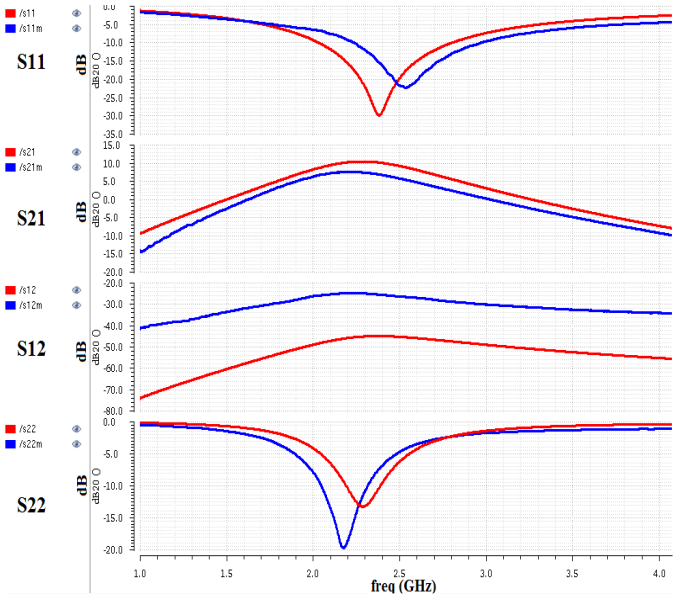

Fig. 5. Post-layout simulations (red) and final LNA (blue) S-parameters.

We observe a slight frequency shift (increase) in S11 and a slight frequency shift (decrease) in S22, which causes a reduction in the overall gain (S21). This discrepancy may be due to the long paths between the LNA and the pads (see Fig. 4), since our parasitic extraction considered RC contributions (we did not performed electromagnetic simulations).

Fig. 6 shows the measured gain for three different samples of the LNA, indicating that the gain is highly reproducible.

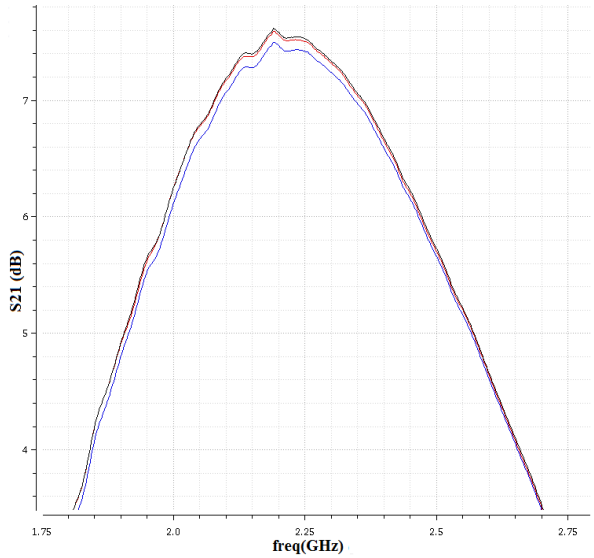

Fig.6. S21 for three LNA samples.

This circuit was designed to operate with a 1.8 V supply voltage. Fig. 7 shows the measured S21 (gain) under different supply voltages.

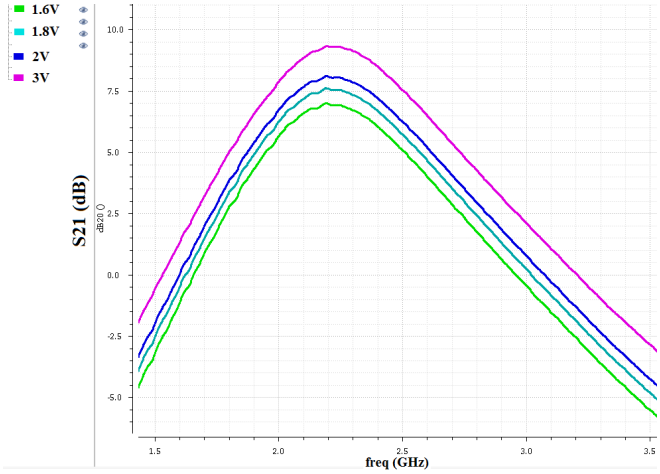

Fig. 7. S21 under different supply voltages: 1.6 V (green), 1.8 V (light blue), 2 V (blue) and 3 V (pink).

We observe a monotonic increase in gain as we increase the supply voltage and simultaneously we noticed that the circuit operates normally with a power source up to 3 V.

In Table II, we compare the performance of our LNA with other published works.

TABLE II. PERFORMANCE COMPARISON WITH PUBLISHED WORKS

	CMOS Tech.	Freq. (GHz)	NF (dB)	Gain (dB)	Pdc (mW)	VDD (V)
[5]	0.18um	2.4	2.88	10.1	0.84	0.6
[6]	0.13um	2.45	2.06	22.1	4.8	1.2
[7]	0.13um	2.4	0.78	16.5	3.3	0.5
[8]	0.18um	2.45	3.7	13.1	75	n/a
This work	0.18um	2.24	2.09[a]	7.7	11.7	1.8

[a] post-layout data

V. CONCLUSIONS

A fully-integrated one-stage inductive source degenerated cascode configuration for narrowband (2.4 GHz) LNA has been designed and discussed. The presented design was implemented using IBM 180 nm CMOS technology process. The actual measurements show a gain of 7.7 dB in 2.24 GHz with a good input and output matching for a power consumption of 11.7 mW. We were not able to get the instrumentation in time for Noise Figure measurements, but post-layout simulations show a good NF (2.09 dB).

References

[1] Lee, T. H., The Design of CMOS Radio-Frequency Integrated Circuits. Cambridge University Press, 2004

[2] Razavi, B., RF Microelectronics 2nd edition. Prentice-Hall, Inc., 2012.

[3] Shaeffer D. K., and Lee T. H., *"A 1.5V, 1.5GHz CMOS Low Noise Amplifier"*, IEEE Journal of Solid-State Circuits, Vol.32, No. 5, May 1997.

[4] Telli A., and Askar M., "CMOS LNA Design For System-on-chip receiver Stages", 2004 Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems, 2004.

[5] J. Wu, Y. Lin, and Y. Tsai, "A sub-mW CMOS LNA for WSN Applications," in Asia-Pacific, Microwave Conference Proceedings (APMC), 2012, pp. 899-901.

[6] H. A. Eshghabadi and F. Eshghabadi, "An Improved Power Constrained Simultaneous Noise and Input Matched 2.45 GHz CMOS NB-LNA," in 2012 IEEE International Conference on Circuits and Systems (ICCAS), 2012, pp. 92–97.

[7] L. Chen, Z. Li, and Z. Wang, "A 0.5 V CMOS LNA for 2.4-GHz WSN application," in International Symposium on Signals Systems and Electronics (ISSSE), 2010

[8] S. Andersson, C. Svensson, and O. Drugge, "Wideband LNA for a multistandard wireless receiver in 0.18um CMOS," in Proceedings of the 29th European Solid-State Circuits Conference, September, 2003, pp. 655-658.