

Study of Thermal Annealing on Irradiated MOSFET Devices

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1. Abstract

Electronic devices exposed to radiation suffer degradation on their electrical characteristics, as the threshold voltage, which can be recovered by thermal annealing treatment. The aim of this work is to characterize irradiated MOSFETs and analyze the behavior of thermal annealing processes, in order to understand the temperature effects in the electrical parameters of irradiated circuits.

2. Introduction

With the development in the microelectronics industry, a broader study is needed on the limitations and reliability of the electronic devices, when they are exposed to external interferences [1]. One of the most important electronic devices, the MOSFET (Metal Oxide Semiconductor Field Effect Transistor) is used to amplify electrical signals. Its operation occurs when a voltage is applied on the gate, which attracts charges between source and drain terminals, and creates a channel through where electric current flows. When the device under test (DUT), MOSFETs, are exposed to ionizing radiation, some energy is accumulated on the material structures, promoting a variation in the mobility of its electrons and holes, which directly affects their electrical conductivity. The kinetic energy obtained by the electron is dissipated through the interaction between electrons and the atomic core. This radiation can interact with the material through three processes: Compton effect, photoelectric effect and the production of electron-positron pairs.

In the Compton effect the photon undergoes elastic scattering with a weakly bound electron to the atom, resulting in the output of the electron from its orbit and the change of direction of the incident photon. In the photoelectric effect, the photon reaches the material and an electron on the orbit of the atom is ejected with a kinetic energy E [3]. This process occurs according to Equation (1) below:

$$E = h\nu - W \quad (1)$$

where h is the Planck's constant, ν is the frequency of the incident photon and W is the work function of the material.

The production of electron-positron pair occurs with the interaction of radiation with the core of a particle, where the radiation disappears, and a pair electron-positron is created [1].

After exposed to direct or indirect ionization radiation, the Total Ionizing Dose (TID) charges are trapped in energy states [2]. By trapping charges in the oxide energies of states and at the interface between oxide/Si, it is possible to notice some effects, such as the change of threshold voltage of the device. These device degradations in the original characteristics of the DUTs, generating uncertainty about its parameters. Depending on the conditions the devices are subjected, the physical mechanisms can provoke permanent failures in the device. Techniques are used to minimize these effects and to recover electronic devices, such as thermal annealing treatment [3]. This technique involves the heating of devices to a certain temperature and time, which promotes the rearrangement of earlier trapped electrons and holes, which usually are in the oxide or in the oxide/Si interface. This fact happens because due the temperature, the material atoms receive energy by inducing the transition of carriers from energy bands that were not excited to energy bands which occurs the conducting and decoupling of some carriers from atoms, ionizing the material [6]. Rapid thermal annealing results in recovery of their initial electrical conditions as a consequence of a recombination of carriers. International Norms, as the standards provided by the European Space Agency (ESA) or the US Department of Defense [4], generally are used to test the resistance of the devices depending on heating.

This work shows the behavior and analyses the recovery of unbiased n- and p-MOSFETS from the device CD4007 after different thermal annealing treatments. The irradiation procedure was performed by a 10-keV X-ray beam. In this case, the most likely effect is the photoelectric effect, and therefore, the ionization occurs mainly by electrons generated by photoelectric effect, which are distributed sparsely in the oxide material, with a range of about $0.5 \mu\text{m}$ [5].

3. Experiment

The epoxy layer of the integrated circuit was removed to eliminate a barrier between the device and radiation as it is shown on Fig. 1. Thus, it is possible to define more precisely the accumulated dose on the device.



Fig. 1 - Detail of the Integrated Circuit CD4007 used on the experiments, after the removal of the epoxy layer.

In order to assess the behavior of the irradiated MOSFETs after thermal annealing, the Integrated Circuit (IC) CD4007, was tested on different conditions. The IC is an inverter that has access to two complementary pairs MOS and a NOT logic gate, which is composed by 3 n-MOS and 3 p-MOS transistors. The X-ray irradiation procedures were performed with a Shimadzu XRD-7000 Diffractometer, as it is shown on Fig. 2, with a 96 rad/s dose rate. It was applied a voltage of 20 kV on the X-ray tube terminals, generating an X-ray beam of 10 keV of effective energy. The electrical parameters of the transistors were characterized with an Agilent HP 4156C semiconductor parameter analyzer. The device was characterized previously in order to record the device behavior without radiation degradation.



Fig. 2 - Detail of the XRD-7000 Diffractometer of the Centro Universitário da FEI.

With the purpose to understand the effect of the temperature on the physical mechanisms that would trap the charges in the device, two different experiments were conducted:

I – Rapid Thermal Annealing (RTA): in the first experiment, with rapid thermal treatment, the device has been exposed to 3 successive doses of radiation, and its electrical parameters were measured right after each irradiation stage. Following each stage, the IC was heated in a FANEM 520 stove during a period of one hour, after a cumulative dose of 100 krad, and for two hours, after a cumulative dose of 250 krad. After the final stage of irradiation, having accumulated a total dose of 500 krad, the device remained in the stove for two hours at 100°C.

II – Extended Thermal Annealing (ETA): in the second procedure, with the extended thermal treatment, the device received a total dose of 500 krad in a single irradiation session, and it was maintained at 100°C for 168 hours (1 week). The IC was characterized after each stage of thermal treatment and also one week after the irradiation process.

4. Results

4.1. Results for experiment I

For the first experiment, with the rapid thermal treatment, Fig. 3 and Fig. 4 present the resulting $I_{DS} \times V_G$ characteristics curves for nMOS and pMOS transistors. Threshold voltages before and after the RTA processes are presented in Table 1. After thermal treatment, the threshold voltage almost returned to its pre-radiation value for the n-MOSFET. In this case, energy provided to the trapped charges in the devices oxides and interfaces increased the rate of recombination, accelerating recovery.

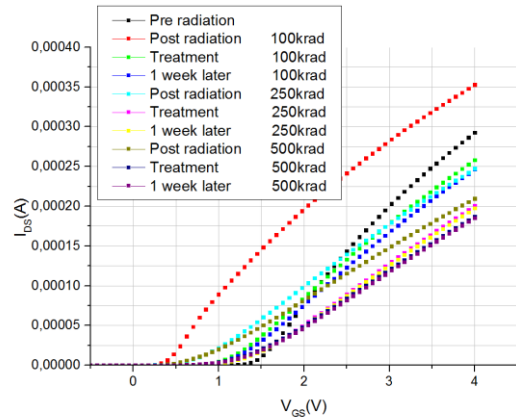


Fig. 3 – n-MOS $I_{DS} \times V_G$ curves for different accumulated doses and thermal annealing treatment periods.

Table 1- Threshold Voltage of n-MOS transistor for accumulated doses of 100 krad, 250 krad and 500 krad, and different thermal annealing periods. Room Temperature (A) refers to an ambient temperature of 25°C; Before Rapid Thermal Annealing (B) is about the moment after the radiation procedure; After Rapid Thermal Annealing (C) refers right after one or two hours of rapid thermal treatment; 168 hours later (D) are the results after one week of the experiment, when the device reaches its permanent state and its electric parameters stabilize.

	Threshold Voltage (V)			
	n type			
Accumulated Dose (krad)	Room Temp. (A)	Before Rapid Thermal Annealing (B)	After Rapid Thermal Annealing (C)	168 hours later (D)
Pre radiation	1.480			
100	0.780(2)	0.415(2)	1.085(3)	1.105(3)
250	0.400(2)	1.165(4)	1.325(4)	1.315(4)
500	0.980(2)	0.650(3)	1.155(4)	1.200(3)

Table 2- Threshold Voltage of p-MOS transistor for different accumulated doses and thermal annealing periods.

Accumulated Dose (krad)	p type			
	Room Temperature	Before Rapid Thermal Annealing	After Rapid Thermal Annealing	168 hours later
Pre radiation	-1.310			
100	-2.815	-3.005	-3.150	-3.035
250	-3.690	-2.980	-3.970	-3.970
500	-4.100	-3.800	-5.000	-5.025

The results presented in Table 2 indicate that the damage on the p-MOSFETs, due to irradiation, could not be recovered with thermal annealing. In fact, thermal annealing even worsened the parametric degradation.

4.1. Results for experiment II

For the second experiment, with the extended thermal treatment (ETA), the resulting $I_{DS} \times V_G$ characteristic curves for nMOS and pMOS transistors are presented on Fig. 5 and Fig. 6. Threshold voltages before and after the thermal annealing process are presented in Table 3.

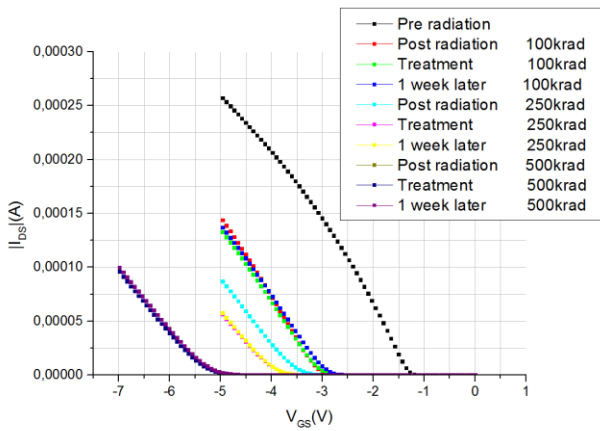


Fig.4 – p-MOS $I_{DS} \times V_G$ curves for different accumulated doses and thermal annealing treatment periods.

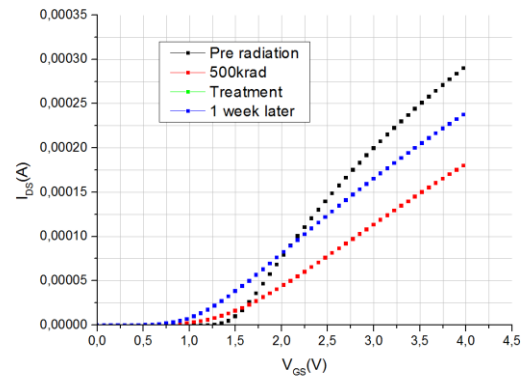


Fig. 5 – n-MOS $I_{DS} \times V_{GS}$ curves for an accumulated dose of 500 krad and after one week of thermal annealing treatment.

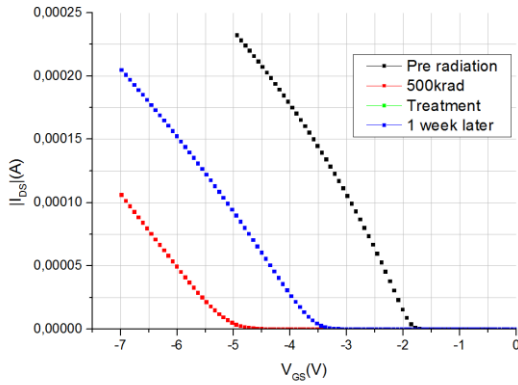


Fig. 6 – p-MOS $I_{DS} \times V_{GS}$ curves for an accumulated dose of 500 krad and after one week of thermal annealing treatment.

Table 3- Threshold Voltage for an accumulated dose of 500 krad and after one week of thermal annealing. The uncertainty in measurements is 0.002

	Threshold Voltage (V)	
	N type	P type
Pre rad	1.480	-1.310
After 500 krad	1.200	-5.025
After treatment	1.030	-3.545
168 hours later	1.030	-3.545

In this experiment, it is noticeable that the threshold voltage of the device reaches its permanent state right after the thermal treatment. The results obtained one week after the experiment are just the same as the one after the heating.

In comparison with the first experiment, the threshold voltage of nMOS transistor reaches lower values, while pMOS transistors shows a better recovery, although its threshold voltage are still distant from its initial conditions.

4. Conclusions

N-MOS transistors have a better response to thermal annealing treatment. The electrical parameters were almost restored to their pristine values, which means that the energy absorbed due heating, assisted in the recombination of charges. Oxide trapped holes were almost removed or at least compensated. However, the same result was not observed for p-MOS transistors. In this case, thermal annealing was not effective and this treatment even worsened the threshold voltage of the p-type transistor.

The experiment after one week of thermal annealing

(ETA) recovered some of the threshold voltage of the transistors. On n-MOS, the threshold voltage reached a lower value than its pristine value.

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