Improvement for the thermal resistance extraction method related with self-heating effect

C. A. B. Mori[1], J. A. Martino[1]
[1]LSI/PSI/USP – University of São Paulo
São Paulo, Brazil
carlos.mori@usp.br

P.G.D. Agopian[1,2]
[2]UNESP - Universidade Estadual Paulista
São João da Boa Vista, Brazil

***Abstract*—In this paper, an improvement for the thermal resistance extraction using one of the traditional methods for self-heating effect study is proposed. It was observed experimentally that, for some devices, the zero power condition could not be linked to room temperature as usually done, because it can strongly underestimate the thermal resistance. Removing this constrain, the thermal resistance increased around 100% for the SOI device studied in this paper.**

Keywords—self-heating effect; thermal resistance

I. INTRODUCTION

The self-heating effect (SHE) has become a greater concern for the industry in recent years, since newer technologies imply in smaller devices, new materials and geometries, ultimately resulting in an increase of this effect. As an example, it is more difficult for Semiconductor-On-Insulator (SOI) transistors to dissipate the heat generated than for conventional bulk devices, since the oxide insulator below the channel has a lower thermal conductivity. This effect and its consequences have been extensively studied, modeled and characterized in many different studies [1][2][3].

II. THEORETICAL REVIEW

A. Causes of the self-heating effect

Firstly, one must note that the main physical effect behind the SHE is the Joule heating. When a current flows through the device's channel, it generates heat proportional to the square of this current. However, the temperature increase caused by this heat that was generated reduces the mobility of the charge carriers according to [4]:

$$\mu_{eff} = \mu_{eff0}(T/T_0)^{-k} \quad (1)$$

where μ_{eff0} is the effective mobility measured at the temperature T_0 (which is usually room temperature), and k is the mobility temperature degradation exponent, commonly obtained from empirical measurements.

Because of this mobility drop, the drain current also decreases, thus, two simultaneous phenomena are taking place in the device: one is the amount of heat generated due to the Joule effect, which is proportional to the square of the current, while the second is the current reduction due to the mobility decrease. As long as the device is kept on, both phenomena will take place, eventually reaching a dynamic equilibrium.

However, older devices do not present a significant SHE, therefore, one must also notice that smaller devices have a smaller surface area, but still a similar current density, which implies in a greater difficulty to dissipate all the heat generated.

Another relevant change in newer devices is the presence of the buried oxide in the case of SOI transistors, presented in Fig. 1 and further explained in [5]. As presented in [6], the thermal conductivity of bulk silicon is approximately ten times greater than that of silicon oxide, which means that traditional bulk devices may dissipate heat much more efficiently through the bulk than SOI devices.

The improvement of the SOI technology allowed thinner buried oxides, resulting eventually in the Ultra Thin Body and Buried oxide (UTBB) [7]. Even though this thinning of the oxide helps to improve the thermal characteristics of the device, the ultra-thin body brings a new problem, since it has a much smaller thermal conductivity due to phonon confinement and boundary scattering [6]. Thus, the self-heating is still a relevant problem even for such state of the art technology.

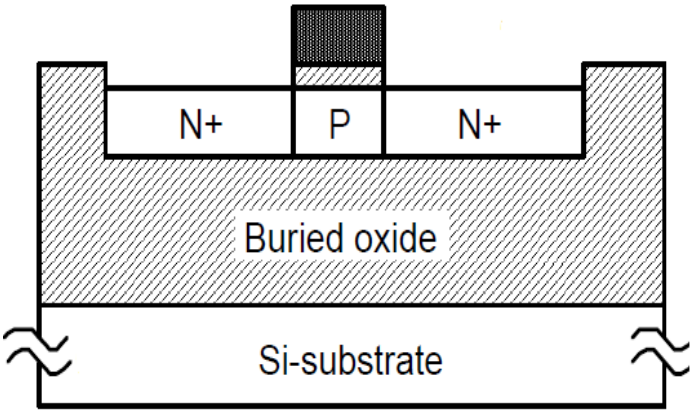

Fig. 1. The SOI transistor. Source: [5]

B. Characterization of the self-heating effect

Two main parameters are defined to represent all the thermal effects taking place inside the device: the thermal resistance R_{th} and the thermal capacitance C_{th}. The first represents how efficiently the heat is removed from the device,

Sponsor: Fundação de Amparo à Pesquisa do Estado de São Paulo (FAPESP)

while the latter represents how much heat is stored inside the device.

Consequently, the thermal resistance is dependent from the device's surface area, since this is through where the heat is removed, meaning that smaller devices have larger thermal resistances; and the thermal capacitance is dependent from the device's volume, since the heat is accumulated along the whole volume of the device, meaning that smaller devices have a smaller thermal capacitance.

C. Measurement methods

There are two main approaches to obtain the parameters related to the SHE, the time domain and the frequency domain. More traditional characterization devices are capable of performing the first, making it more accessible to researchers and hence it is important to improve those methods as much as possible.

Nevertheless, the time domain methods obtain only the thermal resistance, but not the capacitance, and, in addition, it has been shown that even the value of the resistance might be underestimated in some cases [3]. Therefore, measurements in the frequency domain are still necessary in order to allow for a full characterization of the effect and to verify the validity of the resistance first obtained through time methods.

Since this work will focus on an improvement to one of the time domain methods, only this method will be presented here. Further information on the other methods may be found in [3].

The method here presented is known as the pulsed I-V hot chuck, for it is based on obtaining the drain current as a function of the drain voltage of the device at multiple chuck temperatures through pulses short enough in order to avoid the self-heating during the measurement. This method relies on the thermal capacitance, since it ensures that the device may not heat immediately, and therefore ensuring that fast enough measurements will be self-heating free. In addition, a long enough period between measurements must be given, otherwise the device will not have the time to cool, compromising the next measurement.

In this section, the results presented are extracted from [3], where the author used PDSOI nMOSFETs with 400nm BOX, gate length of 240 nm, 15 parallel fingers, each being 4µm wide (therefore, effective width of 60 µm), film thickness of 150 nm, dielectric thickness of 5 nm and channel doping of approximately 10^{18} cm^{-3}. The device are body tied in order to prevent the floating-body effect.

To extract the thermal resistance, firstly one must measure the drain current when short, constant voltage pulses are applied at the gate with a certain the drain voltage. Repeating this procedure for multiple drain currents allows one to obtain the pulsed I-V curve of the device. Then, after obtaining pulsed I-V curves at different temperatures, they are plotted together with a DC I-V curve obtained at room temperature (DC in this case means that the polarization was applied for a long enough time until the device reaches thermal – and therefore electric – equilibrium). Fig. 2 presents those curves.

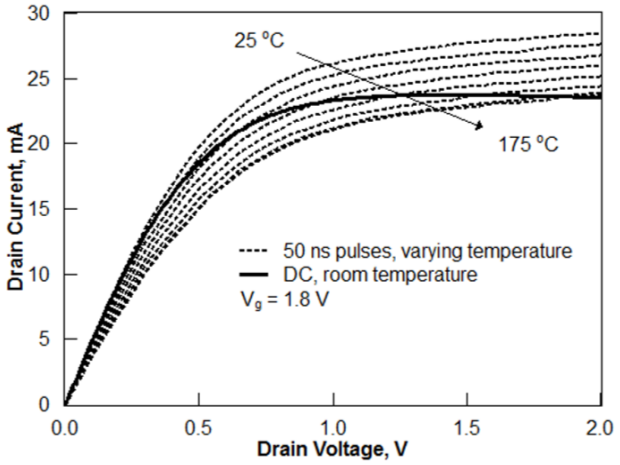

Fig. 2. Drain current versus drain voltage varying temperature with voltage pulses applied to the gate. Source: [3].

From this graph, the channel temperature from the device suffering from the SHE may be induced at some points. The explanation that the current decrease due to the SHE happens only because the carriers' effective mobility decreases implies in the fact that each value for the drain current may be directly related to one and one only channel temperature. Therefore, each point of intersection between the DC measurement and one of the pulsed curves at a certain temperature means that the channel is at such temperature at those polarization conditions.

Finally, the thermal resistance may be calculated as being the slope of the line obtained performing a linear regression with the temperature and power points obtained from the intersections in Fig. 2. Thus, a graph of the temperature as a function of the power applied to the device may be built, as presented in Fig. 3.

One last detail to be observed here is that the linear regression presented in Fig. 3 has a theoretical constraint proposed in [3], forcing the point at room temperature (25°C) to be at zero power. The reasoning for such constraint and its consequences shall be better evaluated in the next session.

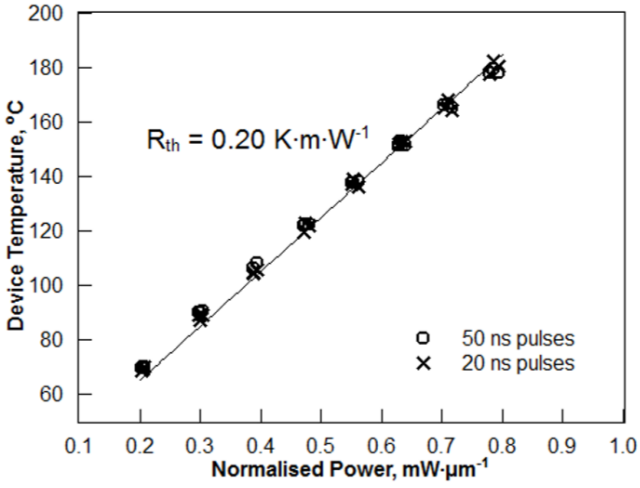

Fig. 3. Device temperature as function of the normalized power to obtain the thermal resistance. Source: [3].

III. An Improvement to the Pulsed I-V Hot Chuck Method

The current method applies a theoretical constraint to the last step, in order to keep the whole process consistent with the linearity of the thermal effects in silicon inside the range of temperatures studied. This means that, for any power level other than zero, the device should heat above the room temperature. However, newer devices fabricated with different geometries and materials may present different results where, although the linear model may still be true, the constraint forcing the point of zero power to room temperature may not apply. As an example, the extraction process with pulses applied to the gate and constant drain voltage is repeated for a different device in Fig. 4 and Fig. 5. This device is an UTBB SOI NMOS with the following dimensions: channel length of 100nm, channel width of 1µm, silicon thickness of 20nm and buried oxide thickness of 10nm.

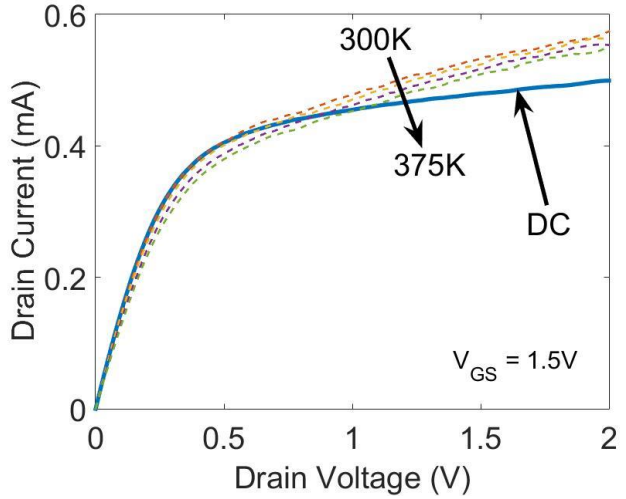

Fig. 4. Drain current versus drain voltage considering DC (room temperature) and pulsed measurements (varying temperature) for a UTBB device

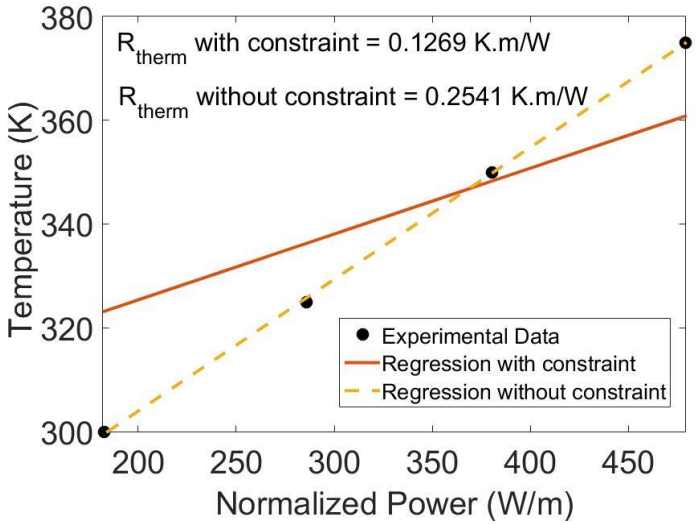

Fig. 5. Obtaining the thermal resistance with and without the theoretical constraint

In Fig. 4 it is clear that the device begins to present the influence of the SHE only after a voltage around 0.5V, meaning that the theoretical constraint should not apply in this case. Indeed, as verified in Fig. 5, keeping the constraint creates a line that is far from well-adjusted to the experimental data. Thus, a new model is proposed, in which the theoretical constraint is discarded and a substitute option is presented: to empirically determine the point where the DC curve separates from the pulsed I-V at room temperature.

The use of this newly proposed method has greatly increased the quality of the linear fit, with its correlation coefficient improving from 0.7217 to 0.9997.

Finally, it is important to note that this new method does not conflict with the older one, since, given the good adjustment observed for the data in older devices, the room temperature point should be close enough to the zero of applied power.

IV. Conclusion

The SHE has become more important in recent years, therefore, fast and efficient methods for its characterization are required. In this work, an improvement is suggested upon one of the traditional characterization methods, generating better results for some devices. Another important characteristic of this improvement is that it provides similar results when compared to the previous version if applied to devices where the theoretical constraint is valid, allowing consistent comparisons between newer measurements and the ones made before the improvement.

References

[1] L. T. Su, J. E. Chung, D. A. Antoniadis, K. E. Goodson and M. I. Flik, "Measurement and modeling of self-heating in SOI nMOSFET's," in IEEE Transactions on Electron Devices, vol. 41, no. 1, pp. 69-75, Jan 1994.

[2] R. H. Tu, C. Wann, J. C. King, P. K. Ko and Chenming Hu, "An AC conductance technique for measuring self-heating in SOI MOSFET's," in IEEE Electron Device Letters, vol. 16, no. 2, pp. 67-69, Feb. 1995.

[3] S. Makojevej, "Characterisation of Thermal and Coupling Effects in Advanced Silicon MOSFETs," Ph.D. dissertation, Sch. of Elect. And Electron. Eng., Newcastle Univ., Newcastle upon Tyne, TWR, 2012

[4] B. M. Tenbroek, M. S. L. Lee, W. Redman-White, J. T. Bunyan and M. J. Uren, "Self-heating effects in SOI MOSFETs and their measurement by small signal conductance techniques," in IEEE Transactions on Electron Devices, vol. 43, no. 12, pp. 2240-2248, Dec 1996.

[5] Colinge, J. P., Silicon-On-Insulator Technology: Materials to VLSI, Kluwer Academic Publishers, NY, 2004.

[6] E. Pop, S. Sinha and K. E. Goodson, "Heat Generation and Transport in Nanometer-Scale Transistors," in Proceedings of the IEEE, vol. 94, no. 8, pp. 1587-1601, Aug. 2006.

[7] J. P-. Raskin, "Silicon-on-insulator (SOI) metal oxide semiconductor field effect transistors (MOSFETs) for radio frequency (RF) and analogue applications", in *Silicon-On-Insulator (SOI) Technology*, ed. O. Kononchuk and B.-Y. Nguyen (Cambridge: Woodhead Publishing, 2014), 275.