A modified Shichman-Hodges model for OTFTs usable in the Quite Universal Circuit Simulator

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***Abstract*—Emergent transistor technologies based on novel electronic materials present a challenge for circuit design. Since these technologies are still under development, extracted transistor parameters and even the required compact transistor models themselves change constantly. Nevertheless, the design of benchmark circuits is needed to demonstrate the advantages and limits that novel electronic materials may offer for electronic applications. We show here that the so called Quite Universal Circuit Simulator (QUCS) offers sufficient flexibility to serve as a design platform for emerging technologies. As a case study we first extracted transistor parameters for an experimentally characterized organic field-effect transistor (OFET) manufactured as top-gate top-contact (TGTC) thin-film transistor (OTFT) employing the well-known Shichman-Hodges (SH) FET model. Second, a smoothing function known from basic junction FET models has been applied to the SH model, combining the linear and saturation regions of the transistor in a single equation. The modified SH model was successfully implemented in QUCS as equation-defined device and as Verilog-A code, demonstrating the possibilities of the circuit simulator. Parameter extraction reveals that the mSH model is better suited for describing the experimental output and transfer characteristics of the selected TGTC OTFT.**

I. Introduction

Organic electronics is a rapidly growing technological field employing the semiconducting properties of small molecules or polymers for realizing light-weight electronics through solution-based manufacturing techniques. Although research on organic electronics has been pursued for a longer period, interest sparked in the 1980s when the performance of organic devices increased significantly [1]. Today organic devices target application areas not easily covered by silicon like sustainable large-area or flexible and wearable electronic devices. Organic field-effect transistors (OFETs) are representative devices that form a basic building block for various microelectronic systems. Compact models for OFETs gain importance as the demand moves from device-level investigation towards circuit-level integration. OFETs are normally realized as thin film devices with the electrical contacts at the bottom or the top of the active layer (top-gate top-contact, top-gate bottom-contact, bottom-gate top-contact or bottom-gate bottom-contact OTFTs). The development of compact transistor models has in recent years profited significantly from the use of equation-defined non-linear functional elements and the use of Verilog-A as the preferred hardware description language for model construction and model interchange between different circuit simulators.

The Quite Universal Circuit Simulator (QUCS) is an open source circuit simulator developed by a group of international scientists and engineers under the GNU General Public License (GPL) [2], [3]. QUCSs release 0.0.11 introduced equation-defined devices (EDD) as a modeling tool allowing to create tailored descriptions of new devices and subroutines [4]. Release 0.0.12 enabled Verilog-A modeling, which has become the standard for device models since it creates high-level behavioral and structural descriptions, encapsulated in easily readable codes [5]. Since the adoption by the QUCS circuit simulation community, EDD and Verilog-A modules of compact device models became an attractive option for non-linear device model development for emerging technologies.

In this paper, we present the implementation of a modified Shichman-Hodges model as equation-defined device and Verilog-A code in QUCS.

II. Methodology

In QUCS, an EDD model is a non-linear component with up to eight branches, and this limit may be increased, if necessary [4]. Algebraic functions of a great number of variables such as voltage, current, admittance and so on can be implemented in a very similar to C-coding environment. Therefore, the user can consider particularities of the device behavior just by creating equations to define or refine the actuation of the corresponding model [6]. A stable EDD model allows interactive development of new non-linear components and a Verilog-A coding helps in the deployment and distribution of the newly developed models. QUCS inherently supports this strategy. Although EDD models are slow, they are very useful in de-bugging and can be easily translated afterwards into a hardware description language. Verilog-A codes are implemented in QUCS using an ADMS compiler and a XML interface [7].

The well-known SH model [8] uses a controlled current source to describe the drain current (I_{D}) as follows:

$$I_{\mathrm{D}} = \beta_p \times \begin{cases} 0 & ; V_{\mathrm{GS}} \leq V_{\mathrm{th}} \\ ((V_{\mathrm{GS}} - V_{\mathrm{th}})V_{\mathrm{DS}} - V_{\mathrm{DS}}^2/2) & ; V_{\mathrm{DS}} \leq V_{\mathrm{GS}} - V_{\mathrm{th}} \\ 0.5\,(V_{\mathrm{GS}} - V_{\mathrm{th}})^2 & ; V_{\mathrm{DS}} \geq V_{\mathrm{GS}} - V_{\mathrm{th}} \end{cases}$$

with

$$\beta_p = K_p \frac{W}{L} (1 + \lambda V_{\mathrm{DS}}) \,. \tag{1}$$

The SH model describes the three operational regions of the FET, cutoff, linear and saturation, by three distinct equations.

TABLE I
EXTRACTED PARAMETERS FOR THE SH AND MSH MODEL. DUE TO HYSTERESIS EFFECTS, PARAMETER VALUES MAY BE EXTRACTED SEPARATELY FOR THE OUTPUT AND TRANSFER CURVES.

Model	Parameter	Value (Transfer)	Value (Output)	Unit
SH/mSH	$LAMDA$	0	0	V^{-1}
SH	VTO	-0.76	-0.76	V
	KP	3.01×10^{-8}	3.01×10^{-8}	$\mathrm{A\,V}^{-2}$
	RS	1×10^{3}	1×10^{3}	Ω
	RD	1×10^{3}	1×10^{3}	Ω
	LD	5.5×10^{-5}	5.5×10^{-5}	cm
mSH	VTO	-0.74	-0.76	V
	KP	1.82×10^{-8}	1.54×10^{-8}	AV^{-n}
	α	2	2.3	-
	n	2.32	2	-
	RS	0	0	Ω
	RD	0	0	Ω
	LD	0	0	cm

The mSH model combines the linear and saturation regions into a single equation giving a smoother transition compared to the original model, which predicts a more abrupt switch-over. The new equation describes the current using basically the same parameters, but with the elegant adding of a hyperbolic tangent, as follows:

$$I_{\mathrm{D}} = \beta_p \, |V_{\mathrm{th}}|^n \left(1 - \frac{V_{\mathrm{GS}}}{V_{\mathrm{th}}}\right)^n \left|\tanh\left(\frac{\alpha V_{\mathrm{DS}}}{V_{\mathrm{th}} - V_{\mathrm{GS}}}\right)\right| . \quad (2)$$

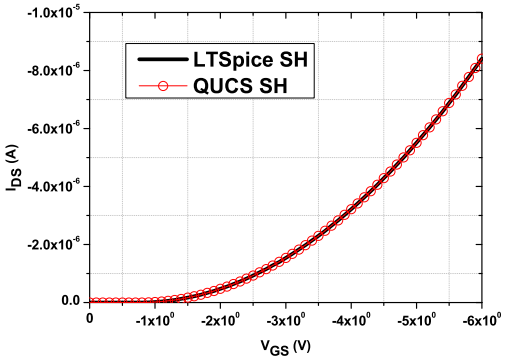
The additional mathematical parameters n and α adjust the linear-to-saturation transition. For small V_{DS} the hyperbolic tangent turns into a linear function describing the linear operation region of the FET, the parameter α describing basically the inclination. For large arguments, i.e. in the saturation region, the hyperbolic tangent approaches one and the only V_{DS} dependence stems from the channel modulation included in β_p as in the original SH model. A sub threshold current is not included in the mSH model, i.e. $I_{\mathrm{D}} = 0$ for $V_{\mathrm{GS}} \leq V_{\mathrm{th}}$.

Even though the described smoothing function is well known in the literature, it should be noted that a corresponding model is not readily available in QUCS. Therefore, the given modification serves as an example of demonstrating the flexibility of QUCS in implementing new or modified models. Moreover, the mSH model is a useful addition to the model library for describing organic thin-film transistors.

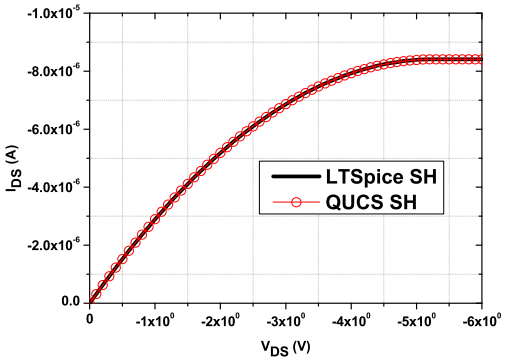
Aside from the in-house development of compact models for emergent transistor technologies, it is interesting to implement models described in the literature to compare and test their validity for a given characterized transistor. QUCS is an ideal platform since the implementation as EDD or Verilog-A code is readily available. We have implemented and tested several compact models, both for organic thin-film transistors, like UMEM and MVS [9], [10], and for carbon nanotube based technologies, like CCAM [11], [12].

III. RESULTS

Experimental transfer and output characteristics were provided by the Chair for Electron Devices and Integrated Circuits (CEDIC) hosted by the Technische Universität Dresden



(a)

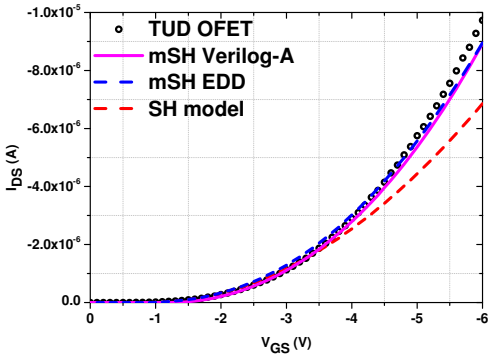


(b)

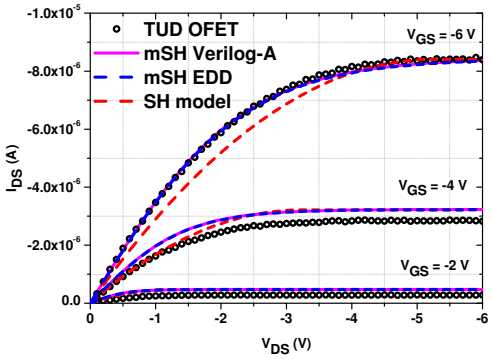
Fig. 1. Comparison of two different circuit simulators (LTSpice and QUCS) employing a SH model with identical model parameters: (a) Transfer curve for $V_{\mathrm{DS}} = -6\,\mathrm{V}$ and (b) Output curve for $V_{\mathrm{GS}} = -6\,\mathrm{V}$.

(TUD), Germany. An organic thin-film transistor with a channel length of $L = 50\,\mu\mathrm{m}$ and a gate width of $W = 1000\,\mu\mathrm{m}$ has been electrically characterized. Source and drain contacts as well as the gate contact were positioned at the top of the device (TGTC OTFT). We extracted the parameters of a standard SH FET model based on the provided experimental output and transfer characteristics. The determined parameter values are given in Tab. I. Two sets of parameters are necessary to describe the transfer and output curve separately. The reason are hysteresis effects, common for emergent technologies, which lead to a different drain current for the same bias point depending on the sequence of ramping the voltages. As common in parameter extraction, we allow for an effective value for the channel length given by $L_{\mathrm{eff}} = L - L_{\mathrm{D}}$. Since contact resistance values are high in organic devices, a source R_{S} and drain R_{D} resistance is included in the model. Therefore, internal and external voltages are related via $V_{\mathrm{DS}} = V'_{\mathrm{DS}} + I_{\mathrm{D}}(R_{\mathrm{S}} + R_{\mathrm{D}})$ and $V_{\mathrm{GS}} = V'_{\mathrm{GS}} + I_{\mathrm{D}} R_{\mathrm{S}}$.

LTSpice was chosen as the first circuit simulator to extract the transistor parameters. The tool is designed by Linear Technology Corporation and can be found at http://www.linear.com/designtools/software/. LTSpice is a professional tool for circuit design. Even though LTSpice is an excellent circuit sim-



(a)



(b)

Fig. 2. Comparison of measured electrical characteristics of a TGTC OTFT with simulations employing a SH and mSH model: (a) Transfer curve for $V_{\mathrm{DS}} = -6\,\mathrm{V}$ and (b) Output curve for $V_{\mathrm{GS}} = -6\,\mathrm{V}$, $-4\,\mathrm{V}$ and $-2\,\mathrm{V}$. Note that for example at the bias point $V_{\mathrm{DS}} = V_{\mathrm{GS}} = -6\,\mathrm{V}$ the drain current differs for the transfer and output characteristic due to hysteresis effects.

ulator, we employed the platform only to benchmark QUCS as we are interested in the EDD and Verilog-A-like modeling features of the latter. We compared the electrical transistor characteristics obtained by the two circuit simulators in Fig. 1 using the parameter values given in Tab. I. As expected no difference between the circuit simulators could be revealed.

The comparison between the SH model and the measured transistor characteristics turned out to be unsatisfactory. After implementing the mSH model as described in the previous section, we re-extracted the model parameters, this time for the modified model version. The extracted model parameter values are in Tab. I including the two transition parameters α and n. It should be noted that the definition of K_p differs by a factor of two in the two models. We compare the experimental data with the SH and mSH model in Fig. 2. As can be seen, the fitting quality has improved considerably when applying the smoothing function which improves the linear-to-saturation crossover.

IV. Conclusion

We extracted model parameters for a SH and modified SH model based on the DC characteristics of a top-gate top-contact organic thin-film transistor. The mSH model improves the linear-to-saturation crossover by substituting the square-law behavior of the SH model by an hyperbolic tangent, providing an additional parameter to adjust the low-bias channel conductance independent of the saturation behavior. The mSH model was implemented as equation-defined device and as Verilog-A code in the Quite Universal Circuit Simulator. Although the employed TGTC OTFT represent a long channel device with a channel length of $L = 50\,\mu\mathrm{m}$, the fitting quality of the SH model could be improved considerably by the introduction of the smoothing function. The given case study of a model parameter extraction underlines the need of simple and fast model adaptation when calibrating compact models for emergent technologies. In this respect, QUCS proved to be a promising design-platform for benchmark circuits for technologies under continuous development.

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