# Analysis and Design of Ultra Low Voltage Dickson Charge Pumps

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*Abstract*—From the need of DC-DC converters applied to energy harvesting systems, this paper presents the modeling and design of a Dickson charge pump focused on ultra-low-voltages. In order to prove the accuracy of the model, three designs were implemented, two of them using off-the-shelf Schottky diodes and a third, fully integrated, using zero-VT transistors of the IBM 130 nm technology.

*Keywords — energy harvesting; Dickson charge pump; ultra-low-voltages; ultra-low-power.*

## I. INTRODUCTION

The necessity of energy autonomy devices in wireless sensors and biomedical applications has increased in the last decades. These devices may have different sources of energy, as heat, light, motion or even glucose from human body. So, it is necessary the development of ways of transfer between energy captured and destination circuits.

It is known that some of the sources of ultra-low-voltage usually provide DC voltages below 100 mV [1], [2]; thus, sometimes the increase of the voltage from some tens of mV to 1 V is required for the operation of some of the current integrated circuits [2]. Among these sources, we mention the photovoltaic cells operating in low-light environments; thermoelectric generators, which operate from temperature differences between human skin and the environment; and fuel cells, which capture energy from glucose in the human body [3]. Thermoelectric generators attached to the human body rarely provide voltages over 100 mV [4]. Still, in certain cases, these voltages may be below the thermal voltage $kT/q$, which is around 26 mV at room temperature [5].

Figure 1 shows a typical system for energy harvesting. For the step-up stage, different circuit topologies may be used [6], namely inductive boost or charge pump converters. The charge pump converters, in general, present less passive losses; this feature allows them to be applied in circuits with input voltages of less than 100 mV and they do not require wide oscillation amplitude signals [7], [8]. From this perspective, this paper presents the modeling of the Dickson charge pump for ultra-low-voltage applications.
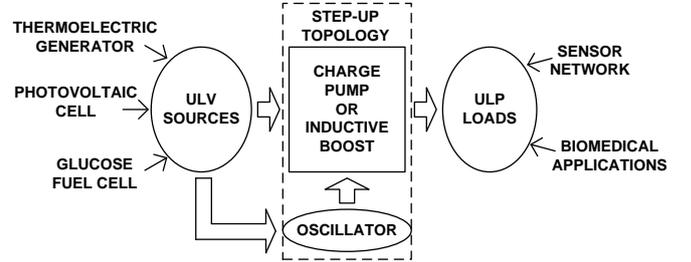


Fig. 1. The conceptualization of an ULV step-up topology.

## II. ANALYSIS OF THE ULV DICKSON CHARGE PUMP

Figure 2 presents a Dickson charge pump schematic along with the voltage drops across the diodes for square wave complementary clocks. The conventional Dickson charge pump model cannot be applied to ultra-low-voltage clocks, since it assumes the diodes voltage drops, $V_D$ to be constant. This assumption is not valid since $V_D$ is dependent on the load current $I_L$ [2].

To analyze the Dickson converter down to input voltages of the order of 100 mV or even less, we introduce a converter model which includes both the load current and the more realistic exponential current-voltage characteristic of the diode.
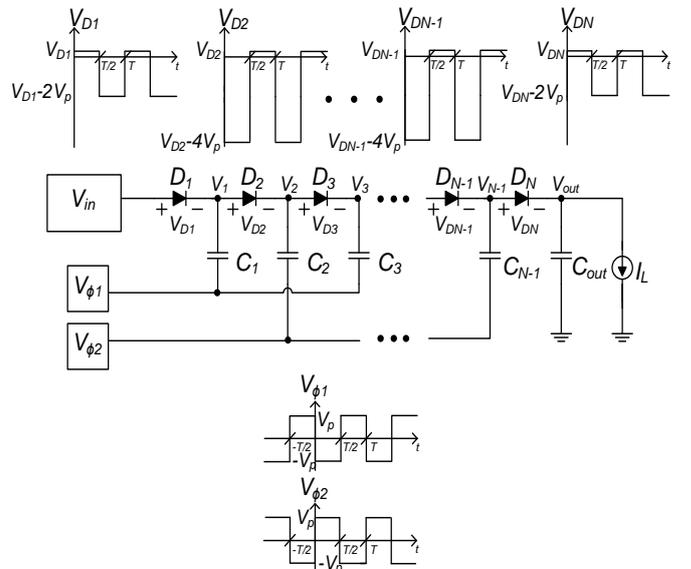


Fig. 2. Dickson charge pump topology.

For the N-stage Dickson converter, assuming steady-state operation as in [9], and, for the sake of simplicity, square signals $V_{\phi 1}$ and $V_{\phi 2}$, the voltage waveform $V_D$ across each diode of the circuit is also shown in Fig. 2, where $V_{DN}$ is the $N^{th}$-diode forward voltage drop and $V_p$ is the peak voltage of $V_{\phi 1}$ and $V_{\phi 2}$. As can be seen in Fig. 2, one of the terminals of both the leftmost and rightmost diodes, $D_1$ and $D_N$ is connected to DC nodes ($V_{in}$ and $V_{out}$, respectively). The voltage across them is the same $V_{D_1} = V_{D_N}$, but differ from the voltage drops across the intermediate diodes. For the other diodes, $D_2$ to $D_{N-1}$, the forward voltage drop will be the same ($V_{D_2} = V_{D_{N-1}}$). Thus, the DC output voltage of the converter is

$$V_{out} = V_{in} + (N-1)2V_p - 2V_{D_1} - (N-2)V_{D_2} \qquad (1)$$

Considering that the average current through each diode during full cycle of $V_{\phi 1}$ and $V_{\phi 2}$ is equal to load current, we have

$$I_L = \frac{1}{T}\int_{-T/2}^{T/2} I_D \, dt \qquad (2)$$

The diode current is given by (3), known as Shockley equation.

$$I_D = I_{sat}\left(e^{\frac{V_D}{nV_t}} - 1\right) \qquad (3)$$

where $V_t$ is the thermal voltage, $I_{sat}$ is the saturation current reverse and $n$ is the diode ideality factor [6].

Substituting (3) into (2) and assuming that the capacitors values are sufficiently high to keep the voltages at each node constant over a half-cycle, yields (4) and (5), which can be solved for the forward voltage drops $V_{D_1}$ and $V_{D_2}$.

$$I_L = \frac{1}{T}\left[\int_{-\frac{T}{2}}^{0} I_{sat}\left(e^{\frac{V_{D_1}-2V_p}{nV_t}} - 1\right)dt + \int_{0}^{\frac{T}{2}} I_{sat}\left(e^{\frac{V_{D_1}}{nV_t}} - 1\right)dt\right] \qquad (4)$$

$$I_L = \frac{1}{T}\left[\int_{-\frac{T}{2}}^{0} I_{sat}\left(e^{\frac{V_{D_2}}{nV_t}} - 1\right)dt + \int_{0}^{\frac{T}{2}} I_{sat}\left(e^{\frac{V_{D_2}-4V_p}{nV_t}} - 1\right)dt\right] \qquad (5)$$

$$V_{D_1} = V_p - nV_t \ln\left[\frac{\cosh\left(\frac{V_p}{nV_t}\right)}{1 + \frac{I_L}{I_{sat}}}\right] \qquad (6)$$

$$V_{D_2} = 2V_p - nV_t \ln\left[\frac{\cosh\left(\frac{2V_p}{nV_t}\right)}{1 + \frac{I_L}{I_{sat}}}\right] \qquad (7)$$

### A. Output Voltage

Substituting (6) and (7) into (1), we obtain (8), the expression for the output voltage of the Dickson converter modeled for any voltage, including the ultra-low-voltage range. To test the accuracy of the model, a set of curves obtained from (8) using several values of $N$ is shown in Fig. 3 in terms of $I_L/I_{sat}$,. The symbols represent $V_{out}$ obtained from simulation, under the same conditions of equation (8).
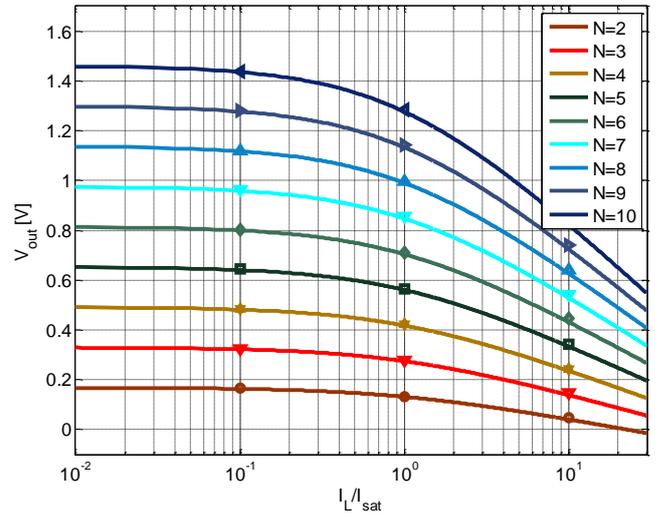


Fig. 3. Calculated (solid lines) and simulated (symbols) output voltage ($V_{out}$) vs. the load current normalized to the saturation current ($I_L/I_{sat}$), for $N$ ranging from 2 to 10, $V_{in} = 25$ mV, $V_p = 90$ mV and $n = 1.0345$.

$$V_{out} = V_{in} + 2nV_t \ln\left[\frac{\cosh\left(\frac{V_p}{nV_t}\right)}{1 + \frac{I_L}{I_{sat}}}\right] + (N-2)nV_t \ln\left[\frac{\cosh\left(\frac{2V_p}{nV_t}\right)}{1 + \frac{I_L}{I_{sat}}}\right] \qquad (8)$$

### B. Power Converter Efficiency (PCE)

One important figure of merit of a converter is its *PCE*, which is the fraction of the input power transferred to the load. By definition,

$$PCE = \frac{P_{out}}{P_{in}} \qquad (9)$$

The output power, $P_{out}$, is the product of $V_{out}$ e $I_L$, while the input power, $P_{in}$, is the addition of $P_{out}$ and power loss, $P_{loss}$. The power loss is the power dissipated in the diodes; thus, we can rewrite (9) as

$$PCE = \frac{P_{out}}{P_{out} + P_{loss}} \qquad (10)$$

where

$$P_{loss} = 2P_{D_1} + (N-2)P_{D_2} \qquad (11)$$

The values of $P_{D_1}$ e $P_{D_2}$ are given by

$$P_{D_1} = \frac{1}{T}\int_{-\frac{T}{2}}^{\frac{T}{2}} V_{D_1}I_{sat}\left(e^{\frac{V_{D_1}}{nV_t}} - 1\right)dt \qquad (12)$$

$$P_{D_2} = \frac{1}{T}\int_{-\frac{T}{2}}^{\frac{T}{2}} V_{D_2}I_{sat}\left(e^{\frac{V_{D_2}}{nV_t}} - 1\right)dt \qquad (13)$$

Solving the integrals, we find that

$$P_{D_1} = (I_{sat} + I_L)V_p \tanh\left(\frac{V_p}{nV_t}\right) - I_L nV_t \ln\left[\frac{\cosh\left(\frac{V_p}{nV_t}\right)}{1 + \frac{I_L}{I_{sat}}}\right] \qquad (14)$$

$$P_{D_2} = (I_{sat} + I_L)2V_p \tanh\left(\frac{2V_p}{nV_t}\right) - I_L nV_t \ln\left[\frac{cosh\left(\frac{2V_p}{nV_t}\right)}{1 + \frac{I_L}{I_{sat}}}\right] \quad (15)$$

Finally, replacing (14), (15), and (11) into (10) yields

$PCE =$

$$\frac{V_{in} + 2nV_t \ln\left(\frac{cosh\left(\frac{V_p}{nV_t}\right)}{1 + \frac{I_L}{I_{sat}}}\right) + (N-2)nV_t ln\left(\frac{cosh\left(\frac{2V_p}{nV_t}\right)}{1 + \frac{I_L}{I_{sat}}}\right)}{V_{in} + \left(1 + \frac{I_L}{I_{sat}}\right)2V_p\left[\tanh\left(\frac{V_p}{nV_t}\right) + (N-2)\tanh\left(\frac{2V_p}{nV_t}\right)\right]} \quad (16)$$

## III. RIPPLE ANALYSIS

The ripple analysis is required for properly calculating the capacitors values used in the converter.

Assuming steady state analysis, the output voltage ripple can be calculated in analogy with the half-wave rectifier shown in Fig. 4. Upon discharge of the capacitor, by the Kirchhoff's current law it is known that

$$I_C = -(I_L + I_{sat}) \quad (17)$$

Note that the current leakage ($I_{sat}$) in the reverse-biased diode has been included in (17). Since the capacitor voltage is given by

$$V_C(t) = V(0) + \frac{1}{C}\int_0^t I_C dt \quad (18)$$

and that, at $t = T/2$, $V_C$ is equal to $V_{out}$, replacing (17) into (18), we have

$$V_C(T) = V_{out} - \frac{1}{C}\int_{\frac{T}{2}}^T (I_L + I_{sat})dt = V_{out} - \frac{(I_L + I_{sat})T}{2C} \quad (19)$$

Thus, $V_{Ripple}$ is given by

$$V_{Ripple} = V_{out} - V_C(T) = \frac{(I_L + I_{sat})T}{2C} \quad (20)$$

The capacitance value required for having a ripple voltage of less than $V_{Ripple}$ is

$$C > \frac{(I_L + I_{sat})T}{2V_{Ripple}} \quad (21)$$
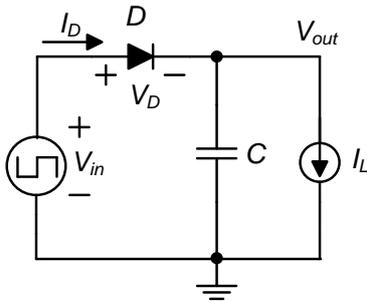


Fig. 4. Half-wave rectifier.

A high value of $C$ has two disadvantages; the first one is area consumption, whereas the second one is a high settling time. The transient analysis of the Dickson charge pump, which is required for the calculation of the settling time, is beyond the scope of this work.

## IV. THE OFF-THE-SHELF PROTOTYPES

Using the values of $I_{sat}$ and $n$ extracted for commercial Schottky diodes, we designed two off-the-shelf converters to supply ultra-low-power loads.

In the first converter, using the framework presented in Section II, with $I_L = 1$ µA, we reached the values of $V_{out} = 1$ V from values of $V_{in} = 10$ mV, $V_p = 80$ mV, and $N = 9$, thereby providing output power close to 1 µW. In this converter we used the Schottky diode MBR1545CT, with $I_{sat}$ and $n$ around 2 µA e 1, respectively.

In the second converter, from $V_{in} = 30$ mV, $V_p = 155$ mV, and $N = 14$, we achieved $V_{out} = 2$ V for $I_L = 100$ µA. Thus, the output power provided by this converter is approximately 200 µW. In this converter we used the Schottky diode 1N5819, with $I_{sat}$ and $n$ about 760 nA e 1, respectively.

With maximum ripple set at 2% and frequency $V_{\phi 1}$ and $V_{\phi 2}$ at 100 kHz, the calculated capacitances were 1.6 nF for the first converter and 260 nF for the second one. For the prototypes we used capacitors of 2.2 nF and 470 nF, respectively.
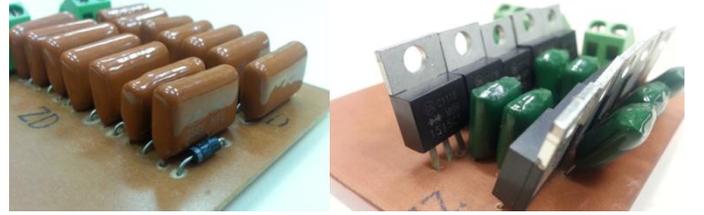


Fig. 5. Off-the-shelf prototypes.
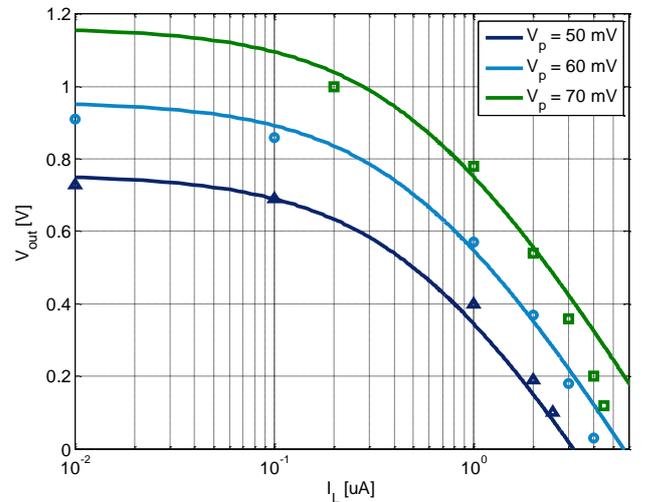


Fig. 6. Calculated (lines) and experimental (symbols) output voltage of the integrated converter in terms of the load current for $I_{sat} = 550$ nA, $N = 11$, $n = 1.4$ and $V_p = 2V_{in}$.

## V. THE FULLY-INTEGRATED PROTOTYPE

The integrated converter has been implemented in the IBM 130 nm CMOS technology using zero-VT transistors connected as diodes. The experimental results are shown in Fig. 6. In this case, the value of $I_{sat}$ could be designed according to the aspect ratio $W/L$ of the transistors. With an 11-stage converter and $I_{sat} = 550$ nA, values of output voltage equal to 1 V and load current equal to 200 nA were obtained from $V_{in} = 35$ mV and $V_p = 70$ mV. For a reverse saturation current of 550 nA, we have $W/L$ equal to 10, with $L = 0.42$ μm and $W = 4.2$ μm.

The clock frequency of the integrated converter is 550 MHz, resulting in capacitances of 2 pF for a peak-to-peak ripple voltage of around 100 mV.

## VI. CONCLUSIONS

The Dickson converter model for ultra-low-voltages, taking into account the voltage drop in the diodes was verified through three prototypes, two of them with off-the-shelf components and a third one which is fully integrated.
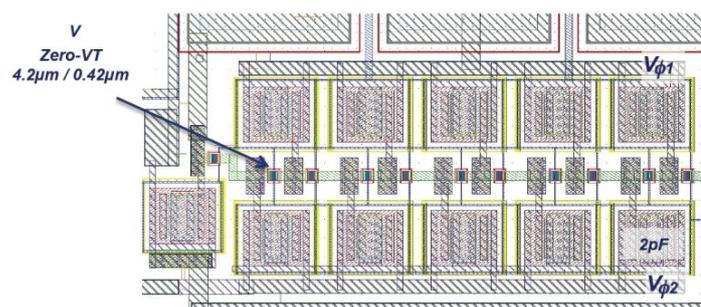


Fig. 7. Layout of the 11-stage Dickson converter designed in the 130 nm technology.

With the development of the prototypes, the model for ultra-low-voltages of the Dickson converter has been validated according with the simulations. As can be seen in Table II, the differences found between the results of the prototype and provided by the developed model are considerably small, thus validating the model presented in this paper.

TABLE I.  RESULTS OBTAINED IN THE PROTOTYPES

| Variable | Prototype | | |
|---|---|---|---|
| | Fully-Integrated | Off-the-Shelf nº 1 | Off-the-Shelf nº 2 |
| $V_{out}$ (V) | 1.01 | 0.9493 | 2.0151 |
| $I_L$ (μA) | 0.2 | 0.930 | 102.81 |
| $V_{in}$ (mV) | 35 | 10.045 | 30.047 |
| $V_p$ (mV) | 70 | 80 | 155 |
| $N$ | 11 | 9 | 14 |
| $n$ | 1.4 | 1.05 | 1.04 |
| $I_{sat}$ (nA) | 550 | 2062 | 765 |

TABLE II.  COMPARISON BETWEEN CALCULATED AND EXPERIMENTAL RESULTS OBTAINED IN OFF-THE-SHELF AND FULLY-INTEGRATED PROTOTYPES

| Result | Prototype | | | | | |
|---|---|---|---|---|---|---|
| | Fully-Integrated | | Off-the-Shelf nº 1 | | Off-the-Shelf nº 2 | |
| | $V_{out}$ (V) | $I_L$ (μA) | $V_{out}$ (V) | $I_L$ (μA) | $V_{out}$ (V) | $I_L$ (μA) |
| Calculated | 1.04 | 0.2 | 1.02 | 1 | 1.96 | 100 |
| Experimental | 1.01 | 0.2 | 0.95 | 0.93 | 2.01 | 102.8 |
| Difference | 0.03 | 0 | 0.07 | 0.07 | -0.05 | -2.8 |

## REFERENCES

[1] Bender Machado, Marcio, et al. "Fully-integrated 86 mV–1V step-up converter for energy harvesting applications." *New Circuits and Systems Conference (NEWCAS), 2014 IEEE 12th International*. IEEE, 2014.

[2] Machado, Marcio Bender, et al. "10 mV: 1V Step-up Converter for Energy Harvesting Applications." *Proceedings of the 27th Symposium on Integrated Circuits and Systems Design*. ACM, 2014.

[3] Rapoport, Benjamin I., Jakub T. Kedzierski, and Rahul Sarpeshkar. "A glucose fuel cell for implantable brain–machine interfaces." *PloS one* 7.6 (2012): e38436.

[4] Chen, Po-Hung, et al. "Startup techniques for 95 mV step-up converter by capacitor pass-on scheme and-tuned oscillator with fixed charge programming." *Solid-State Circuits, IEEE Journal of* 47.5 (2012): 1252-1260.

[5] Sedra, Adel S., and Kenneth Carless Smith. *Microeletrônica*. Pearson Prentice Hall, 2007.

[6] Richelli, Anna, Simone Comensoli, and Zsolt M. Kovács-Vajna. "A DC/DC boosting technique and power management for ultralow-voltage energy harvesting applications." *Industrial Electronics, IEEE Transactions on* 59.6 (2012): 2701-2708.

[7] Pan, Feng, and Tapan Samaddar. *Charge pump circuit design*. McGraw Hill Professional, 2010.

[8] Richelli, A., et al. "A fully integrated inductor-based 1.8-6-V step-up converter." *Solid-State Circuits, IEEE Journal of* 39.1 (2004): 242-245.

[9] Cardoso, Adilson J., et al. "Analysis of the rectifier circuit valid down to its low-voltage limit." *Circuits and Systems I: Regular Papers, IEEE Transactions on* 59.1 (2012): 106-112.