Simulation and Electrical Caraterization of Fully Depleted SOI MOSFETs with 10 nm Thick Silicon Layer

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***Abstract*— This work presents the electrical characteristics of FD SOI MOSFETs made in a 10 nm thick silicon film through bidimensional numerical simulations and experimental measurements. Threshold voltage, subthreshold slope, maximum transconductance, carrier mobility, DIBL and on/off current ratio have been extracted. Finally, an analysis on the gate current is made, considering tunneling models for simulation, and the results were compared to the experimental measures.**

Keywords—Electrical Measurement; Simulation; SOI MOSFET; Nanoelectronics.

I. INTRODUCTION

The Silicon-on-Insulator (SOI) MOS Field Effect Transistor is one of the usual examples of Ultra Large Scale of Integration (ULSI) devices used for reduction of Short Channel Effects (SCE's) due to shorter dimensions. Such devices consist in separating the active part of the transistor from the substrate through a silicon oxide layer (buried oxide) [1], providing intrinsic dielectrical insulation. The structure of a SOI nMOSFET is shown in Fig. 1, where the thickness of the silicon layer (t_{si}), the thickness of the buried oxide (t_{ox}) and the channel length (L) are indicated.

The dimensions of the silicon layer define the type of SOI transistor, being the Fully Depleted, where the thickness of the silicon layer is smaller than the depletion layer width, the one with the most interesting performance properties [2]. Several improvements can be noticed in the use of FDSOI transistors, such as a reduced electrical field and parasitic capacitances, parasitic thyristor supression on CMOS structures and higher transconductance.

The processing of CMOS SOI devices, and more specifically fully depleted SOI devices is simpler than that of bulk CMOS as there's no need of creating wells.

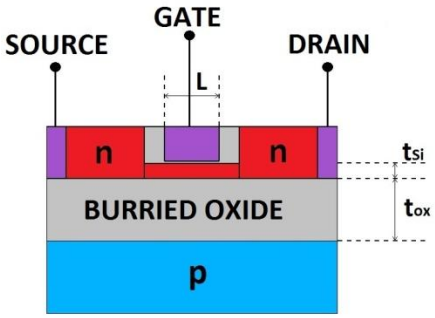


Fig 1. Longitudinal section of a SOI nMOSFET.

When the silicon layer thickness is reduced to 20 nm or below (ultrathin SOI devices), the short channel effects such as DIBL (Drain Induced Barrier Lowering) are even more reduced. However, several effects related to band structure modification appear when these layers are implemented, resulting in a larger silicon bandgap [2]. Also, in these transistors, due to the gate oxide being thinner, gate tunneling effects are seen. In n-MOSFETs, gate biasing can make the substrate's valence band energy level and the gate's polysilicon conduction band level be the same. This leads to electron tunneling from the substrate to the gate [3]. This can result in gate leakage current, that depends exponentialy on the oxide thickness, witch could make it the dominant leakage mechanism, deteriorate the device's reliability and raise it's power consumption [4]. Also, Electron Valence Band (EVB) tunneling may result in holes being left in the substrate, constituting a substrate current [3].

II. DEVICE STRUCTURE AND METHODOLOGY

The devices used for the electrical mesurement were FD SOI transistors fabricated, with 10 nm of Silicon layer thickness and 1.7 nm of gate oxide, varying the channel length from 250 nm to 3 µm and the channel width from 10 µm to 1 µm. The transistors' dimensions are shown in Table I. The gate insulator is silicon oxynitride and the gate metal is n-type polysilicon.

TABLE I. STUDIED FD SOI MOSFETS' DIMENSIONS

Transistor	W (µm)	L (nm)
1	10	250
2	10	500
3	10	700
4	10	1000
5	10	3000
6	1	1000
7	3	1000
8	3	3000

These devices were fabricated in the Interuniversity Microelectronics Center (imec) in Belgium, and were measured with the equipments Keithley 4200 semiconductor parameter analyzer and a Cascade microprover REL 3600.

A. Numerical Bidimensional Simulations

The simulations were made in Silvaco's Atlas Simulator [5]. Devices with similar characteristics as the ones used for the electrical characterization were simulated, having $3x10^{16}$ cm^{-3} p-type channel doping concentration and $5x10^{20}$ cm^{-3} n-type source and drain doping concentration, but different values were used for channel length, varying from 50 nm to 1 µm.

As a result from these simulations, a series of $I_D x V_{GS}$ curves were obtained as well, when it was biased 50 mV and 1.5 V in the drain, and $-0.5 \leq V_{GS} \leq 1.2$ V in the gate. In the simulations that included gate current, tunneling models such as Fowler-Nordheim Tunneling Current, Band-to-Band Tunneling, Hot Electrons and Hot Holes were included on simulation files. In this case, the drain was biased with 1 V.

III. RESULTS AND DISCUSSION

A. Simulation Results

The drain current for all the simulated devices with 50 mV of drain voltage is presented in Fig. 2. It can be noticed a raise on current flow for shorter channel length transistors.

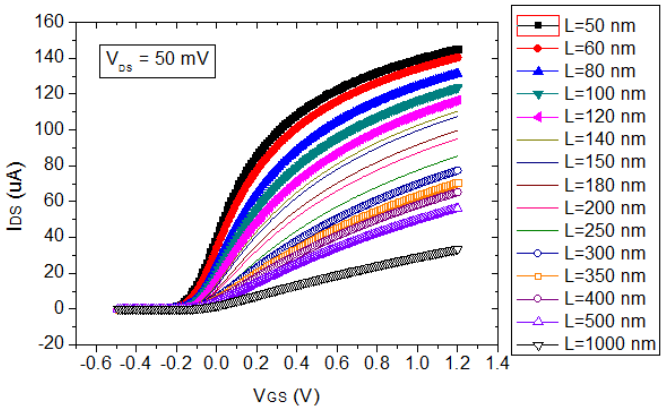


Fig 2. Drain current as a function of gate voltage for different channel length transistors, with 50 mV of drain voltage biasing.

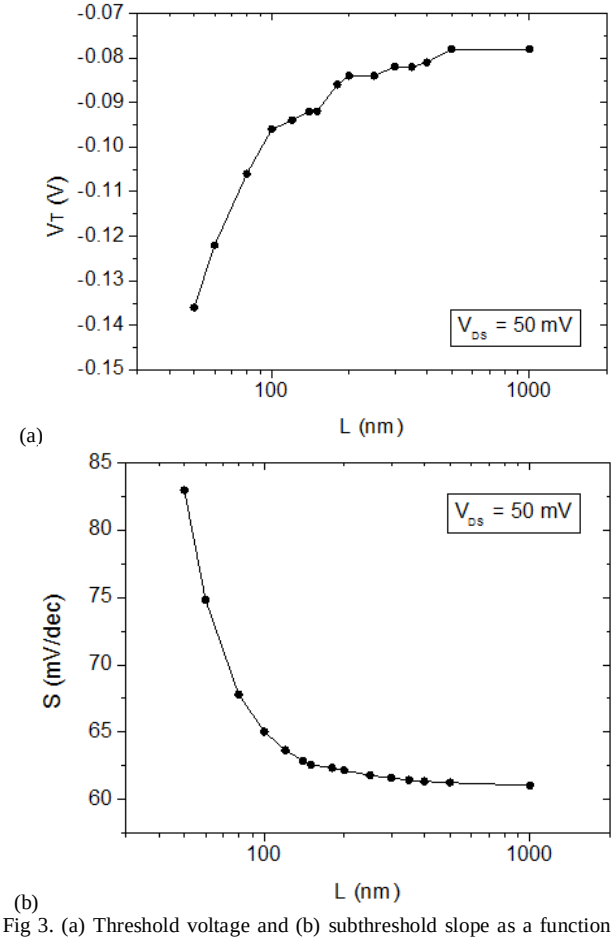


Fig 3. (a) Threshold voltage and (b) subthreshold slope as a function of channel length.

The threshold voltage was extracted through the Second-Derivative method [6], and the subthreshold slope was obtained by inverting the derivate of the drain current logarithm. The results are shown in Fig. 3, where it can be seen a stability in the threshold voltage for most channel lengths, with a reduction on shorter channel lengths, as well as in the subthreshold slope, where most devices present value close to the theoretical value of 60 mV/dec. Because of the gate material workfunction, all n-type SOI MOSFETs present negative threshold voltages. Assuming a maximum degradation of 10% for the threshold voltage and subthreshold slope, the minimum L that is not suffering from SCEs is 140 nm.

For maximum transconductance, the peak value of drain current derivate as a function of gate voltage was considered. Given that the equation for transconductance is a function of channel length and carrier mobility, the transconductance-channel length product curve indicates the variation of carrier mobility with channel length.

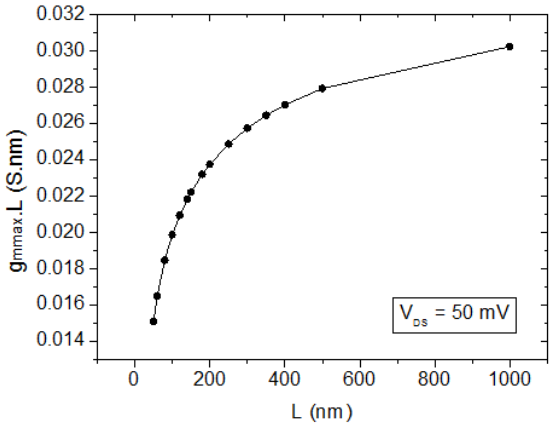


Fig 4. Transconductance-channel length product versus channel length.

As shown in Fig. 4, mobility also decreases as channel length is reduced when a thin SOI layer is used, as it happens in buk CMOS transistors and thicker SOI MOS, where carrier mobility degradation is seen for short channel devices. This degradation is explained by the raise on the lateral electric field, and the of the subthreshold slope raises in shorter transistors due to short channel effects (SCE).

With the simulations of 1.5 V drain voltage biasing, DIBL was calculated using 50 mV and this value of drain voltage, with their respective threshold voltage results for a reference drain current. The obtained DIBL values for each simulated device are indicated in Fig. 5. The barrier lowering causes a threshold voltage reduction when drain voltage is raised. This barrier lowering is caused by the interaction between depletion regions of source and drain, enabling drain voltage to lower the source-substrate PN Junction's voltage barrier.

On-off current ratio was also calculated when 1.5 V was applied to the drain. For this calculation, the curves of drain current as a function of gate voltage minus threshold voltage (V_{GS}-V_T) were obtained, and the current values, where this subtraction was -300 mV and 1 V were defined, respectively, as off-current and on-current. Off current suffers a raise for shorter devices, meaning a higher current takes place when the transistor is not operating, and thus lowering the on/off currente ratio curve.

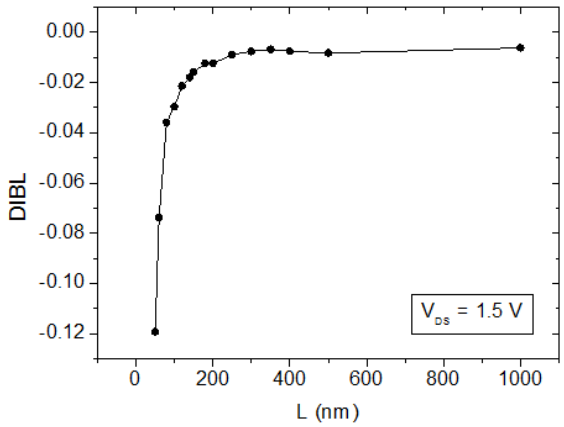


Fig 5. Drain Induced Barrier Lowering as a function of channel length.

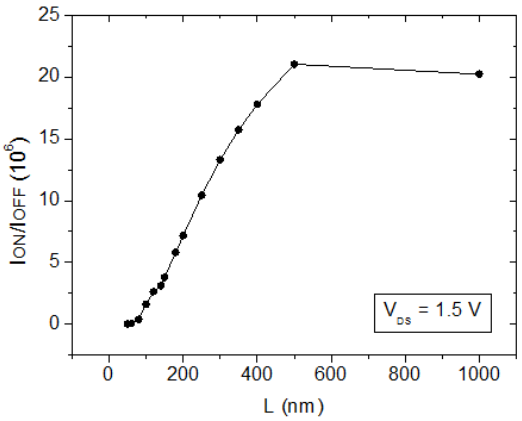


Fig 6. On/off current ratio as a function of channel length.

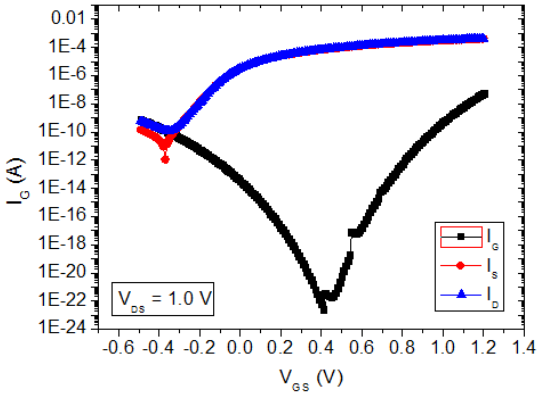


Fig 7. Gate, source and drain current as a function of gate voltage for a 1 µm channel length transistor when considering gate tunneling models.

The influence of transistor's gate current can be noticed in Fig. 7, where 1 V of drain voltage was biased on a 1 µm channel length transistor. One can notice that gate current only has a significant value when low V_{GS} is applied. Also, there is a raise on gate current when there are higher absolute values of gate voltage in the transistor. This is probably due to Hot Electron Effect, because the electrons acceleration by high electric field may be enough to surpass the oxide layer and reach the gate electrode.

For that reason, for the electrical parameters analyzed in the previous simulations, little difference was noticed on their behavior when adding gate current tunneling models. The simulations showed that the results were similar to the ones seen previously, witch means they weren't affected by gate current.

B. Experimental Results

Drain current was extracted as a function of gate voltage, where it can be seen in Fig. 9 that this current raises as channel length is shortened. In addition, channel width shortening causes a reduction on the drain current. This is in accordance with drain current equations. The same method as the one used in simulations was used to obtain the threshold voltage of the transistors. The values, presented in Fig. 11(a), are similar to the ones seen on simulation, when considering 10 µm of channel width.

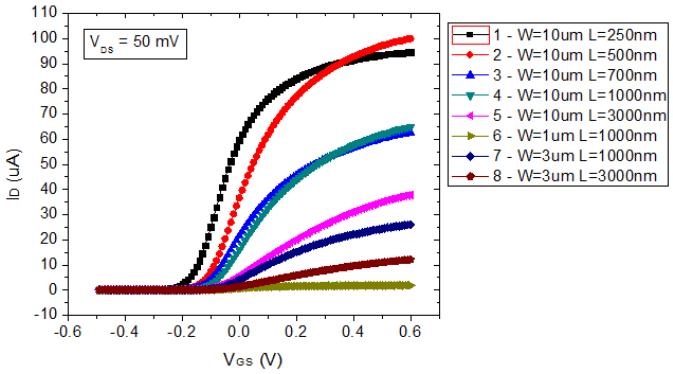
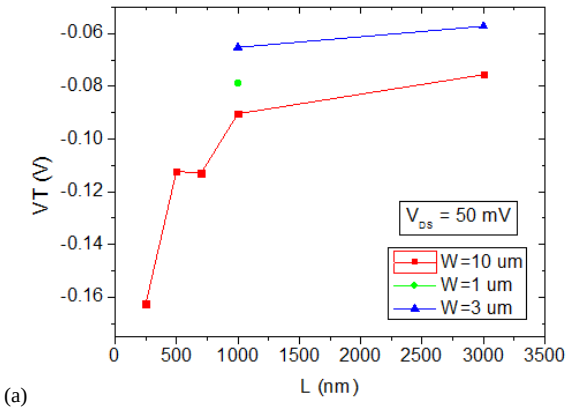
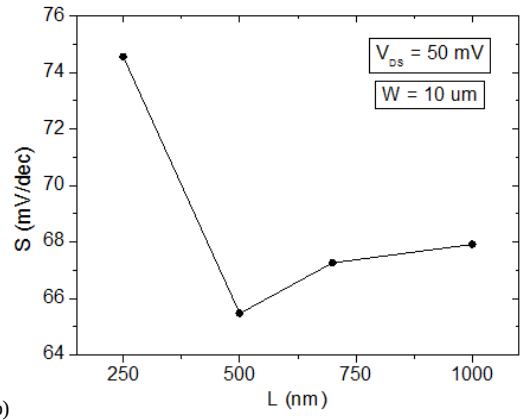


Fig 9. Drain current as a function of gate voltage for the 8 measured transistors, with 50 mV of drain voltage biasing.

Subthreshold slope was also calculated for the experiments results. Fig. 10(b) shows that there were some divengences with the simulated results. In the previous subthreshold slope figure, it can be seen that from 250 nm to 1 µm, this parameter was calculated about 60 to 63 mV/dec, while the experimental results shows values of 65 to 75 mV/dec, and there is a raise for larger channel length transistors.



(a)



(b)

Fig 10. (a) Threshold voltage for the 8 measured transistors and (b) subthreshold slope as a function of channel length.

The values obtained for maximum transconductance-channel length product, being, as related previously, proportional to carrier mobility, are presented in Fig. 11 and has a similar behaviour as obtained in simulations. This means that mobility degradation is indeed present in shorter devices, even when a thin SOI layer is used.

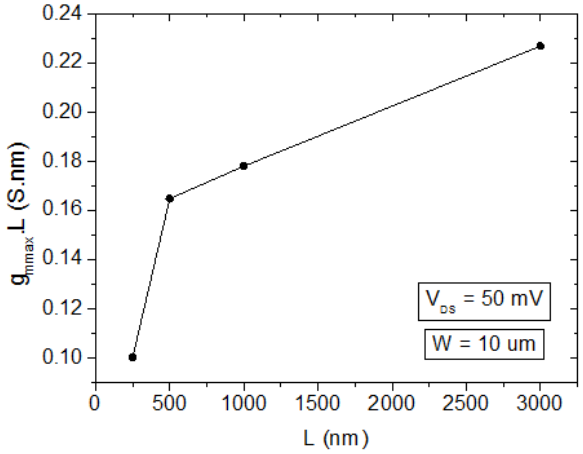


Fig 11. Maximum transconductance-channel length product as a function of channel length.

IV. CONCLUSION

Results showed that most of the analyzed parameters suffer degradation when shorter channel length devices are studied, as it happens to bulk MOS devices and SOI devices with regular thickness. Despite, some of the parameters show an improvement when compared to these devices such as the threshold voltage and subthreshold slope, that presented values close to that expected for most of the simulated devices. It could be noticed by including gate current models, that, despite it can present high values depending on the gate voltage, the analyzed parameters did not suffer change with the presence of gate current. By comparing these results to the ones obtained by electrical measurement, it can be seen some similarity in most cases, thus showing the simulation files used presented good and valid results.

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REFERENCES

[1] PAVANELLO, M. A. “Projeto, Fabricação e Caracterização Elétrica de uma Nova Estrutura para o SOI MOSFET” [tese]. São Paulo: Escola Politécnica da Universidade de São Paulo; 2000.

[2] COLINGE, J. P. Silicon-on-Insulator Technology: Materials to VLSI. 3rd Ed. Massachusetts: Kluwer Academic Publishers, 2004.

[3] MERCHA, A. et al., “’Linear Kink Effect’ Induced by Electron Valence Band Tunneling in Ultrathin Gate Oxide Bulk and SOI MOSFETs”. IEEE Transactions on Electron Devices, Vol. 50, No. 7, July 2003.

[4] LUISIER, M. and SCHENK, A., “Two-Dimensional Tunneling Effects on the Leakage Current of MOSFETs With Single Dielectric and High-κ Gate Stacks”. IEEE Transactions on Electron Devices, Vol. 55, No. 6, June 2008.

[5] ATLAS User's Manual, Silvaco (2007).

[6] ORTIZ-CONDE, A. and SÁNCHEZ F. J. G. “Scrutinizing MOSFET Threshold Voltage Extraction Methods”, Solid State Electronics, v. 1 p. 1-58, 2013.