Chip in RIO

SBCCI2007

20th Symposium on Integrated Circuits and Systems Design

SBMicro2007

22nd Symposium on Microelectronics Technology and Devices

SForum2007

Student Forum 2007

Rio de Janeiro

Brazil

Conference Guide

Contents

General Chairman's Message

On behalf of the Organizing Committee, it is my pleasure to warmly welcome you all to Chip in RIO, in the beautiful Rio de Janeiro, a city rich in culture and natural beauties. Three symposia are included in this event: the 20th Symposium on Integrated Circuits and System Design (SBCCI2007), the 22nd Symposium on Microelectronics Technology and Devices (SBMicro2007) and the 7th Microelectronics Student Forum (SForum2007).

Chip in RIO is to be held at the Rio Othon Palace Hotel, facing one of the most famous beaches in the world and Rio's best known postcards, Copacabana Beach.

The technical program this year consists of 29 sessions that cover a broad range of technical subjects. We are very pleased that the response of the Integrated Circuits Design, Technology and Devices Scientific Community confirmed the tradition of continued growth of the above symposia, reaching even more countries outside Latin America. A panel discussion on Government-sponsored research and industry initiatives in Brazil, along with four plenary presentations are also planned. In addition to the regular technical program, 8 specially organized tutorials are scheduled on Monday, September 3, preceding the start of the regular program.

Besides hard work, a conference is also a good opportunity to travel and learn more about the world countries and peoples. A number of social events are planned throughout the conference, including a Welcoming Reception and a Banquet with great Brazilian food and music. Additionally, companion activities are organized, and include bus tours to famous places such as the planet's largest urban forest, with an area of 3,300 hectares encompassing trees, belvederes, caves and waterfalls, the Sugar Loaf, and of course, the statue of Christ the Redeemer, which has just been chosen to be among the modern-day seven Wonders of the World.

I would like to express my gratitude to all the members of the organizing and technical committees for their dedication. I am honored to have such a team.

I sincerely hope you enjoy your visit to Rio de Janeiro, and you will remember both the technical and social aspects of Chip in RIO as a pleasant and worthwhile experience.

ANTONIO PETRAGLIA
General Chairman
Chip in RIO

SBCCI2007
Conference at a Glance

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08:00 - 12:30 Morning Tutorials
14:00 - 17:30 Afternoon Tutorials
19:00 - 21:00 Conference Cocktail
17:30 CECCI/SBC Assembly

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10:00 - 12:00 Technical Sessions
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17:00 - 18:00 Plenary: Mohammed Ismail

Thursday, September, 6, 2007
08:30 - 09:30 Plenary: Betty Prince
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SBMicro2007
Conference at a Glance

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Social Events

Conference Cocktail - Monday, 19:00 - 21:00

Conference Dinner - Wednesday, 20:00 - 22:00

Assemblies

CECCI/SBC Assembly - Monday, 17:30, Guaratiba

SBMicro Assembly - Wednesday, 18:00, Itaipú A

Tutorials - SBCCI2007

Monday, September, 3, 2007
Local: Guaratiba
08:00 - 10:30

Low Power Design Techniques for Nanometer Design Processes – 65nm and smaller

Subhomoy Chattopadhyay
AMD Corporation 10101 Brimfield Drive Austin, TX, USA 78726

ABSTRACT
Power has become one of the most important paradigms of design convergence for future microprocessor and ASIC/SOC designs in the 65nm and smaller geometries. The amount of logic that goes on a SOC is determined by the power envelope of the part for the applications that the part would support. In this tutorial I am presenting the importance of low power design techniques and methodologies for microprocessor/SOC design from the high level micro architectural, RTL, gate level to transistor level design. We cover the conflicting goals of performance versus low power, routinely faced by designers in the 65nm and smaller geometries. Embedded microprocessor/SOC designs are particularly dictated by standby and max/thermal design power and battery life constraints. Performance/watt or MIPS/watt is the design metric of today that we focus on in the sub 65nm geometries. We cover the main components of leakage power and elaborate on the transistor design characteristics for low power. A short discussion of different process variants for various types of applications will also be discussed followed by an introduction of shadow latches and state retention techniques used by microprocessors and DSPs of today. Tradeoff between amount of state retained and the exit latency of the processor from deep sleep/standby states will be discussed. In short, this tutorial attempts to provide a broad overview on the importance of low power design methodologies for SOC/ASICs in the sub 65nm era. It also discusses the state of the art techniques for lower power design for wireless and mobile applications.

Biography:
Mr. Subhomoy Chattopadhyay is a Senior member of Technical Staff Lead at AMD Corporation in Austin, TX, USA. He is leading a team on mobile platform power/performance optimization. After graduating from the University of Tennessee with a MSEE degree, Mr. Chattopadhyay has worked as a senior technical lead and manager at IBM Corporation, Sun Microsystems and Intel Corporation for the last 13 years. He is a Senior member of the IEEE and has many publications in various IEEE International conferences. He has worked on various aspects of Low Power Design at Intel Corporation for the last 5 years. He has presented invited lectures and Low Power Tutorials at various conferences around the world - like Japan, Germany, UK, India and USA.

Monday, September, 3, 2007
Local: Itaipú A
09:00 - 10:30

RF Architectures in CMOS for the Emerging Wireless Technologies – Challenges and opportunities

Ahmed A. Youssef
University of Calgary, Canada

ABSTRACT
The recent proliferation of personal communications systems (PCS) applications and cellular hones is driving a demand for portable systems which share the common requirements of low cost, small form factor and low power consumption. In addition, the emergence of various wireless technologies around the world has created a demand for RF wireless radios (transceivers) that can operate in more than one mode. Thus, multistandard/mode RF transceivers are predicted to play a critical role in wireless communication systems in the future. This tutorial will discuss the evolution of the wireless industry and will focus on power technology and transceiver architectures used in modern cost effective integrated mobile communication systems. Architectures and design techniques suitable for multi-standard/mode low power transceivers in CMOS technology will be presented. We will be exploring the amazing possibilities that cognitive radio technologies may offer for new RF applications.

Biography:
Ahmed A. Youssef received the B.Sc. (Hon.) and M.Sc. degrees both in Electrical Engineering from Ain Shams University, Cairo, Egypt, in 1998 and 2002, respectively. Since 2003, he has been with the University of Calgary, AB, Canada, where he is currently working toward the Ph.D. degree in RF integrated circuits and systems. His research interests include the analog high speed integrated circuit for the wireless applications.
Mr. Youssef is the recipient of the Mobinil Telecommunication Inc. Pre-master Fellowship in 2000 (for two years). He also received the Young Scientist Award at the Maastricht General Assembly of the International Union of Radio Science in 2002 (the Netherlands) and an Honorable Mention at 2003 in the Symposium of the Microelectronics Research & Development in Canada, Montreal. In 2005 he received the prestigious GORDON LEWIS HEDBERG DOCTORAL Award and TRLabs award in 2006.
Mr. Youssef has also industrial experience through working as an RF project engineer at Mentor Graphics in several projects related to the design reuse of RF integrated circuits. He presented several short courses and tutorials to IEEE conferences and to the industry as well in the area of high speed integrated circuit for wireless communication systems.

Monday, September, 3, 2007
Local: Itaipú A
11:00 - 12:30

First-pass-silicon Radio IPs for B3G Wireless Networks
Mohammed Ismail
Analog VLSI Lab, Ohio State University, USA

ABSTRACT
As we move from third generation (3G) to 4G wireless and as we strive to meet the demands for higher data rates and short distance wireless applications, a debate has ensued on whether cellular and WLAN/WMAN are seen as complementary or competing technologies. In either case, wireless services beyond 3G (B3G) are moving to all-IP, always-best-connected, convergent wireless solutions requiring access to different wireless infrastructures from the same wireless device, be it a cell phone, a laptop or a PDA for a multitude of services including voice, data and multimedia applications. For future handheld wireless devices, this requires low power, low cost multi-standard multi-band chipsets, the radio part of which will be increasingly complex with stringent demands on power consumption and cost as the two main differentiators.
We will present radio design IPs at the system, architectural and block levels for emerging always-best-connected wireless applications and with focus on smart power, first-pass-silicon radio transceiver design in deep sub-micron CMOS. We will highlight both the challenges and the opportunities for innovation in this area.

Biography:
Mohammed Ismail has over 20 years experience of R&D in the fields of analog, RF and mixed signal integrated circuits. He has held several positions in both industry and academia and has served as a corporate consultant to nearly 30 companies in the US, Europe and the far east. He is The Founding Director of the Analog VLSI Lab at Ohio State. His current interest lies in research involving digitally programmable/configurable fully integrated radios with focus on low voltage/low power first-pass solutions for 3G and 4G wireless handhelds. He publishes intensively in this area and has been awarded 11 patents. He has coedited and coauthored several books including a text on Analog VLSI Signal and Information Processing, (McGraw Hill). His last book (2007) is entitled Radio Design in Nanometer Technologies, Springer. He co-founded ANACAD-Egypt (now part of Mentor Graphics,Inc.) and Spirea AB, Stockholm (now Firstpass Technologies Inc.), a developer of CMOS radio and mixed signal IPs for handheld wireless applications.
Dr. Ismail has been the recipient of several awards including the US National Science Foundation Presidential Young Investigator Award, the US Semiconductor Research Corp Inventor Recognition Awards in 1992 and 1993, and a Fulbright/Nokia fellowship Award in 1995. He is the founder of the International Journal of Analog Integrated Circuits and Signal Processing, Springer and serves as the Journal's Editor-In-Chief. He has served as Associate Editor for many IEEE Transactions, was on the Board of Governors of the IEEE Circuits and Systems Society and is the Founding Editor of "The Chip" a Column in The IEEE Circuits and Devices Magazine. He obtained his BS and MS degrees in Electronics and Communications from Cairo University, Egypt and the PhD degree in Electrical Engineering from the University of Manitoba, Canada. He is a Fellow of IEEE.

Monday, September, 3, 2007
Local: Itaipú A
14:00 - 15:30

Focal Plane Processors & Pixel Level Processing - Mimicking natural vision systems to solve image processing problems

Gustavo Liñán Cembrano
Instituto de Microelectrónica de Sevilla - IMSE

ABSTRACT
It can be to some extent strange for non-experts to observe that, despite its potential interest for many different industries, artificial vision systems are far to reach the performance of those of the smallest insects. Is not that a paradox when we have microprocessors in 65nm technologies with GHz clocks?
In order to find out some of the reasons, one needs to realize that vision is an extremely complex task. Just to give a number, consider that reading a text at a normal velocity requires processing some 1Gigabit per second (1GBPS), and this is a simple task. On the other hand, our eye is able to cover almost 200dB of dynamic range, whereas today's wider dynamic range sensors barely reach 120dB, at the expense of a very poor contrast. Besides, one needs to consider the analogies and differences between elementary units in artificial and natural visual systems, that is neurons vs. transistors. Talking about computational efficiency and reliability, it is clear that a single transistor has not the functionality of a single neuron, which can connect to hundreds of neighbouring cells to get/send information from/to. Moreover, natural neural networks are fault tolerant by design, that is, computational power does not rely on a single extremely powerful unit, but on the massive cooperation of elementary processors.
In addition to these noticeable facts, perhaps, the most important aspect is the difference in architecture. Conventional vision systems include a camera, a powerful Analog-to-Digital converter, and a high-end DSP or microprocessor which executes any computational task in the process. This is clearly in contrast to what happens in primate's visual systems where the eye, does not only contain the iris and photoreceptors, but a number of stratified layers of neurons performing a crucial preprocessing which allows to transmit compressed information about the scene through the optic nerve, implementing a concept which is commonly known as the "near-sensor" approach. Architecturally, every major block in the natural visual system executes some image processing task and has a structure which is optimized for the kind of data being processed, maintaining the parallelism of the operation everywhere.
Can we try to imitate some of this evolution's wonderful engineering work in an electronic system? This is what we will try to answer in this tutorial, where we will present the advances and motivations for the design of Focal Plane Array Processors. A kind of device whose main property is that of having an array of sensors which are not only able to capture the scene, but are also provided with some basic computational resources (scalers, adders, memories, connections to neighbours) which permit the execution of highly-parallelized image processing tasks (typical of low-level vision applications) in a very efficient manner.

Biography:
Gustavo Linan Cembrano was born in Seville in 1973. He received the B.S. degree in electronic physics in June 1996, and the M.S. degree in microelectronic in June 1998. In September 2002 He received the Ph.D. degree in physics for his work entitled "Design of Low-Power Mixed-Signal Vision Chips". In 1995 He got an scholarship from the Andalusian goverment to start researching at the Institute of Microelectronic of Seville (IMSE), where he is since then. Since January 2002 he is also with the Department of Electronic and Electromagnetism of the University of Seville where he is an assistant professor in the Faculty of Physics and the School of Technical Engineering in Computer Science.
Gustavo Linan Cembrano has worked in various research projects dealing with integrated circuits and systems. His main areas of interest are design and analysis of real-time image

processing and preprocessing systems. He has been in the design teams of different Low-Level image processing chips ACE4k, and ACE16k, headed by Prof. Angel Rodriguez Vazquez.

Gustavo Linan is co-recipient of the International Journal of Circuit Theory and Applications "Best Paper Award 1999", edited by John Wiley & Sons, for the paper: R. Carmona, I. Garcia-Vargas, G. Linan, R. Dominguez-Castro, S. Espejo and A. Rodriguez-Vazquez, "SIRENA: A CAD Environment for Behavioral Modeling and Simulation of VLSI CNNs", International Journal of Circuit Theory and Applications, John Wiley & Sons, Vol. 27, No. 1, pp. 43-76. January-February 1999.

He was also co-recipient of the award to the Most Innovative Research Project of the Salva i Campillo 2002 awards, given by the Catalonian Association of Telecomunication Engineers for the project: A. Rodriguez-Vazquez, S. Espejo, R. Dominguez-Castro, E. Roca, R. Carmona y G. Linan (Centro Nacional de Microelectrónica, Sevilla - CSIC): Circuitos Integrados Para Aplicaciones de Vision Mediante Procesamiento en el Plano Focal. 7 Nit de les Telecomunicacions, Barcelona, February 6, 2002.

Monday, September, 3, 2007
Local: Itaipú A
16:00 - 17:30

Embedded Non-Volatile Memories
Betty Prince
Memory Strategies International, USA

ABSTRACT

This tutorial covers trends in embedded non-volatile memories including details of issues for scaling NAND and NOR flash and descriptions of scaled flash memory technologies and various evolutionary flash memory technologies such as trapping site storage memory including SONOS/MONOS and Nanocrystal memory. It also covers details of the technology and status of various emerging and nanotechnology non-volatile memories including: Magnetic RAM, Phase-Change RAM, Ferroelectric Memory and others.

Biography:
Dr. Betty Prince is CEO of Memory Strategies International. She has 35 years experience in the semiconductor industry with T.I., Philips, Motorola, R.C.A., and Fairchild. She is author of the books: Semiconductor Memories (1982), Semiconductor Memories 2nd Edition (1992), High Performance Memories, (1999) (John Wiley & Sons), and Emerging Memories - Technologies and Trends, (2002) (Kluwer Academic). She is a Senior Member of the IEEE, an IEEE SSCS Distinguished Lecturer, is on the Program Committee of the IEEE Custom Integrated Circuit conference and served on the Technical Advisory Board of IEEE Spectrum magazine. She was founder of the JEDEC JC-16 Interface Standards body, co-chair of the JC-42 JEDEC SRAM standards group and on the IEC SC47A WG3 Memory Standards Committee. She serves on the Technical Advisory Board of several memory companies and holds patents in the memory, processor and interface areas. She has a B.S. and M.S. in physics and math from the University of New Mexico and the University of California, an M.B.A. and a Ph.D. from the University of Texas with doctoral dissertation on fractal modeling.

Tutorials - SBMicro2007

Monday, September, 3, 2007
Local: Guaratiba
11:00 - 12:30
Chair: João Antonio Martino - *LSI/EPUSP, Brazil*

SOI Technology : from Materials to Device Physics and Characterization
Sorin Cristoloveanu
Institute of Microelectronics, Electromagnetism and Photonics (IMEP, UMR 5130)
INP Grenoble - Minatec, BP 257, 38016 Grenoble Cedex 1, France

ABSTRACT
The aim of this tutorial is to offer a comprehensive image of the state-of-the-art and future trends. The first part is dedicated to SOI materials: methods of fabrication (epitaxy, implantation and/or bonding), typical structures, ultra-thin strained or unstrained films, evaluation methods. The family of SOI devices will briefly be introduced to show how the SOI materials can adapt to each application. The various mechanisms which govern the operation of fully depleted and partially depleted transistors will be explained. We will next see how to manipulate the MOSFET in order to reveal, from its static and dynamic characteristics, key parameters like carrier mobility and lifetime, self-heating, noise, oxide and interface defects, etc.

The second part of the tutorial will address the horizon of SOI-based CMOS technology. We will explain the scaling strategy of SOI MOSFETs. Several nano-size mechanisms and short-channel effects will be discussed based on experimental evidence: fringing fields, self-heating, transition from partial to full depletion, gate tunneling, super-coupling, volume inversion, and quantization. The impact of strain, channel orientation and film thickness on the carrier mobility will be illustrated. Finally, the 3-D scaling of the transistor volume will take us from single-gate to multiple-gate transistors.

Biography:
Sorin Cristoloveanu received the PhD (1976) and the Doctorat ès-Sciences (1981) from the National Polytechnic Institute, Grenoble. He joined the National Centre of Scientific Research (CNRS) and became a Director of Research in 1989. He also worked at several Universities (Maryland, Florida, Vanderbilt, Perth) and at JPL (Pasadena). He served as the director of the LPCS Laboratory and the Center for Advanced Projects in Microelectronics (Grenoble), initial seed of the Minatec center. He is the author or co-author of more than 600 technical journal papers and conference presentations, author/editor of 17 books, and organizer of 16 international conferences. His expertise is in the area of the electrical characterization and modeling of SOI materials and devices. With his students, he has received several Best Paper and Society Awards. He is a Fellow of IEEE, Fellow of ECS, and Editor of Solid-State Electronics.

Monday, September, 3, 2007
Local: Guaratiba
14:00 - 15:30
Chair: Marcelo Antonio Pavanello - *FEI, Brazil*

Impact Strain Engineering on Device Performance
Cor Claeys
IMEC - Belgium

ABSTRACT
To keep track with Moore's law, strain engineering based on either a global or a local approach is gaining much interest and has already been successfully implemented for 65 and 45 nm technology nodes. Although the first goal is to improve the drive current by mobility enhancement, other performance parameters such as leakage current, minority carrier lifetime and low frequency 1/f noise have to be considered.
This presentation will first give an overview of the different strain engineering techniques already used or under investigation nowadays, before discussing more in detail their impact on several electrical device parameters. Attention will be given to illustrate a global approach based on strained Si on strain-relaxed SiGe buffer layers and the use of process-induced stressors such as an embedded SiGe layer and a contact etch stop etch layer (CESL). Some advantages and disadvantages of the different approaches will be outlined. Also the use of Ge and GeOI as high-mobility substrates is briefly addressed.

Biography:
Cor Claeys was born in Antwerp, Belgium. He received the electrical-mechanical engineering degree in 1974 and the Ph.D. degree in 1979, both from the Katholieke Universiteit Leuven (KU Leuven), Belgium. From 1974 to 1984 he was a Research Assistant and Staff Member, respectively, of the ESAT Laboratory of the KU Leuven and since 1990, a Professor. In 1984, he joined IMEC as Head of Silicon Processing Group. Since 1990 he is Head of the research group on Radiation Effects, Cryogenic Electronics and Noise Studies. He is also responsible for Strategic Relations and is for IMEC on the management board of several projects funded by the European Commission (NANOCMOS, SINANO, FLYING WAFER, CADRES, STAR, EUROSOI, SEA-NET, PULLNANO…). He is also member of the European Expert Group on Nanosciences. His main interests are in general silicon technology for ULSI, device physics, including low-temperature operation, low frequency noise phenomena and radiation effects, and defect engineering and material characterization. He coedited a book "*Low Temperature Electronics*" and wrote a book "*Radiation Effects in Advanced Semiconductor Materials and Devices*". He also authored and co-authored eight book chapters and more than 700 technical papers and conference contributions related to the above fields. He has been involved in the organisation of a large number of international conferences and edited more than 35 Proceedings Volumes. He is an associated Editor for the *Journal of the Electrochemical Society*. He had short stays as Visiting Professor at the Queens University in Belfast, Ireland, and the University of Calabria, Italy.
Prof. Claeys is a member of the European Material Research Society, a Senior Member of IEEE and a Fellow of the Electrochemical Society. He was the founder of the IEEE Electron Devices Benelux Chapter, was Chair of the IEEE Benelux Section, was in the period 1999-2005 elected AdCom member of the Electron Devices Society (EDS), and was EDS Vice-President for Chapters and Regions during 2000-2006. Since 2000 he is an EDS Distinguished Lecture. In 2006, he has been elected as EDS President-Elect. He also received the IEEE Third Millennium Medal. Within the Electrochemical Society he has been serving in different committees and was Chair of the Electronics Division (2001-2003). In 1999 he was elected as Academician and Professor of the International Information Academy. In 2004 he received the Electronics Division Award of the Electrochemical Society.

Monday, September, 3, 2007
Local: Guaratiba
16:00 - 17:30
Chair: Cor Claeys - *IMEC, Belgium*

Noise in Advanced Electronic Devices and Circuits
M. Jamal Deen
Electrical and Computer Engineering Department, CRL 226, McMaster University
280 Main Street West, Hamilton, ON L8S 4K1, Canada

ABSTRACT
The recent explosion in wireless and information technology has been one of the most dramatic applications of semiconductor technology in the past decade. This explosive revolution is apparent in the ever increasing use of wireless products such as cell-phones, personal digital assistants (PDA), digital cameras and electronic entertainment systems. Key ingredients of this technological revolution have been the rapid advances in the quality and processing of materials, and in device, circuit and system design and integration. In the area of materials, the science and technology of dielectrics occupies a prominent place in providing the dominant technology, complementary metal-oxide-semiconductor (CMOS), with its important characteristics of negligible standby power dissipation, good input-output isolation and surface potential control for switching operations. However, with this explosion in wireless and portable applications of semiconductor technology, noise has become a major concern. This is clearly underscored in the recent update of ITRS roadmap which highlights the importance of both low-frequency noise (LFN) as well as radio-frequency (RF) noise as silicon-based devices are scaled to deepsubmicron dimensions in the nanometer range for the nanoscale transistors and circuits.
In this presentation, state-of-art low-frequency and high-frequency noise performance and modeling in modern semiconductor devices and circuits will be discussed. The first part of the presentation will be on low-frequency noise where it will be shown that the increase of noise-to-DC current ratio may compromise circuit performance in the near future. For statistically valid experiments, it will be demonstrated that the low-frequency noise (LFN) tends to a log-normal distribution. Since the random-telegraph-signal (RTS) noise is pronounced in deep submicron devices, new techniques for characterization of multilevel RTS being observed will be discussed. The second part of the presentation will be focused on radio-frequency (RF) noise modeling of MOSFETs, including a model for the important effect of gate-tunneling current for future devices, plus sample experimental results. Then, based on the extracted active noise sources form highfrequency noise measurements, physics-based noise models for these noise sources of interest in deep submicron MOSFETs will be discussed. A simple analytic model that can be used as a guide for circuit design will be highlighted, including its scalability. The third part of the presentation will briefly introduce the subject of noise in circuits. Here, results from different types of oscillators will be discussed. Finally, the effects of hot-carrier stress on the performance of a RF voltage-controlled oscillator and a RF low-noise amplifier will be discussed.

Biography:
Dr. M. Jamal Deen was born in Georgetown, Guyana. He completed a B.Sc. degree in Physics and Mathematics at the University of Guyana (1978), a M.S. degree (1982) and a Ph.D. degree (1985) in Electrical Engineering and Applied Physics at Case Western Reserve University (CWRU), Cleveland, Ohio, U.S.A.
Dr. Deen has published extensively in microelectronics/ nanolectronics and optoelectronics. He has edited two research monographs and eleven conference proceedings. He has written fifteen invited book chapters, was awarded six patents, has published more that three-hundred and fifty peer-reviewed articles and has given eighty invited, keynote or plenary conference presentations. Dr. Deen has also won six best papers awards at national and international conferences/workshops and for a journal paper. He has also served as a consultant to the

semiconductor industry in Canada, the USA and Japan. His current research interests are in microelectronics/ nanoelectronics and opto-electronics.
Dr. Deen has been elected a Fellow of the Royal Society of Canada (RSC); a Fellow of the Institute of Electrical and Electronic Engineers (IEEE); a Fellow of the Engineering Institute of Canada (EIC); a Fellow of the Electrochemical Society (ECS); a Fellow of the American Association for the Advancement of Science (AAAS);and an Honorary Member of the World Innovation Foundation – the foundation's highest honor.

Plenary Sessions - SBCCI2007 and SBMicro2007

Tuesday, September, 4, 2007
Local: Itaipú A
08:30 - 09:30

Highly Sensitive, Low-cost Integrated Biosensors
M. Jamal Deen
Electrical and Computer Engineering Department, CRL 226
McMaster University, Hamilton, ON L8S 4K1, Canada

ABSTRACT
Recently there has been an increasing interest in the development of electronic sensors for the detection and identification of biological species. For example, label-free DNA detection has been made possible by the use of field-effect sensors. In these sensor systems, the intrinsic charge of DNA molecules is detected through the use of metal-oxide-semiconductor field-effect transistors (MOSFETs) in which the gate electrode has been removed and the gate oxide area functionalized to make them sensitive to the species of interest. These modified transistors are called BioFETs because they are FETs that are modified to be sensitive to biological molecules. The feasibility of this BioFET approach has been demonstrated experimentally, but the sensitivity of these systems has to be significantly improved if they are to be used as a means to detect and identify biological species such as pathogen agents, quickly and at low cost. The sensitivity of biosensors is ultimately determined by their noise properties. While in principle it is possible to amplify an arbitrarily small electric signal, if this signal is embedded in noise, very little information can be recovered. In general, the noise performance of an electrical system is determined by the initial stages. In an instrumentation system, the transducer and the first amplifier connected to it have to add very little noise to the signal of interest. Also, the noise from the succeeding stages is less critical if the signal has been brought to reasonable levels by the first amplifier. For this reason, the noise properties of field-effect biosensors (BioFETs), as well as design techniques for very low-noise integrated amplifiers will be discussed. The detection of biological species is a relatively slow process, where the time constants typically range from minutes to hours; therefore, low-frequency noise is the main concern in integrated biosensors. In this presentation, we will discuss a BioFET sensor we have been developing for detecting specific pathogens. The noise properties of field-effect biosensors (BioFETs), as well as design techniques for very low-noise integrated amplifiers will be discussed in detail. Next, we will discuss the detailed modeling of all important parts of the electrolyte-sensor system and will show that by detailed analyses of both signal and noise characteristics of the integrated sensor system, that it is possible to optimize the BioFET's performance. Experimental results will also be described to show current state-of-the-art in these BioFET sensor systems. Finally, we will show how to create low-cost, highly integrated and parallel detection systems by integrating the sensor with fluidic and mechanical components, plus the processing electronics on the same chip, for real-world applications, and what are the resulting system's performance characteristics.

Biography:
Dr. M. Jamal Deen was born in Georgetown, Guyana. He completed a B.Sc. degree in Physics and Mathematics at the University of Guyana (1978), a M.S. degree (1982) and a Ph.D. degree (1985) in Electrical Engineering and Applied Physics at Case Western Reserve University (CWRU), Cleveland, Ohio,
U.S.A. Dr. Deen has published extensively in microelectronics/ nanolectronics and optoelectronics. He has edited two research monographs and eleven conference proceedings. He has written fifteen invited book chapters, was awarded six patents, has published more that three-hundred and fifty peer-reviewed articles and has given eighty invited, keynote or

plenary conference presentations. Dr. Deen has also won six best papers awards at national and international conferences/workshops and for a journal paper. He has also served as a consultant to the semiconductor industry in Canada, the USA and Japan. His current research interests are in microelectronics/ nanoelectronics and opto-electronics. Dr. Deen has been elected a Fellow of the Royal Society of Canada (RSC); a Fellow of the Institute of Electrical and Electronic Engineers (IEEE); a Fellow of the Engineering Institute of Canada (EIC); a Fellow of the Electrochemical Society (ECS); a Fellow of the American Association for the Advancement of Science (AAAS);and an Honorary Member of the World Innovation Foundation – the foundation's highest honor.

Wednesday, September, 5, 2007
Local: Itaipú A
08:30 - 09:30

Meeting with the Forthcoming IC Design - Solving issues by 3D stacking
Takayasu Sakurai
University of Tokyo, Japan

ABSTRACT

In the foreseeable future, VLSI design will meet a couple of explosions: power, variability and NRE (non-recurring engineering cost). Some of the solutions for power-aware designs are covered in this talk with relation to variability. A remedy for the NRE explosion is to reduce the number of developments and manufacture and sell tens of millions of chips under a fixed design. System-in-a-Package approach may embody such possibility. Several new technologies are described to enable 3-dimensional stacking of chips to build high-performance yet low-power electronics systems. On the other extreme of the silicon VLSI's which stay as small as a centimeter square, a new domain of electronics called large-area integrated circuit as large as meters is waiting, which may open up a new continent of applications in the era of ubiquitous electronics. One of the implementations of the large-area electronics is based on organic transistors. The talk will provide perspectives of the organic circuit design taking E-skin, sheet-type scanner, Braille display and wireless power transmission sheet as examples.

Biography:
Takayasu Sakurai received the B.S., M.S. and Ph.D degrees in EE from University of Tokyo. In 1981 he joined Toshiba Corp., where he designed numerous VLSI products including memories and processors. From 1988 to 1990, he was a visiting researcher at Univ. of Calif., Berkeley. From 1996, he is a professor at University of Tokyo, working on VLSI design and organic circuits. He was a conference chair and a TPC member of international conferences in the field of VLSI design including ISSCC, VLSI Circuit Symp., A-SSCC, CICC, ESSCIRC and DAC. He is a recepient of 2005 IEEE ICICDT award, 2004 IEEE Takuo Sugano award and 2005 P&I patent of the year award and other awards. He is an IEEE Fellow, a STARC Fellow, an elected AdCom member for the IEEE SSCS and an IEEE CAS and SSCS distinguished lecturer.

Wednesday, September, 5, 2007
Local: Itaipú A
17:00 - 18:00

WiMAX: A competing or Complementary Technology to 3G?

Mohammed Ismail
Analog VLSI Lab, Ohio State University, USA

ABSTRACT
This presentation will contrast WiMAX and 3G wireless technologies and will discuss whether the two technologies are competing or complementary particularly for developing countries.The eventual convergence of the two in what is called "LTE or Long Term Evolution,or Super 3G, S3G " will also be discussed. To this end, the challenges that lie ahead in developing complex MIMO radios with multi-band front end modules (FEMs) will be discussed.Examples of WiMAX and LTE radio architectures will be presented.

Biography:
Mohammed Ismail has over 20 years experience of R&D in the fields of analog, RF and mixed signal integrated circuits. He has held several positions in both industry and academia and has served as a corporate consultant to nearly 30 companies in the US, Europe and the far east. He is The Founding Director of the Analog VLSI Lab at Ohio State. His current interest lies in research involving digitally programmable/configurable fully integrated radios with focus on low voltage/low power first-pass solutions for 3G and 4G wireless handhelds. He publishes intensively in this area and has been awarded 11 patents. He has coedited and coauthored several books including a text on Analog VLSI Signal and Information Processing, (McGraw Hill). His last book (2007) is entitled Radio Design in Nanometer Technologies, Springer. He co-founded ANACAD-Egypt (now part of Mentor Graphics,Inc.) and Spirea AB, Stockholm (now Firstpass Technologies Inc.), a developer of CMOS radio and mixed signal IPs for handheld wireless applications.
Dr. Ismail has been the recipient of several awards including the US National Science Foundation Presidential Young Investigator Award, the US Semiconductor Research Corp Inventor Recognition Awards in 1992 and 1993, and a Fulbright/Nokia fellowship Award in 1995. He is the founder of the International Journal of Analog Integrated Circuits and Signal Processing, Springer and serves as the Journal's Editor-In-Chief. He has served as Associate Editor for many IEEE Transactions, was on the Board of Governors of the IEEE Circuits and Systems Society and is the Founding Editor of "The Chip" a Column in The IEEE Circuits and Devices Magazine. He obtained his BS and MS degrees in Electronics and Communications from Cairo University, Egypt and the PhD degree in Electrical Engineering from the University of Manitoba, Canada. He is a Fellow of IEEE.

Thursday, September, 6, 2007
Local: Itaipú A
08:30 - 09:30

Nanotechnology and Emerging Memories

Betty Prince, Ph.D., CEO
Memory Strategies International 16900 Stockton Drive Leander, TX, USA 78641

ABSTRACT
Scaling conventional memories such as SRAM, DRAM and Floating Gate Flash has become difficult in the nanotechnology regions where the properties historically associated with these memories change. Scaled SRAM issues include decreased cell stability, increased sub-threshold leakage and variability. Solutions range from high-k dielectrics to double gate and vertical structures or to added transistors in the cell. Magnetic RAM (MRAM) offers a possible solution for the future. Issues for scaled DRAM include power dissipation and processing of vertical capacitors, and pass transistor engineering. Intermediate solutions include SOI trench and MIM capacitors, and double gate or material engineered transistors. Future DRAMs being investigated include: floating body cells, gain cells and negative differential conductance memories. For non-volatile memory, issues with scaled floating gate flash cells include: capacitive interference between floating gates, loss of coupling between control and floating gate, drain disturbance and charge leakage. Scaling issues differ somewhat for NAND and NOR flash. In the near term, a solution for scaling non-volatile memories is being found by replacing the floating gate with multi-bit trapping site materials such as nitride storage and nanocrystal. Longer term, various Phase Change RAMs are being investigated for future non-volatile memory. Very low power non-volatile RAM applications are beginning to be served by Ferroelectric memory. Much further out in time, other new memory technologies are being investigated such as MEMs, molecular, and single electron memories.

Biography:
Dr. Betty Prince is CEO of Memory Strategies International. She has 35 years experience in the semiconductor industry with T.I., Philips, Motorola, R.C.A., and Fairchild. She is author of the books: Semiconductor Memories (1982), Semiconductor Memories 2nd Edition (1992), High Performance Memories, (1999) (John Wiley & Sons), and Emerging Memories - Technologies and Trends, (2002) (Kluwer Academic). She is a Senior Member of the IEEE, an IEEE SSCS Distinguished Lecturer, is on the Program Committee of the IEEE Custom Integrated Circuit conference and served on the Technical Advisory Board of IEEE Spectrum magazine. She was founder of the JEDEC JC-16 Interface Standards body, co-chair of the JC-42 JEDEC SRAM standards group and on the IEC SC47A WG3 Memory Standards Committee. She serves on the Technical Advisory Board of several memory companies and holds patents in the memory, processor and interface areas. She has a B.S. and M.S. in physics and math from the University of New Mexico and the University of California, an M.B.A. and a Ph.D. from the University of Texas with doctoral dissertation on fractal modeling.

Technical Program

SBCCI2007

TUESDAY MORNING

SÃO CONRADO 10:00 - 12:00

A/D and D/A Converters

Chair: **Wilhelmus Van Noije** - *USP*

10:00 A SMALL AREA 8BITS 50MHZ CMOS DAC FOR BLUETOOTH TRANSMITTER
Hugo Hernández, Wilhelmus Van Noije, and João Navarro, *Integrable Systems Laboratory - Polytechnic School of São Paulo University*
Elkim Roa, *Design and Research Group on Integrated Circuits - Industrial University of Santander*

10:20 SUPPRESSION OF DELTA-SIGMA DAC QUANTISATION NOISE BY BANDWIDTH ADAPTATION
Jørgen Andreas Michaelsen and Dag T. Wisland, *University of Oslo*

10:40 NOVEL SWAPPING TECHNIQUE FOR BACKGROUND CALIBRATION OF CAPACITOR MISMATCHING IN PIPELINE ADCS
Antonio José Ginés Arteaga, Eduardo José Peralías Macías and Adoración Rueda Rueda, *Instituto de Microelectrónica de Sevilla CNM-CSIC, University of Seville*

11:00 HIGH-SPEED CMOS ANALOG-TO-DIGITAL CONVERTER FOR FRONT-END RECEIVER APPLICATIONS
Andre Mariano, Birama Goumballa, Dominique Dallet, Yann Deval and Jean-Baptiste Begueret, *University of Bordeaux*

TUESDAY MORNING

GUARATIBA 10:00 - 12:00

SoCs and Embedded Systems I
Chair: **Fernanda Kastensmidt** - UFRGS

10:00 A HYBRID MEMORY ORGANIZATION TO ENHANCE TASK MIGRATION AND DYNAMIC TASK ALLOCATION IN NoC-BASED MPSoCS
Daniel Barcelos, Eduardo Wenzel Brião and Flávio Rech Wagner, *Universidade Federal do Rio Grande do Sul*

10:20 CACHE COHERENCY COMMUNICATION COST IN A NOC-BASED MP-SOC PLATFORM
Gustavo Girão, Bruno Cruz de Oliveira and Ivan Saraiva Silva, *Universidade Federal do Rio Grande do Norte*
Rodrigo Soares, *Universidade de São Paulo*

10:40 THE INTERVAL PAGE TABLE: VIRTUAL MEMORY SUPPORT IN REAL-TIME AND MEMORY-CONSTRAINED EMBEDDED SYSTEMS
Xiangrong Zhou and Peter Petrov, *University of Maryland*

11:00 A SOFT ERROR ROBUST AND POWER AWARE MEMORY DESIGN
Costas Argyrides and Dhiraj Pradhan, *Bristol University*
Carlos Lisboa and Luigi Carro, *Instituto de Informática, PGCC, Universidade Federal do Rio Grande do Sul*

TUESDAY AFTERNOON

SÃO CONRADO 14:30 - 15:30

Analog Circuits I
Chair: **Altamiro Susin** - *UFRGS*

14:30 A ULTRA LOW POWER CMOS pA/V TRANSCONDUCTOR AND ITS APPLICATION TO WAVELET FILTERS
Peterson Agostinho and Osamu Saotome, *Technological Institute of Aeronautics*
Sandro Haddad and Jader Lima, *Freescale Semiconductor*
Wouter Serdijn, *Delft University of Technology*

14:50 A PROGRAMMABLE VOLTAGE REFERENCE OPTIMIZED FOR POWER MANAGEMENT APPLICATIONS
Filipe Ramos, *Freescale Semiconductor*
Laercio Caldeira and Tales Pimenta, *UNIFEI*

15:10 TRIM RANGE LIMITED BY NOISE IN BANDGAP VOLTAGE REFERENCES
Dalton Colombo, Gilson Wirth and Sergio Bampi, *Universidade Federal do Rio Grande do Sul*

TUESDAY AFTERNOON

SÃO CONRADO 15:30 - 16:30

Analog Circuits II
Chair: **Carlos G. Montoro** - *UFSC*

15:30 CURRENT MODE INSTRUMENTATION AMPLIFIER WITH RAIL-TO-RAIL INPUT AND OUTPUT
Filipe Costa Beber Vieira, Cesar Augusto Prior, Cesar Ramos Rodrigues, Leonardo Perin and Joao Baptista Martins, *Universidade Federal de Santa Maria*

15:50 A MULTISAMPLING TIME-DOMAIN CMOS IMAGER WITH SYNCHRONOUS READOUT CIRCUIT
Fernando de Souza Campos, *FEB - Unesp*
Ognian Marinov, Naser Faramarzpour and Jamal Deen, *McMaster University*
Jacobus W. Swart, *Unicamp*

16:10 A SYSTEMATIC METHOD TO APPROXIMATE CAPACITANCE RATIOS TO IMPROVE CAPACITANCE MATCHING IN SC FILTERS
Carlos Fernando Soares and Antônio Petraglia, *Federal University of Rio de Janeiro*

16:30 - 17:00 Coffee break

TUESDAY AFTERNOON

SÃO CONRADO 17:00 - 18:00

Biomedical Devices
Chair: **Antonio Petraglia** - *UFRJ*

17:00 ON THE DESIGN OF ULTRA LOW NOISE AMPLIFIERS FOR ENG RECORDING
Alfredo Arnaud, Martin Bremermann, Joel Gak and Matias Miguez, *Universidad Católica*

17:20 DESIGN OF AN INTEGRATED LOW POWER HIGH CMRR INSTRUMENTATION AMPLIFIER FOR BIOMEDICAL APPLICATIONS
Cesar Augusto Prior, Cesar Ramos Rodrigues, João Baptista Martins, Andre Luiz Aita and Filipe Costa Beber Vieira, *Universidade Federal de Santa Maria - RS*

17:40 DESIGN OF A CLASS D AMPLIFIER FOR HEARING AID DEVICES
Daniel Ruiz, Robson Moreno and Tales Pimenta, *UNIFEI*

TUESDAY AFTERNOON

GUARATIBA 14:30 - 15:30

Reconfigurable Logic and FPGAs I
Chair: **Ivan Saraiva Silva** - *UFRGN*

14:30 HIGH THROUGHPUT UNIFIED AND RECONFIGURABLE MONTGOMERY MULTIPLIER ARCHITECTURE WITHOUT USING FOUR-TO-TWO CSA
Sudhakar M and Srinivas M.B, *International Institute of Information Technology (IIIT)*

14:50 OPTIMIZATION TECHNIQUES FOR A RECONFIGURABLE, SELF-TIMED, AND BIT-SERIAL ARCHITECTURE
Achim Rettberg, *University Paderborn/C-LAB*
Florian Dittmann and Raphael Weber, *University Paderborn/HNI*

15:10 RoSA: A RECONFIGURABLE STREAM-BASED ARCHITECTURE
Monica Magalhaes Pereira, Bruno Cruz de Oliveira and Ivan Saraiva Silva, *Universidade Federal do Rio Grande do Norte*

TUESDAY AFTERNOON	
GUARATIBA	15:30 - 16:30

Reconfigurable Logic and FPGAs II
Chair: **Renato Ribas** - *UFRGS*

15:30 A RECONFIGURABLE PLATFORM FOR MULTI-SERVICE EDGE ROUTERS
Christoforos Kachris and Stamatis Vassiliadis, *Delft University of Technology*

15:50 AQUARIUS - A DYNAMICALLY RECONFIGURABLE COMPUTING PLATFORM
Jordana Seixas, Stelita Silva, Paulo Sergio Nascimento, Remy Eskinazi, Edson Barbosa, Vinícius Kursancew, Edna Barros and Manoel Eusebio, *Centro de Informática UFPE*

16:10 DESIGN OF ADAPTIVE MULTIPROCESSOR ON CHIP SYSTEMS
Bobda Christophe, Haller Thomas, Jung Simon, Rech Dennis and Felix Muehlbauer, *University of Kaiserslautern*

16:30 - 17:00 Coffee break

TUESDAY AFTERNOON

GUARATIBA 17:00 - 18:00

SoCs and Embedded Systems II

Chair: **David Harris** - *HMC*

17:00 SPECIFICATION OF ALTERNATIVE EXECUTION SEMANTICS OF UML SEQUENCE DIAGRAMS WITHIN ACTOR-ORIENTED MODELS
Leandro Indrusiak and Manfred Glesner, *Technische Universität Darmstadt*

17:20 FPGA INFRASTRUCTURE FOR THE DEVELOPMENT OF AUGMENTED REALITY APPLICATIONS
Germano Guimarães, João Lima, João Teixeira, Guilherme Silva, Veronica Teichrieb and Judith Kelner, *Universidade Federal de Pernambuco, Brazil*

WEDNESDAY MORNING

SÃO CONRADO 10:00 - 12:00

Neural Nets and Intelligent Systems

Chair: **Jose Gabriel Gómes** - *UFRJ*

10:00 HIGH-SPEED, MODEL-FREE ADAPTIVE CONTROL USING PARALLEL SYNCHRONOUS DETECTION
Dimitrios Loizos and Paul Sotiriadis, *The Johns Hopkins University*
Gert Cauwenberghs, *University of California, San Dieg*

10:20 RADIAL BASIS FUNCTION NETWORK APPLIED TO THE LINEARIZATION OF A VOLTAGE CONTROLLED OSCILLATOR
Marcio Lucks, *IAE - Instituto de Aeronáutica e Espaço*
Nobuo Oki, *UNESP Universidade Estadual Paulista*

10:40 VIABILITY OF ANALOG INNER PRODUCT OPERATIONS IN CMOS IMAGERS
Hugo Haas, Jose Gabriel Gomes and Antônio Petraglia, *Federal University of Rio de Janeiro, Brazil*

11:00 CMOS ENCODER FOR SCALE-INDEPENDENT PATTERN RECOGNITION
Julio Saldaña-Pumarica and Carlos Silva-Cárdenas, *Pontificia Universidad Católica del Perú*
Emilio Del-Moral-Hernández, *Escola Politécnica da USP*

WEDNESDAY MORNING

GUARATIBA 10:00 - 12:00

Circuit Test and Verification
Chair: **Homero Santiago Maciel** - *ITA*

10:00 AN OPTIMIZED HYBRID APPROACH TO PROVIDE FAULT DETECTION AND CORRECTION IN SoCs
Leticia Bolzani, Paolo Bernardi and Matteo Sonza Reorda, *Politecnico di Torino*

10:20 A SOFTWARE-BASED METHODOLOGY FOR THE GENERATION OF PERIPHERAL TEST SETS BASED ON HIGH-LEVEL DESCRIPTIONS
Leticia Bolzani, Ernesto Sanchez and Matteo Sonza Reorda, *Politecnico di Torino*

10:40 USING MAJORITY LOGIC TO COPE WITH LONG DURATION TRANSIENT FAULTS
Lorenzo Petroli, Carlos Lisboa, Fernanda Kastensmidt and Luigi Carro, *Instituto de Informática, PGCC, Universidade Federal do Rio Grande do Sul*

11:00 FUNCTIONAL VERIFICATION OF AN MPEG-4 DECODER DESIGN USING A RANDOM CONSTRAINED MOVIE GENERATOR
George Sobral Silveira, Karina R. G. da Silva and Elmar U. K. Melcher, *Universidade Federal Campina Grande*

WEDNESDAY AFTERNOON

SÃO CONRADO 14:30 - 15:30

Circuits for Communications I
Chair: **Flavio Wagner** - *UFRGS*

14:30 BUFFER SIZING FOR QoS FLOWS IN WORMHOLE PACKET SWITCHING NoCs
Leonel Tedesco, Ney Calazans and Fernando Moraes, *PUCRS*

14:50 FITTING THE ROUTER CHARACTERISTICS IN NoCs TO MEET QoS REQUIREMENTS
Edgard de Faria Corrêa, Leonardo Alves de Paula e Silva, Flávio Rech Wagner and Luigi Carro, *Universidade Federal do Rio Grande do Sul*

15:10 ROUTER ARCHITECTURE FOR HIGH-PERFORMANCE NoCs
Everton Carara, Ney Calazans and Fernando Moraes, *PUCRS*

WEDNESDAY AFTERNOON

SÃO CONRADO 14:30 - 16:30

Circuits for Communications II
Chair: **Mohamed Ismail** - *OSU*

15:30 A 9.6 Kb/s CMOS FSK MODEM FOR DATA TRANSMISSION THROUGH POWER LINES
Walter Lancioni, Pablo Petrashin, Luis Toledo and Carlos Dualibe, *Universidad Católica de Córdoba*

15:50 A 4.1 GHZ PRESCALER USING DOUBLE DATA THROUGHPUT E-TSPC STRUCTURES
João Navarro, Fernando de Miranda and Wilhelmus Van Noije, *Universidade de São Paulo*

16:10 TrACS: TRANSCEIVER ARCHITECTURE AND WIRELESS CHANNEL SIMULATOR
Chithrupa Ramesh, Ana Rusu, Mohammed Ismail and Mikael Skoglund, *Royal Institute of Technology, KTH*

WEDNESDAY AFTERNOON

GUARATIBA 14:30 - 16:30

Process and Layout Techniques I
Chair: **David Fries** - *Intelligent MP*

14:30 RAPID FABRICATION OF MICROCIRCUIT DESIGNS USING MASKLESS LITHOGRAPHIC PATTERNING AS AN ALTERNATIVE TO PROCESS SIMULATION FOR OPTIMIZED CIRCUITS
David Fries, *Intelligent MP*
Stan Ivanov, Kevin Stichnot and Heather Broadbent

14:50 CONTRIBUTIONS TO IMPROVE DESIGN ACCURACY OF BIPOLAR ICS VIA PHYSICAL EFFECTS
Agnes Nagy, Alicia Polanco and Manolo Alvarez, *Microelectronics Research Center*

15:10 A QUASI-DIFFERENTIAL QUANTIZER BASED ON SMOBILE
Juan Núñez, José M. Quintana and María J. Avedillo, *IMSE-CNM-CSIC and Universidad de Sevilla*

WEDNESDAY AFTERNOON

GUARATIBA 15:30 - 16:30

Process and Layout Techniques II
Chair: **Marcelo Lubaszewski** - *UFRGS*

15:30 LAYOUT TECHNIQUES FOR RADIATION HARDENING OF STANDARD CMOS ACTIVE PIXEL SENSORS
Leo Huf Campos Braga, Suzana Domingues, Milton Ferreira Rocha, Leonardo Bruno Sá, Filipe Vinci Santos, Antonio Carneiro Mesquita and Mário Vaz Silva, *Federal University of Rio de janeiro, Brazil*
Jacobus Willibrordus Swart and Fernando Campos, *Universidade Estadual de Campinas (UNICAMP)*

15:50 TOTAL IONIZING DOSE EFFECTS IN SWITCHED-CAPACITOR FILTERS USING OSCILLATION-BASED TEST
John M. Espinosa-Duran and Jaime Velasco-Medina, *Universidad del Valle*
Gloria Huertas and José Luis Huertas, *Institute of Microelectronic of Seville*

THURSDAY MORNING

PONTAL 10:00 - 12:00

Device Modeling and Simulation I
Chair: **Ashok Srivastava** - *LSU*

10:00 BUS ENCODING SCHEMES FOR MINIMIZING DELAY IN VLSI INTERCONNECTS
Sainarayanan K S, Raghunandan C and Srinivas M B, *International Institute of Information Technology (IIIT), Hyderabad*

10:20 A BUILT-IN CURRENT SENSOR FOR HIGH SPEED SOFT ERRORS DETECTION ROBUST TO PROCESS AND TEMPERATURE VARIATIONS
Egas Henes Neto, *CEITEC*
Fernanda Lima Kastensmidt and Gilson Wirth, *UFRGS*

10:40 SOFT-WELL DIGITAL CIRCUIT DESIGN
Jens Petter Abrahamsen and Tor Sverre Lande, *University of Oslo*

11:00 TRANSFER CHARACTERISTICS AND HIGH FREQUENCY MODELING OF LOGIC GATES USING CARBON NANOTUBE FIELD EFFECT TRANSISTORS (CNT-FETs)
Jose Marulanda and Ashok Srivastava, *Louisiana State University*
Ashwani Sharma, *Kirtland Air Force Base*

THURSDAY MORNING

GUARATIBA 10:00 - 12:00

SoCs and Embedded Systems III

Chair: **David Harris** - *HMC*

10:00 PARALLELIZED RADIX-4 SCALABLE MONTGOMERY MULTIPLIERS
Nathaniel Pinckney and David Harris, *Harvey Mudd College*

10:20 A TIME PETRI NET-BASED APPROACH FOR HARD REAL-TIME SYSTEMS SCHEDULING CONSIDERING DYNAMIC VOLTAGE SCALING, OVERHEADS, PRECEDENCE AND EXCLUSION RELATIONS
Eduardo Tavares, Bruno Silva and Paulo Maciel, *Federal University of Pernambuco*
Meuse Oliveira Jr, *Education of Pernambuco*

10:40 OBJECT AND METHOD EXPLORATION FOR EMBEDDED SYSTEMS APPLICATIONS
Julio Mattos and Luigi Carro, *Universidade Federal do Rio Grande do Sul - UFRGS*

11:00 ANALYSIS OF THE USE OF DECLARATIVE LANGUAGES FOR ENHANCED EMBEDDED SYSTEM SOFTWARE DEVELOPMENT
Emilena Specht, Ricardo Redin, Luigi Carro, Luís Lamb, Flávio Wagner and Erika Cotta, *UFRGS - Universidade Federal do Rio Grande do Sul*

THURSDAY AFTERNOON

PONTAL 14:30 - 15:30

Device Modeling and Simulation II

Chair: **Ricardo Jacobi** - *UNB*

14:30 MODELING AND ANALYSIS OF CROSSTALK FOR DISTRIBUTED RLC INTERCONNECTS USING DIFFERENCE MODEL APPROACH
Ravindra Jayanthi and Srinivas M B, *International Institute of Information Technology*

14:50 INSTANTANEOUS DE-EMBEDDING OF THE ON-WAFER EQUIVALENT-CIRCUIT PARAMETERS OF ACOUSTIC RESONATOR (FBAR) FOR INTEGRATED CIRCUIT APPLICATIONS
Humberto Campanella, *Centro Nacional de Microelectrónica CNM-CSIC*
Arantxa Uranga, Pedro De Paco and Nuria Barniol, *Universitat Autònoma de Barcelona*
Pascal Nouet, *Laboratoire d'Informatique de Robotique et de Microélectronique de Montpellier LIRMM*
Jaume Esteve, *Centro Nacional de Microelectrónica CNM-CSIC*

15:10 THREE-DIMENSIONAL ON-CHIP INDUCTANCE AND RESISTANCE EXTRACTION
Alexandre Nentchev and Siegfried Selberherr, *Institute for Microelectronics, TU Vienna*

THURSDAY AFTERNOON

PONTAL 15:30 - 16:30

Circuits for Communications III
Chair: **Antonio Queiroz** - *UFRJ*

15:30 A CMOS AM DEMODULATOR FOR INSTRUMENTATION APPLICATIONS
Pietro Maris Ferreira, Antônio Petraglia and Fernando Barúqui, *Federal University of Rio de Janeiro, Brazil*

15:50 DESIGN OF A DIGITAL FM DEMODULATOR BASED ON A 2º ORDER ALL-DIGITAL PHASE-LOCKED LOOP
Juan Pablo Martinez Brito and Sergio Bampi, *Universidade Federal do Rio Grande do Sul - UFRGS*

16:10 DIGITAL PM DEMODULATOR FOR BRAZILIAN DATA COLLECTING SYSTEM
Jose Marcelo Lima Duarte and Francisco Chagas Mota, *Universidade Federal do Rio Grande*
Manoel J. M. de Carvalho, *Instituto Nacional de Pesquisa*

THURSDAY AFTERNOON

GUARATIBA 14:30 - 15:30

RF Circuits

Chair: **Sergio Bampi** - *UFRGS*

14:30 MINIMIZING THE MISMATCH ERRORS AT THE VCO AND CASCODE BUFFERS CONNECTIONS IN FRONT END OF BiCMOS RFICs OPERATING ON S BAND
C. N. M. Marins, *National Institute of Telecommunications Inatel*
L.C. Kretly, *State University of Campinas Unicamp*

14:50 A FULLY INTEGRATED CMOS RF FRONT-END FOR A MULTI-BAND ANALOG MIXED-SIGNAL INTERFACE
Fernando Paixão Cortes and Sergio Bampi, *Universidade Federal do Rio Grande do Sul*

15:10 A 915 MHZ UHF LOW POWER RFID TAG
César Marcon, Fabiano Hessel and Eduardo Bezerra, *PPGCC / FACIN / PUCRS*
José Carlos Palma, *PPGC / INFORMÁTICA / UFRGS*

THURSDAY AFTERNOON

GUARATIBA 15:30 - 16:30

Design Automation Tools
Chair: **Volnei A. Pedroni** - *UTFPR*

15:30 MODEL DRIVEN ENGINEERING FOR MPSoC DESIGN SPACE EXPLORATION
Marcio Oliveira, Eduardo Brião, Francisco Nascimento and Flávio Wagner, *Universidade Federal do Rio Grande do Sul*

15:50 CELL PLACEMENT ON GRAPHIC PROCESSING UNIT
Guilherme Flach, Marcelo Johann, Renato Hentschke and Ricardo Reis, *UFRGS*

16:10 DESIGNING CMOS GATES WITH MINIMUM STACKED TRANSISTORS
Leomar Rosa Jr, Felipe Schneider, Renato Ribas and Andre Reis, *Universidade Federal do Rio Grande do Sul*

Technical Program

SBMicro2007

TUESDAY MORNING

PONTAL 10:30 - 12:00

Thin Films and Processes I

Chair: **José A. Diniz** - *CCS/UNICAMP, Brazil*

10:30 THE EFFECT OF THE Si-SUBSTRATE ON THE OPTICAL CHARACTERIZATION OF Ge NANOSTRUCTURES OBTAINED BY LPCVD
Segundo Nilo Muñoz Mestanza, Eugenio Rodriguez, Ioshiaki Doi, Alfredo Vaz and Newton Cesario Frateschi, *CCS, State University of Campinas, Brazil*

10:50 DYNAMIC SCALING OF THE SURFACE ROUGHNESS DURING ELECTROLESS Cu PLATING ONTO Si IN AQUEOUS FLUORINE SOLUTION
Giuliano Gozzi and Sebastião Santos, LSI/PSI/USP, *University of Sao Paulo, Brazil*

11:10 ECR-CVD SiNX PASSIVATION IN GaAs-BASED MISFET DEVICES
L.B. Zoccal, J.A. Diniz, J. Godoy Fo., A. Daltrini and J. W. Swart, *CCS, State University of Campinas, Brazil*

11:30 DESIGN OF FINISH PROCESS OF FREEFORM SURFACE IN MAGNETIC-ASSISTANCE ELECTROCHEMICAL FINISHING
P.S. Pa, *National Taipei University of Education, Taiwan*

TUESDAY MORNING

ITAIPÚ A 10:00 - 12:00

Multiple Gates
Chair: **Cor Claeys** - *IMEC, Belgium*

10:00 MULTIPLE GATES FOR SOI MOSFETs : TWO, THREE OR FOUR ?
Sorin Cristoloveanu, *IMEP, INP, France* - **Invited Paper**

10:30 Triple Gate FinFET Parameter Extraction Using High Frequency Capacitance - Voltage Curves
Michele Rodrigues, Victor Sonnenberg and João Antonio Martino, *LSI/PSI/USP, University of Sao Paulo, Brazil*

10:50 LOW TEMPERATURE OPERATION OF UNDOPED BODY TRIPLE-GATE FinFETs FROM AN ANALOG PERSPECTIVE
Marcelo Pavanello, *Centro Universitário da FEI, Brazil*
Joao Martino, *LSI/PSI/USP, University of Sao Paulo, Brazil*
Eddy Simoen, Rita Rooyackers, Nadine Collaert and Cor Claeys, *IMEC, Belgium*

11:10 INFLUENCE OF THE N-TYPE FinFET WIDTH ON THE ZERO TEMPERATURE COEFFICIENT
Marcello Bellodi, *Centro Universitário da FEI, Brazil*
João Antonio Martino, *CCS, State University of Campinas (Unicamp Brazil*
Luciano Mendes Camillo, *LSI/PSI/USP, University of Sao Paulo, Brazil*
Eddy Simoen and Cor Claeys, *IMEC, Belgium*

11:30 IMPROVED COMPACT MODEL FOR SYMMETRIC DOPED DOUBLE-GATE MOSFETs
Antonio Cerdeira and Magali Estrada, *CINVESTAV, México*
Benjamín Iñiguez, *Universitat Rovira i Virgili, Spain*

TUESDAY AFTERNOON

ITAIPÚ A 14:30 - 16:30

Thin Films and Processes II
Chair: **Sebastião G. S. Filho** - *LSI/EPUSP, Brazil*

14:30 SEMICONDUCTOR SURFACE CLEANING AND CONDITIONING CHALLENGES BEYOND PLANAR SILICON TECHNOLOGY
Jerzy Ruzyllo, *The Pennsylvania State University, U. S. A.* - **Invited Paper**

15:00 ULTRA-THIN DEFORMABLE SILICON SUBSTRATES WITH LATERAL SEGMENTATION AND FLEXIBLE METAL INTERCONNECT
Theodoros Zoumpoulidis, *Delft Institute of Microelectronics and Submicron Technology, the Netherlands*
Lingen Wang and Leo J. Ernst, *Delft University of Technology, the Netherlands*
Marian Bartek and Kaspar M.B. Jansen, *Delft Institute of Microelectronics and Submicron Technology, the Netherlands*

15:20 STRESS ANALYSIS ON ULTRA THIN GROUND WAFERS
Ricardo Cotrin Teixeira, Chris Van Hoof, *K. U. Leuven, Belgium*
Koen De Munck, Piet De Moor, Kris Baert, Bart Swinnen, *IMEC, Belgium*
Alexansder Knüttel, *Isis Sentronics, Germany*

15:40 ANISOTROPIC RESISTIVITY OF PMMA DOPED WITH GOLD
Fernanda de Sá Teixeira and Ronaldo Domingues Mansano, *LSI/PSI/USP, University of Sao Paulo, Brazil*
Maria Cecília Salvadori and Mauro Cattani, *University of São Paulo, Brazil*
Ian G. Brown, *UC Berkeley, U. S. A.*

16:00 A GRAVIMETERIC TECHNIQUE TO DETERMINE THE CRYSTALLITE SIZE DISTRIBUTION IN HIGH POROSITY NANOPOROUS SILICON
Monuko du Plessis, *University of Pretoria, South Africa*

16:30 - 17:00 Coffee break

TUESDAY AFTERNOON

ITAIPÚ A 17:00 - 18:00

Sensors and Actuators
Chair: **Nilton Morimoto** - *LSI/EPUSP, Brazil*

17:00 STUDY OF NICKEL SILICIDE AS MASK FOR ALKALINE SOLUTIONS TO V-GROOVES FABRICATION
Amanda Mascaro, Luiz Gonçalves and Nilton Morimoto, *LSI/PSI/USP, University of Sao Paulo, Brazil*

17:20 ZINC-OXIDE SURFACE ACOUSTIC WAVE DEVICE FABRICATION
Edval Santos and A Santos, *Universidade Federal de Pernambuco, Brasil*

17:40 INFLUENCE OF THE INTERFERENCES IN THE NITRITE DETECTION BY USING PLANAR ELECTROCHEMICAL SENSORS
Fernando Almeida, *Centro Universitário da FEI, Brazil*
Marcelo B. A. Fontes, *LSI/PSI/USP, University of Sao Paulo, Brazil*

TUESDAY AFTERNOON

PONTAL 15:00 - 16:30

Characterization and Modeling I
Chair: **João Antonio Martino** - *LSI/EPUSP, Brazil*

15:00 THE IMPACT OF THE GATE OXIDE THICKNESS REDUCTION ON THE GATE INDUCED FLOATING BODY EFFECT IN SOI nMOSFETs
Paula Agopian and João Martino, *LSI/PSI/USP, University of Sao Paulo, Brazil*
Eddy Simoen and Cor Claeys, *IMEC, Belgium*

15:20 A STUDY OF FLICKER NOISE IN MOS TRANSISTOR UNDER SWITCHED BIAS CONDITION
Matias Miguez and Alfredo Arnaud, *Universidad Católica de Montevideo, Uruguay*

15:40 ANALYSIS OF MATCHING IN GRADED-CHANNEL SOI MOSFETs
Michelly de Souza, *LSI/PSI/USP, University of Sao Paulo, Brazil*
Denis Flandre, *Université Catholique de Louvain, Belgium*
Marcelo Pavanello, *Centro Universitário da FEI, Brazil*

16:00 FUNDAMENTALS, COMPUTER IMPLEMENTATION AND APPLICATIONS OF THE ADVANCED COMPACT MOSFET (ACM) MODEL
Osmar Franca Siebel, Márcio Cherem Schneider and Carlos Galup-Montoro, *Federal University of Santa Catarina, Brazil.*

16:30 - 17:00 Coffee break

TUESDAY AFTERNOON

PONTAL 17:00 - 18:00

MEMS

Chair: **Renato Ribas** - *UFRGS, Brazil*

17:00 SILICON MICROTIPS WITH SELF-ALIGNED INTEGRATED ELECTRODES
Alex de Lima Barros, Alexandre Lopes Tavares and Marcelo Nelson Páez Carreño, *University of São Paulo, Brazil*

17:20 SILICON MICROTIPS ARRAYS FABRICATED BY HI-PS TECHNIQUE FOR APPLICATION IN FIELD EMISSION DEVICES
Michel Dantas, M. Kopelvski, Elizabete Galeazzo, Henrique Peres and Francisco Fernandez, *LME, EPUSP, University of São Paulo, Brazil*

17:40 SIMPLE MEMS-BASED INCANDESCENT MICROLAMPS
Gustavo P. Rehder, Marcelo N. P. Carreno and Marco I. Alayo, PSI, *University of São Paulo, Brazil*

WEDNESDAY MORNING

ITAIPÚ A 10:00 - 12:00

Characterization and Modeling II
Chair: **Marcelo Antonio Pavanello** - *FEI, Brazil*

10:00 PHYSICAL CHARACTERIZATION AND RELIABILITY ASPECTS OF MuGFETs
C. Claeys and E. Simoen, *IMEC, Belgium*
J.M. Rafi, *IMB-CNM-CSIC, Spain*
M. Pavanello, *Centro Universitário da FEI, Brazil*
J. Martino, *LSI/PSI/USP, University of Sao Paulo, Brazil* - **Invited Paper**

10:30 IMPROVED MODEL TO DETERMINE THE GENERATION LIFETIME IN DOUBLE GATE SOI nMOSFETs
Milene Galeti and João Antonio Martino, *LSI/PSI/USP, University of Sao Paulo, Brazil*
Eddy Simoen and Cor Claeys, *IMEC, Belgium*

10:50 SIDEWALL ANGLE INFLUENCE ON THE FinFET ANALOG PARAMETERS
Renato Giacomini and Marcelo Antonio Pavanello, *Centro Universitário da FEI, Brazil*
João Antonio Martino, *LSI/PSI/USP, University of Sao Paulo, Brazil*

11:10 THE COHERENT FinFET
Carlo Requiao da Cunha, *Federal University of Santa Catarina, Brazil*

11:30 A NEW METHOD FOR POLYNOMIAL COEFFICIENT EXTRACTION APPLIED TO HARMONIC DISTORTION CALCULATION
Adelmo Ortiz-Conde, Francisco García-Sánchez and Ramon Salazar, *Universidad Simón Bolívar, Venezuela*

WEDNESDAY AFTERNOON

ITAIPÚ A 14:30 - 15:30

Thin Films and Processes III

Chair: **Ioshiaki Doi** - *FEEC/UNICAMP, Brazil*

14:30 CONTACT IMPROVEMENT FOR CARBON NANOTUBES DEPOSITED BY DIELECTROPHORESIS
J. Leon, A. Vaz, S. Moshkalev, A. R. Flacker and J. W. Swart, *CCS, State University of Campinas, Brazil*
M. B. de Moraes, *IFGW, UNICAMP, Brazil*

14:50 SIMULATION, FABRICATION AND CHARACTERIZATION OF A TUNABLE BRAGG REFLECTOR BASED ON SILICON OXIDE AND SILICON NITRIDE DIELECTRIC FILMS DEPOSITED BY PECVD
G. Martins, H. Baez and M.I. Alayo, *PSI, University of São Paulo, Brazil*

15:10 PHOTORESPONSE ANALYSIS OF SENSORS FABRICATED WITH STANDARD 2.0 μm CMOS TECHNOLOGY
Segundo Nilo Muñoz Mestanza, Eugenio Rodriguez, Ioshiaki Doi, José Alexandre Diniz, Jacobus Swart and Newton Cesário Frateschi, *CCS, State University of Campinas, Brazil*

WEDNESDAY AFTERNOON

PONTAL 15:30 - 16:30

Poster Section

Chair: **João Antonio Martino** - *LSI/EPUSP, Brazil*

DISTORTION ANALYSIS OF TRIPLE GATE TRANSISTORS IN SATURATION
Jorge Evaristo Conde, *Simón Bolívar University, Venezuela*
Antonio Cerdeira and Magali Estrada, *CINVESTAV, México*

ON THE THRESHOLD VOLTAGE OF UNDOPED DOUBLE-GATE SOI MOSFETs
Francisco García-Sánchez, Adelmo Ortiz-Conde, Juan Muci and Ramon Salazar, *Simón Bolívar University, Venezuela*

THE INFLUENCE OF SUBSTRATES ON THE CARBON NANOTUBE GROWTH PROCESS
Marina R. de Aguiar, *PSI, University of São Paulo, Brazil*
Carla Verissimo, Stanislav A. Moshkalev and Jacobus W. Swart, *CCS, State University of Campinas, Brazil*

ETCHING STUDIES OF POST-ANNEALED SiC FILM DEPOSITED BY PECVD: Influence OF THE OXIGEN CONCENTRATION
Mariana Amorim Fraga, Rodrigo Savio Pessoa, Marcos Massi, Homero Santiago Maciel and Sebastião Gomes dos Santos Filho, *Technological Institute of Aeronautics, Brazil*

ELECTRICAL CHARACTERIZATION OF PLATINUM THIN FILMS DEPOSITED BY FOCUSED ION BEAM
M.M da Silva, A. R. Vaz, S. A. Moshkalev and and J. W. Swart, *CCS, State University of Campinas, Brazil*

NOVEL EUROPIUM BETA-DIKETONATE COMPLEX IN ORGANIC LIGHT EMITTING DIODE: Eu(BTA)3bipy [tris(1-(2-benzoyl)-3,3,3-trifluoroacetone))-bipyridine, Europium(III)]
Gerson Santos, Fernando Fonseca, and Adnei Andrade, *LME, EPUSP, University of São Paulo, Brazil*
Susana Braga, Ana Coelho, Isabel Gonçalves, Wilson Simões and Luiz Pereira, *Universidade de Aveiro, Portugal*

DEPOSITION AND CHARACTERIZATION OF INDIUM-TIN OXIDE THIN FILMS DEPOSITED BY RF SPUTTERING
Larissa Damiani and Ronaldo Mansano, *LSI/PSI/USP, University of Sao Paulo, Brazil*

ELECTRICAL CHARACTERIZATION OF a-C:H AS INSULATOR MATERIAL IN MIM STRUCTURES
Carlos Zuñiga-Islas, Andrey Kosarev, Alfonso Torres-Jacome, Claudia Reyes-Betanzo, Wilfrido Calleja-Arriaga and Pedro Rosales-Quintero, *INAOE, Mexico*

CLUSTERS FORMATION BY RAPID THERMAL ANNEALING ON SiO2/Ge AND SiH/Ge HETEROSTRUCTURES
Alexandre Miranda Pires dos Anjos, José Alexandre Diniz, Leonardo Zoccal, Mara Canesqui and Ioshiaki Dói, *CCS, State University of Campinas, Brazil*
Ursula Mengui, *National Institute of Space Research, Brazil*

STUDY OF THE DRAIN LEAKAGE CURRENT BEHAVIOR IN CIRCULAR GATE SOI nMOSFET Using 0.13µm SOI CMOS TECHNOLOGY AT HIGH TEMPERATURES
Luciano Mendes Almeida and Marcello Bellodi, *Centro Universitário da FEI, Brazil*

10 GHz RF PASSIVE COMPONENTS OBTAINED BY MCM-D TECHNOLOGY
L. B. Zoccal, C.M. Cabreira, S.D. Yamamoto, R. A. Flacker, E.A. Gomes, J. A. Diniz and J. W. Swart, *CCS, State University of Campinas, Brazil*

THREE-DIMENSIONAL (3-D) ELECTRO-THERMAL SIMULATION OF FOUR-LAYER DEVICES
Rodolfo Quintero-Romo, *CINVESTAV, Mexico*

COUPLED QUANTUM DOT CELL DYNAMICS
Marcelo F. Stella, Marcus V. Batistuta and José Camargo da Costa, *University of Brasilia, Brazil*

STABILITY OF COUPLED QUANTUM DOT CELLS AT FINITE TEMPERATURES
Marcus Vinicius Batistuta, Marcelo F. Stella and José Camargo da Costa, *University of Brasilia, Brazil*

IMPACT OF GRADED-CHANNEL SOI MOSFET APPLICATION ON THE PERFORMANCE OF CASCODE AND WILSON CURRENT MIRRORS
André Santos and Marcelo Pavanello, *Centro Universitário da FEI, Brazil*
Denis Flandre,

IMPROVED CHARGE SHEET MODEL FOR PD SOI SUB-MICRON MOSFETs
Joaquin Alvarado and Antonio Cerdeira, *CINVESTAV, México*
Valeria Kilchytska, *Université Catholique de Louvain, Belgium*
Denis Flandre, *Université Catholique de Louvain, Belgium*

STUDY OF MOS CAPACITORS WITH ANNEALED TiO2 GATE DIELECTRIC LAYER
Katia Franklin Albertin, Marcio Valle and Inés Pereyra, *LME, EPUSP, University of São Paulo, Brazil*

MICROSTRUCTURAL AND ELECTRICAL CONDUCTIVITY RELATIONSHIPS IN ALUMINA-CONTAINING YTTRIA STABILIZED CUBIC ZIRCONIA USED AS A SOLID ELECTROLYTE IN SOLID OXIDE FUEL CELLS
Suleyman Tekeli, Ahmet Kayis, Osman Gurdal and Metin Guru, *Gazi University, Turkey*

PRECISION RECYCLE PROCESS OF ITO REMOVAL FROM COLOR FILTER USING ELECTROCHEMICAL MACHINING
P.S. Pa, *National Taipei University of Education, Taiwan*

EFFECT OF NUMBER OF LAYERS ON THE OPTICAL RESPONSE OF POROUS SILICON BRAGG'S MIRRORS
Danilo Roque Huanca and Walter Jaimes Salcedo, *LME, EPUSP, University of São Paulo, Brazil*

A THEORETICAL STUDY OF A NOVEL MULTI-TERMINAL PRESSURE SENSOR BASED ON THE TRANSVERSAL PIEZORESISTIVE EFFECT
Guilherme Coraucci and Fabiano Fruett, *University of Campinas, Brazil*

CHARACTERIZATION OF A ISFET DEVICE AS A pH SENSOR FOR APPLICATIONS IN THE INDUSTRIAL, ENVIRONMENTAL AND BIOMEDICAL FIELDS
Robson Scaff, Marcelo B. A. Fontes and Sebastião G. S. Filho, *LSI/ PSI/USP - University of São Paulo, Brazil*

MACROPOROUS SILICON STRUCTURE FUNCTIONALIZED BY METHYLENE BLUE TO pH MEASUREMENTS APPLICATION
Daniel Raimundo, Gustavo Cechelero, Francisco Ramirez-Fernandez, A. A. Costa and Walter Salcedo, *LME, EPUSP, University of São Paulo, Brazil*

CHARACTERIZATION OF A P3HT- Si HETEROJUNTION FOR SOLAR CELLS APPLICATIONS

Jairo Cesar Nolasco, Magali Estrada and Yasuhiro Matsumoto, *INAOE , Mexico*
Lluis Francesc Marsal and Josep Pallares, *Universitat Rovira i Virgili, Spain*

THURSDAY MORNING

ITAIPÚ A 10:00 - 12:00

Characterization and Modeling III
Chair: **José Camargo da Costa** - *UnB, Brazil*

10:00 ELECTROMIGRATION MODELING FOR INTERCONNECT STRUCTURES IN MICROELECTRONICS
H. Ceric and S. Selberherr, *TU Wien, Austria* - **Invited Paper**

10:30 THE LENGTH-DEPENDENCE OF THE 1/f NOISE OF GRADED-CHANNEL SOI nMOSFETs
Eddy Simoen and Cor Claeys, *IMEC, Belgium*
Tsung Ming Chung, Denis Flandre and Jean-Pierre Raskin, *Université catholique de Louvain, Belgium*

10:50 MODELING NEGATIVE DIFFERENTIAL RESISTANCE (NDR) DEVICES USING RADIAL BASIS FUNCTION NEURAL NETWORKS
Monique Bandeira, Janaina Guimaraes, Jussara Durães, Lorena Silva, Artemis Ceschin, , Maria José Sales and José Camargo da Costa, *University of Brasilia, Brazil*

11:10 ELECTRICAL STUDIES ON METAL/SrTa2O6 OR TiO2/Si SUBSTRATE STACK SYSTEMS
Osama Awadelkarim, Jiayu Jiang, Samia Suliman, Karthik Saraptwari and Lucas Passmore, D.O- Lee, P. Roman and J. R. Ruzyllo, *The Pennsylvania State University, U. S. A.*

11:30 REVERSIBLE ELECTRICAL CHARACTERISTICS IN PMMA ON P3HT OTFTs
Israel Mejía, Magali Estrada and Antonio Cerdeira, *CINVESTAV-IPN, Mexico*
Benjamin Iniguez, *Universitat Rovira i Virgili, Spain*

THURSDAY AFTERNOON

ITAIPÚ A 14:30 - 16:30

Thin Films and Processes IV

Chair: **Jacobus Swart** - *CenPRA, Brazil*

14:30 ADVANCED ESD PROTECTION SOLUTIONS IN CMOS/BiCMOS TECHNOLOGIES
Juin J. Liou and Zhiwei Liu, *University of Central Florida, U. S. A.*
Javier A. Salcedo, *Analog Devices Inc., U. S. A.*- **Invited Paper**

15:00 EFFECT OF THE SUBSTRATE HEATING DUE TO THE SPUTTERING PROCESS ON THE CRYSTALLINITY OF TiO2 THIN FILMS
Helson Toku, Rodrigo S. Pessoa, Tiago B. Liberato, Marcos Massi, Homero S. Maciel and A.S.da Silva Sobrinho, *Technological Institute of Aeronautics, Brazil*

15:20 ELECTROLESS DEPOSITION OF CuNiP ALLOYS ONTO SILICON SURFACES
Fernando Parra and Sebastião Santos, *LSI/PSI/USP, University of Sao Paulo, Brazil*
Angelo Marques and Sandro Martini, *Universidade São Judas Tadeu, Brazil*

15:40 IMPROVEMENT OF POLYMERIC ELECTROLUMINESCENT DEVICE STRUCTURES THROUGH SIMULATION OF UV-Vis ABSORPTION SPECTRA OF PANI/PVS FILMS
John Paul Lima and Adnei Andrade, *University of São Paulo, Brazil*

16:00 GaAs AND AlGaAs REACTIVE ION ETCHING IN SiCl4/Ar GAS MIXTURES FOR HEMT APPLICATIONS
Alcinei Nunes, *FEEC-UNICAMP, Brazil*
Stanislav Moshkalev and Peter Tatsch, *CCS, State University of Campinas, Brazil*
Celso Duarte and Guennadii Gusev, *University of São Paulo, Brazil*

Technical Program

SForum2007

WEDNESDAY

FOYER 15:30 - 16:30

Poster Session: Design

Chair: **Renato Ribas** - *UFRGS*

A MPEG-4 DECODER DESIGN VERIFICATION USING FUNCTIONAL COVERAGE
Leandro M. de L. Silva, Romulo C. P. Camara, Maria de L. N. Neta, Helder F. de A. Oliveira, Fabrício G. L. de Melo, Karina R. G. da Silva and Elmar U. K. Melcher, *UFCG*

CHARGE PUMP CURRENT LIMITATION AND DRIVER
André Luís Mansano, Jader De Lima and Jacobus Swart, *UNICAMP*

ANALYSIS AND MODELING OF MULTI-PHASE BUCK REGULATORS APPLIED TO MICROPROCESSORS
Fernando Zampronho, Jader De Lima and Jacobus Swart, *UNICAMP*

ELECTROMAGNETICS SCATTERING SIMULATIONS OF SYSTEM-ON-CHIP USING TLM-JSN WITH DIAKOPTICS TECHNIQUE
N. Carvalho Pinheiro, C. Tenório de Carvalho Jr., J. Camargo da Costa and L. R.A.X. de Menezes, *UNB*

DERIVATIVE APPROXIMATION FOR ANALOG DESIGN
Marcio Lucks and Nobuo Oki, *UNESP*

AUTOMATIC ARCHITECTURE GENERATION FOR COARSE-GRAINED RECONFIGURABLE ARRAY
Tiago Teixeira, Brian Luppi and Ricardo Ferreira, *UFV*

VERIFICATION COVERAGE AND SYNTHESIS OF AN ETHERNET ASIC
Vitor Righi, Robert Torrel, Marco Hennes, Lucio Prade and Rafael dos Santos, *UNISC*

PDESIGNER – A MPSOC MODELING FRAMEWORK
André Souza, Millena Almeida, Williams Azevedo, Cristiano Araújo, Filipe Rolim and Abel Silva, *UFPE*

ANALYSIS AND VALIDATION OF 8 POINT RADIX-2 TIME DECIMATION FFT ALGORITHMIC
Rafael Mallmann and Fernanda Kastensmidt, *UFRGS*

RECONFIGURABLE CORDIC BASED DIGITAL MODULATOR
Bruno Vitorino, Fernando Sousa and Manoel Jozeane, *UFRN*

SET OF DIGITAL CELLS ACCORDING TO LOGIC EQUIVALENCES
Marcos Ledur, Leomar Rosa Jr, Andre Reis and Renato Ribas, *UFRGS*

IPPC: INTELLECTUAL PROPERTY PROCESSOR COMPONENT APPLIED IN EMBEDDED COMPUTER SYSTEMS
Alexandre Marques Amaral, Márcio Oliveira Soares de Souza and Carlos Augusto Paiva da Silva Martins, *PUCMINAS*

COMBINATIONAL BLOCK GENERATION FOR LIBRARY VALIDATION OF BENCHMARK CIRCUITS
Mateus Gomes, Simone Bavaresco, André Reis and Renato Ribas, *UFRGS*

LEE: A LEAKAGE ESTIMATION ENVIRONMENT
Mateus Gomes, Fábio Pereira, Leomar Rosa Jr., André Reis and Renato Ribas, *UFRGS*

CONFIGURABLE RING OSCILLATOR FOR LOGIC CELL EVALUATION
Fabio Pereira, Carlos Afonso Silva, Dionatan Moura, Leomar da Rosa Jr., Andre Reis and Renato Ribas, *UFRGS*

LOGICAL SYNTHESIS FOR EFFICIENT CMOS TRANSISTOR NETWORK

Dionatan Moura, Caio Alegretti, Leomar da Rosa Jr., André Reis and Renato Ribas,
UFRGS

WEDNESDAY

PONTAL 15:30 - 16:30

Poster Session: Technology
Chair: **Victor Sonnenberg** - *FATEC, SP*

HARMONIC DISTORTION COMPARISON BETWEEN CIRCULAR GATE AND CONVENTIONAL Soi NMOSFET USING 0.13 µm PARTIALLY-DEPLETED SOI CMOS TECHNOLOGY
Leandro Dantas and Salvador Gimenez, *Centro Univ. FEI*

COMPARISON OF THE DRAIN LEAKAGE CURRENT BETWEEN A CONVENTIONAL AND A DOUBLE GATE SOI NMOSFETS AT HIGH TEMPERATURES
Alfonso Gutierrez and Bellodi Marcello, *Centro Univ. FEI*

PLANK TRANSISTOR: A NEW GATE STRUCTURE TO REDUCE DIE AREA
Vinicius Mello dos Santos and Salvador Pinillos Gimenez, *Centro Univ. FEI*

RADIATION INFLUENCE ON Soi CMOS DEVICES
Marcio Martino, Marcelo Sandri, Paula Agopian, Milene Galeti, Wilhelmus Noije and João Martino, *USP*

SHORT-CHANNEL EFFECTS IMPROVEMENT BY USING DOUBLE-GATE Soi MOSFET
Sara Dereste dos Santos, Michelly de Souza and João Antônio Martino, *USP*

NUMMERICAL ANALYSIS OF BEVELED STRUCTURES
Felipe Della Lucia and Jacobus Swart, *UNICAMP*

STUDY OF HIGH TEMPERATURE INFLUENCE ON HIGH FREQUENCY C-V CHARACTERISTICS OF MOS CAPACITOR
Ana Paula Ziliotto and Marcello Bellodi, *Centro Univ. FEI*

THRESHOLD VOLTAGE OF DOUBLE AND TRIPLE GATE SOI FINFET
Maria Andrade and Joao Martino, *USP*

THE HALO INFLUENCE ON PD SOI N-MOSFETS AT LOW TEMPERATURE OPERATION
Julia Maria Arrabaça, Paula Der Agopian and João Martino, *USP*

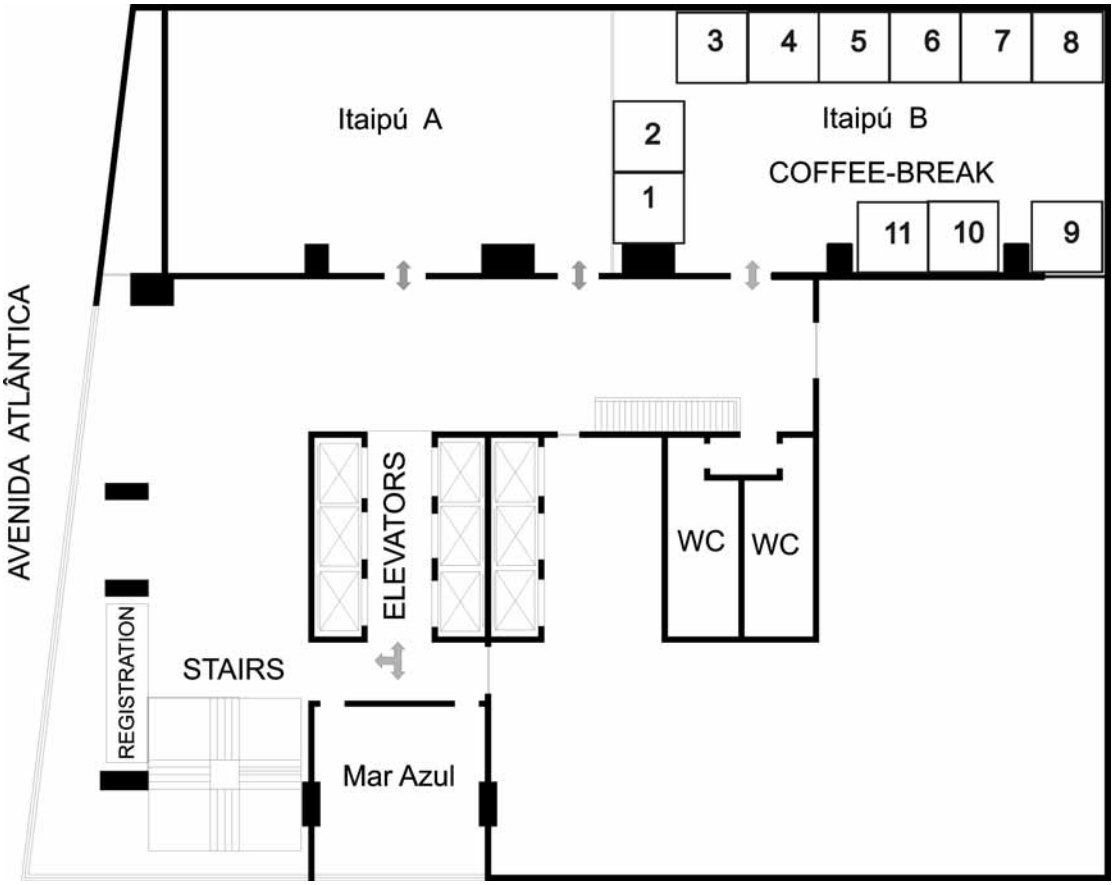
TRANSCONDUCTANCE AND TRANSCONDUCTANCE OVER DRAIN CURRENT RATIO BEHAVIORS IN CIRCULAR GATE Soi NMOSFET BY USING 0.13 µm PARTIALLY-DEPLETED Soi CMOS TECHNOLOGY
Wellington Silva and Salvador Gimenez, *Centro Univ. FEI*

FIELD EMISSION DEVICES ELECTRICAL CHARACTERISTICS TRIAL SYSTEM
Maycon Kopelvski, Michel Dantas, Elisabete Galeazzo, Henrique Peres and Francisco Fernandez, *USP*

DOUBLE-EFFICIENCY QUAD-CELL FOR OPTICAL POSITION SENSING
Pedro Retes, Édilla Fernandes, Luciana Salles, André Furtado and Davies Monteiro, *UFMG*

CHARACTERIZATION OF A ROM TEST STRUCTURE DESIGNED FOR A SOC FOR IRRIGATION CONTROL
Jose Edil Guimaraes de Medeiros, Gilmar Silva Beserra, Helder Henrique Guimaraes, Adson Ferreira da Rocha and Jose Camargo da Costa, *UNB*

Rio Othon Palace



1st Floor

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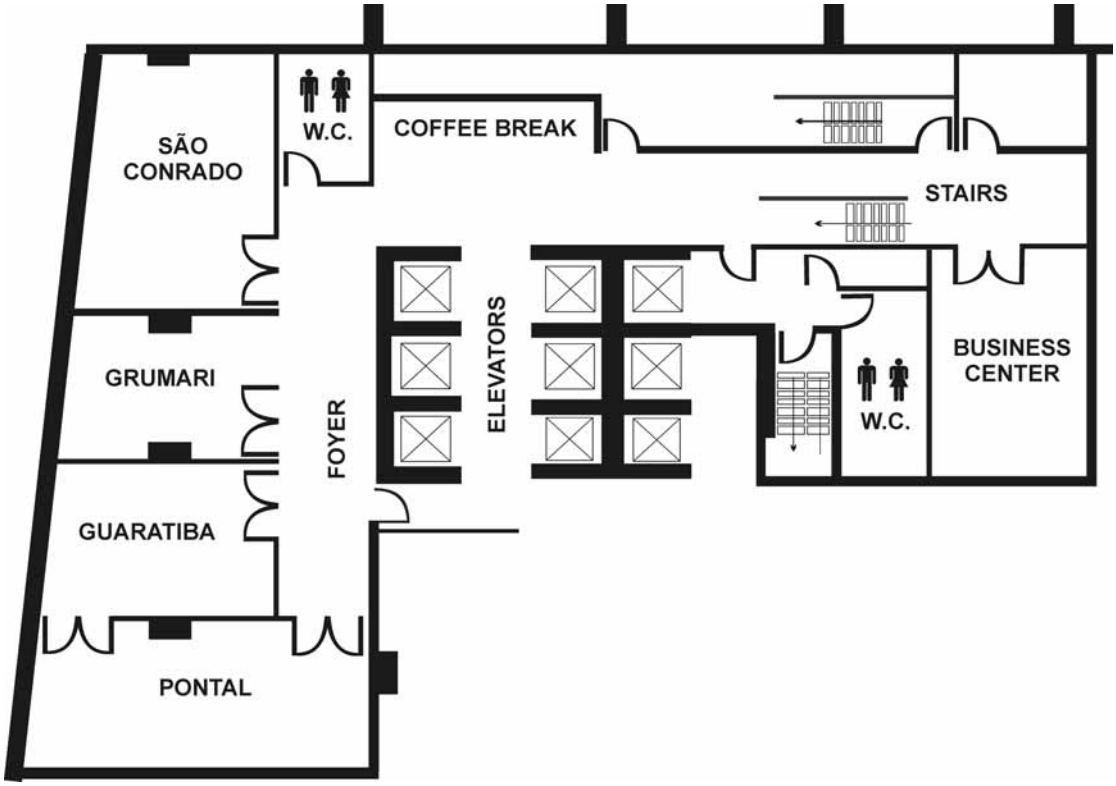

2nd Floor